

Adjustable shunt regulator

TL432KA3/N3/M3

Description

The TL432K is a three terminal adjustable shunt regulator with thermal stability guaranteed over temperature. The output voltage can be adjusted to any value from 1.24V (V_{REF}) to 16V with two external resistors. The TL432 has a typical dynamic output impedance of 0.05Ω . Active output circuitry provides a very sharp turn on characteristic, making TL432 an excellent replacement for zener diodes. The TL432 shunt regulator is available with two voltage tolerances (0.5%, and 1%), and three package options (TO-92, SOT-23 and SOT-89).

This allows the designer the opportunity to select the optimum combination of cost and performance for their application.

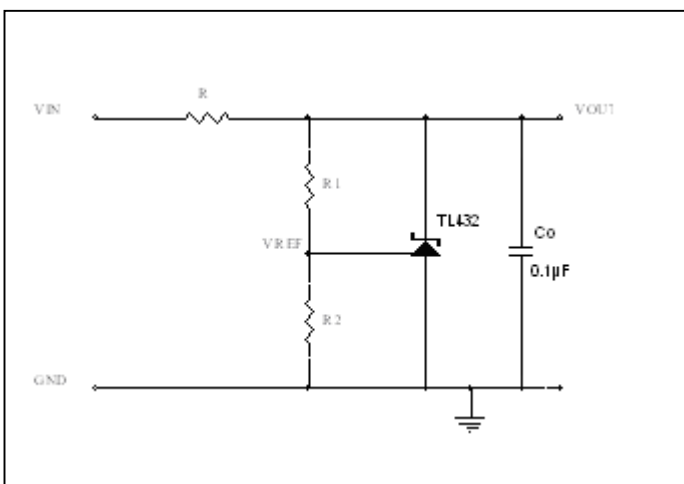
Features

- ◆ Low voltage operation (down to 1.24V)
- ◆ Fast turn on response
- ◆ Low dynamic output impedance 0.05Ω typ.
- ◆ Trimmed bandgap design : $\pm 0.5\%$
- ◆ Operating current range : $80 \mu A \sim 100mA$
- ◆ Available in TO-92, SOT-23, and SOT-89 packages

Applications

- ◆ Linear Regulators
- ◆ Adjustable Supplies
- ◆ Switching Power Supplies
- ◆ Battery Operated Computers
- ◆ Instrumentation
- ◆ Computer Disk Drives

Typical Application Circuit (Note 1,2)



Notes:

- 1) Set V_{OUT} according to the following equation:

$$V_{OUT} = V_{REF}(1 + R1/R2) + I_{REF}R1$$
- 2) Choose the value for R as follows:
 - The maximum limit for R should be such that the cathode current, I_z , is greater than the minimum operating current ($80 \mu A$) at $V_{IN(MIN)}$.
 - The minimum limit for R should be as such that I_z does not exceed 100mA under all load conditions, and the instantaneous turn-on value for I_z does not exceed 150mA. Both of the following conditions must be met:

$$R_{min} \geq V_{IN(max)} / 150mA \text{ (to limit instantaneous turn-on } I_z)$$

$$R_{min} \geq \frac{V_{IN(max)} - V_{OUT}}{I_{OUT(min)} + 100mA} \text{ (to limit } I_z \text{ under normal operating conditions)}$$



Absolute Maximum Ratings

Parameter	Symbol	Maximum	Units
Cathode Voltage	V _Z	20	V
Continuous Cathode Current	I _Z	100	mA
Reference Input Current	I _{REF}	3	mA
Power Dissipation at T _A =25°C			
SOT-23	P _D	0.18	W
SOT-89		0.4	
TO-92		0.5	
Thermal Resistance			
SOT-23	R _{θJA}	556	°C/W
SOT-89		250	
TO-92		200	
ESD susceptibility(HBM) (Note)	V _{ESD}	2000	V
Operating Ambient Temperature Range	T _A	-40 to +85	°C
Operating Junction Temperature Range	T _J	-40 to +125	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

Note : Human body model, 1.5kΩ in series with 100pF

Electrical Characteristics

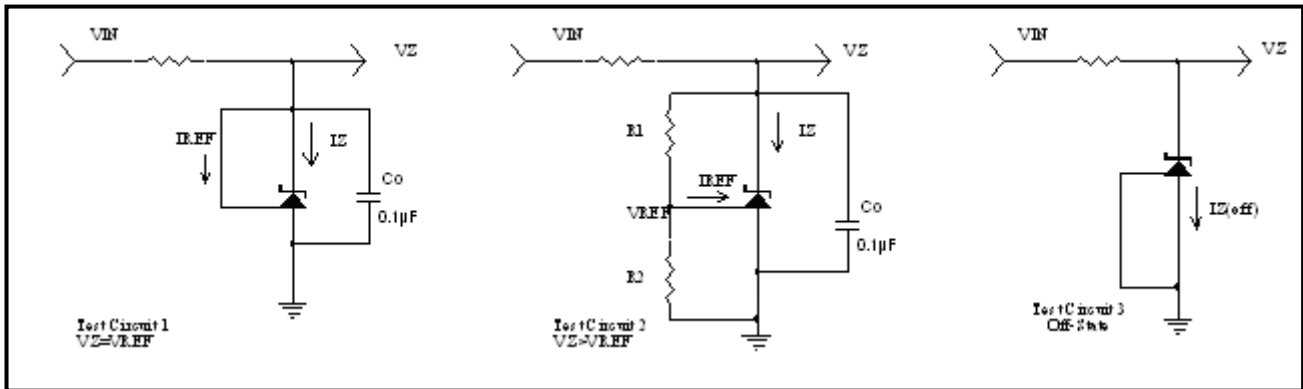
(At 25°C free air ambient temperature, unless otherwise noted.)

Parameter	Symbol	Condition	TL432 A-rank(±0.5%)			TL432 B-rank(±1%)			Unit
			Min	Typ	Max	Min	Typ	Max	
Reference Voltage	V _{REF}	V _Z =V _{REF} , I _Z =10mA (Note 1)	1.234	1.240	1.246	1.228	1.240	1.252	V
V _{REF} Temperature Deviation	V _{DEV}	V _Z =V _{REF} , I _Z =10mA, T _A =-40~85°C (Note 1)	-	10	25	-	10	25	mV
Ratio of Change in V _{REF} to change in V _Z	$\frac{\Delta V_{REF}}{\Delta V_Z}$	I _Z =10mA, ΔV _Z =16V to V _{REF}	-	-1	-2.7	-	-1	-2.7	mV/V
Reference Input Current	I _{REF}	R1=10kΩ, R2=∞, I _Z =10mA (Note2)	-	0.15	0.5	-	0.15	0.5	μA
I _{REF} Temperature Deviation	I _{REF(DEV)}	R1=10kΩ, R2=∞, I _Z =10mA (Note 2)	-	0.1	0.4	-	0.1	0.4	μA
Off-state Cathode Current	I _{Z(OFF)}	V _{REF} =0V, V _Z =16V (Note 3)	-	0.14	0.5	-	0.14	0.5	μA
Dynamic Output Impedance	r _Z	f < 1kHz, V _Z =V _{REF} I _Z =1mA to 100mA (Note 1)	-	0.05	0.2	-	0.05	0.2	Ω
Minimum Operating Current	I _{Z(MIN)}	V _Z =V _{REF} (Note 1)	-	20	80	-	20	80	μA

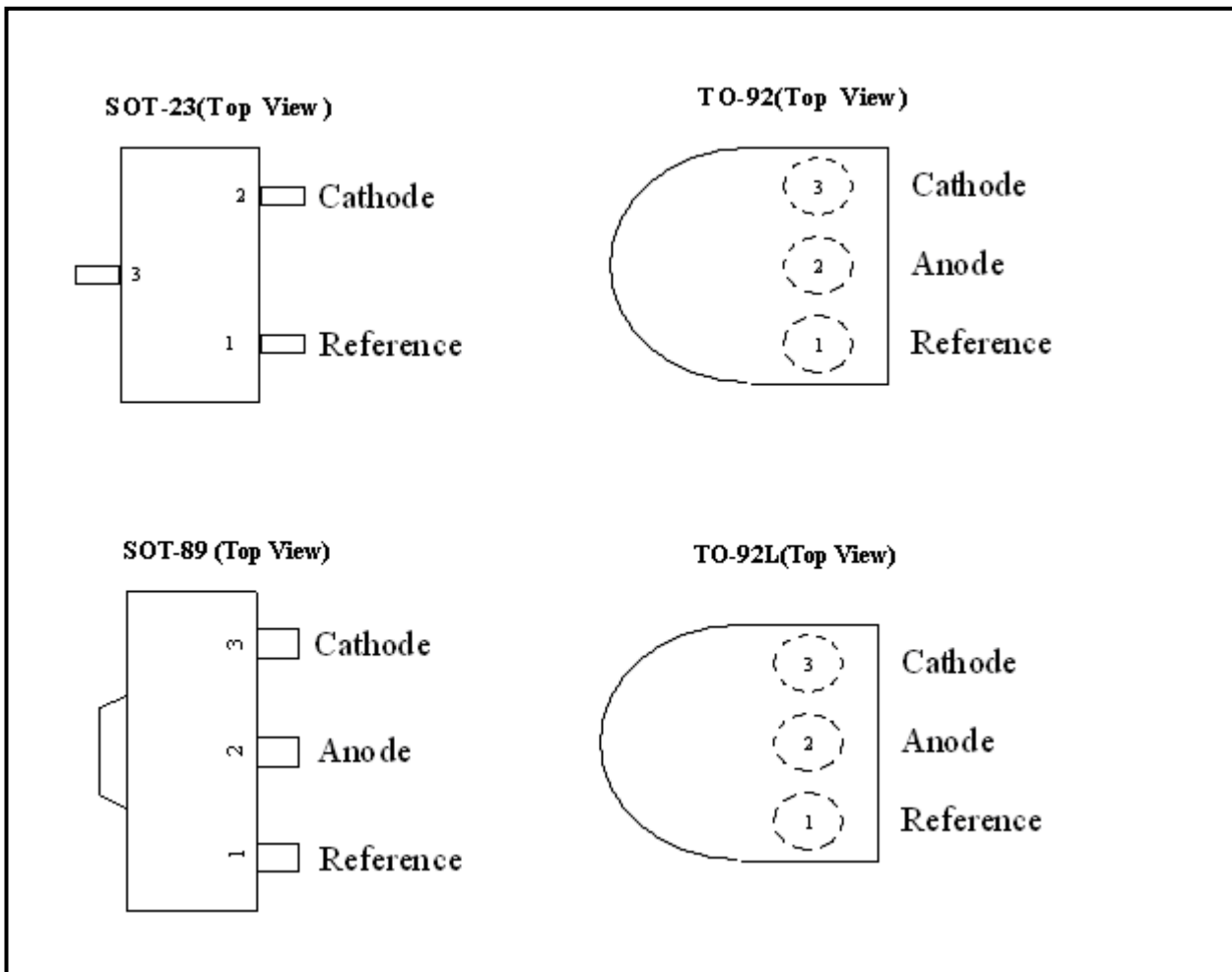
Notes:

- (1) See Test Circuit 1.
- (2) See Test Circuit 2.
- (3) See Test Circuit 3.

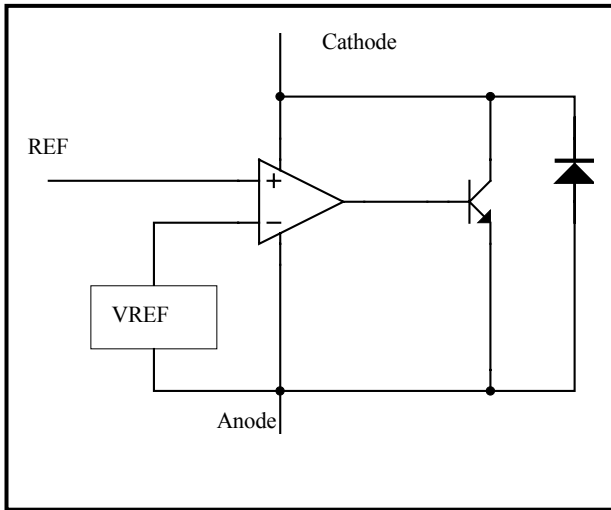
Test Circuits



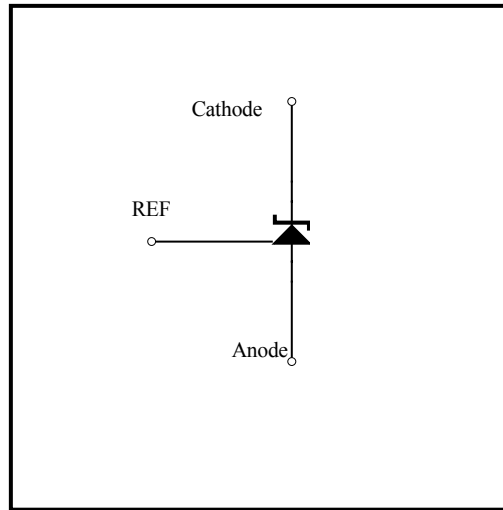
Pin Configurations



Block Diagram

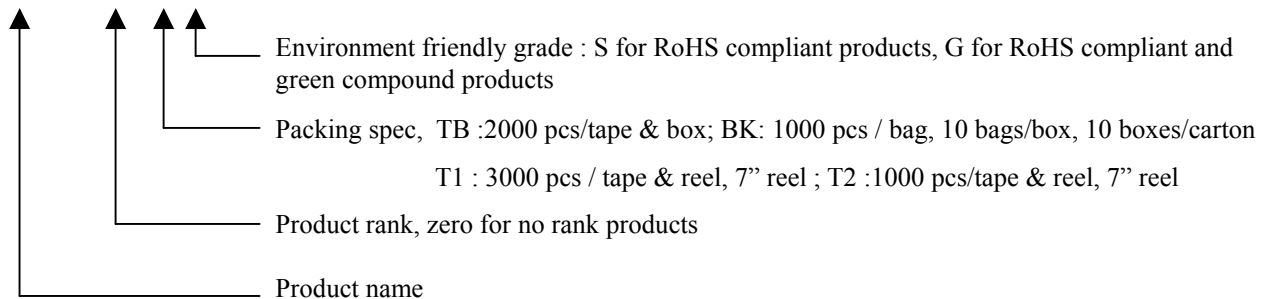


Symbol



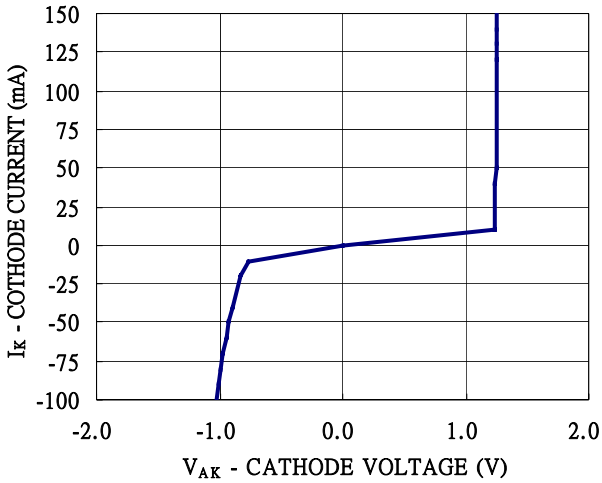
Ordering Information

Device	Package	Rank	Tolerance	Shipping
TL432KA3-A-TB-G	TO-92 (Pb-free lead plating and halogen-free package)	A	±0.5%	2000 pcs / Tape & Box
TL432KA3-B-TB-G		B	±1%	
TL432KA3-A-BK-G		A	±0.5%	1000 pcs/ bag, 10 bags/box, 10boxes/carton
TL432KA3-B-BK-G		B	±1%	
TL432KN3-A-T1-G	SOT-23 (Pb-free lead plating and halogen-free package)	A	±0.5%	3000 pcs / Tape & Reel
TL432KN3-B-T1-G		B	±1%	
TL432KM3-A-T2-G	SOT-89 (Pb-free lead plating and halogen-free package)	A	±0.5%	1000 pcs / Tape & Reel
TL432KM3-B-T2-G		B	±1%	

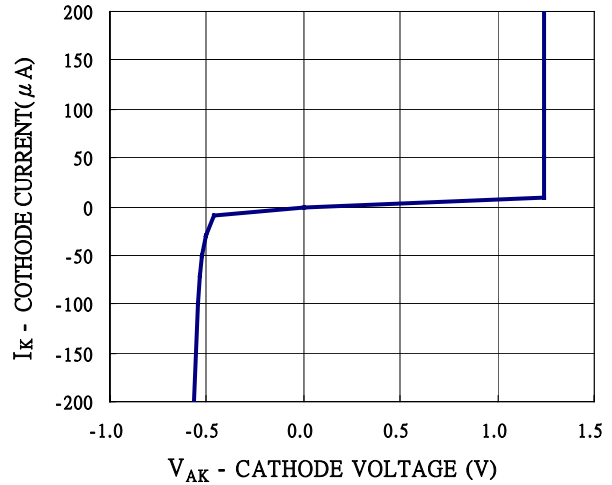


Typical Characteristics

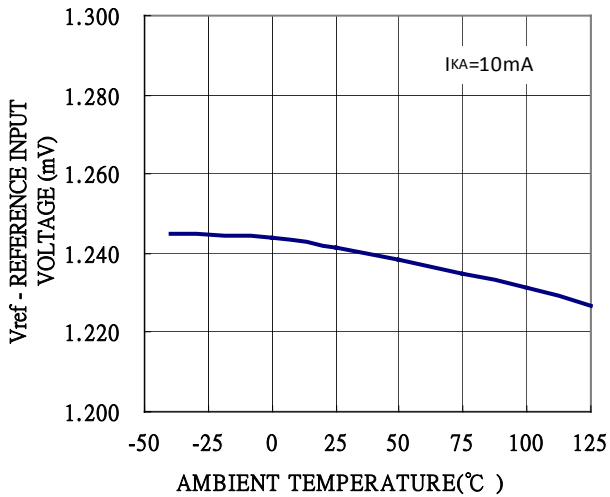
CATHODE CURRENT vs CATHODE VOLTAGE



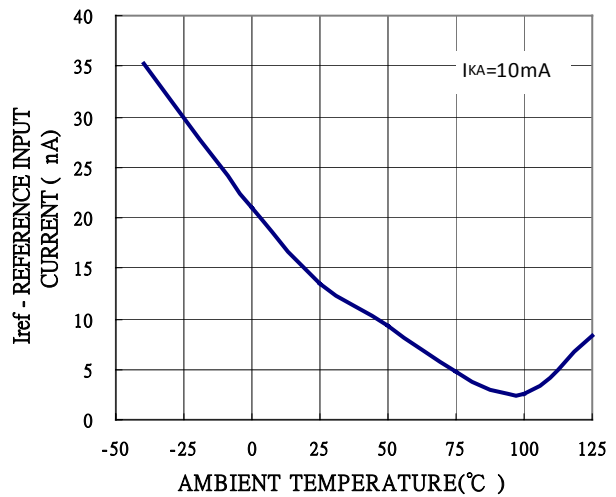
CATHODE CURRENT vs CATHODE VOLTAGE



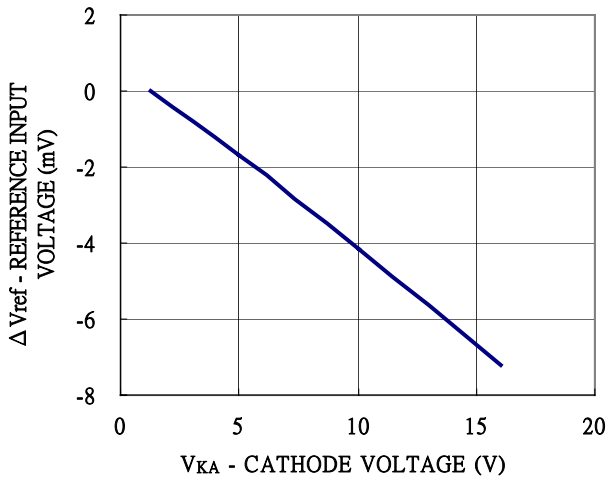
REFERENCE INPUT VOLTAGE vs AMBIENT TEMPERATURE



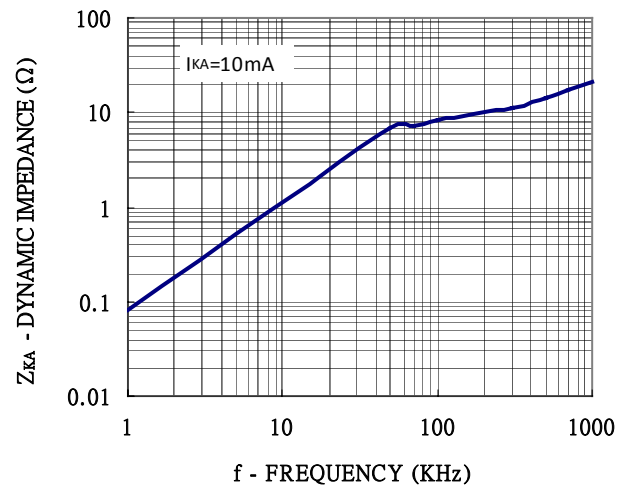
REFERENCE INPUT CURRENT vs AMBIENT TEMPERATURE



CATHODE VOLTAGE vs REFERENCE INPUT VOLTAGE

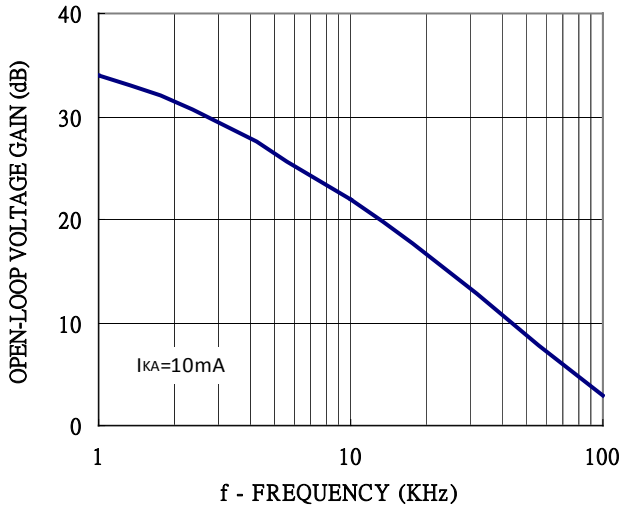


DYNAMIC IMPEDANCE vs FREQUENCY

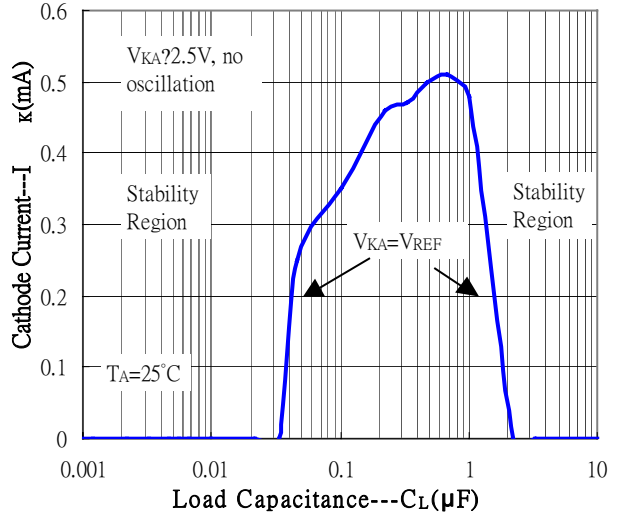


Typical Characteristics (Cont.)

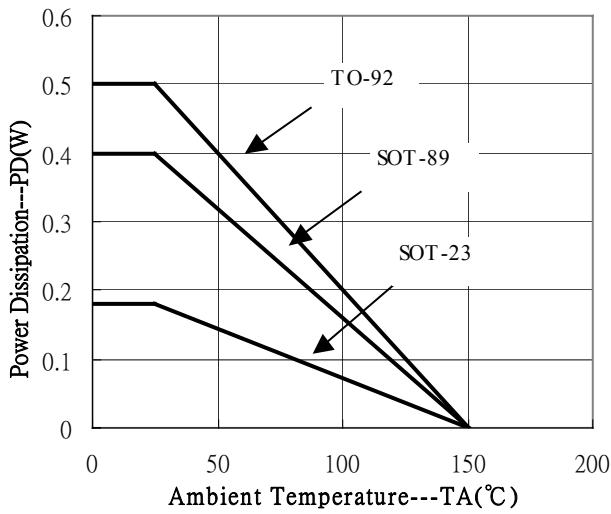
OPEN-LOOP VOLTAGE GAIN vs FREQUENCY



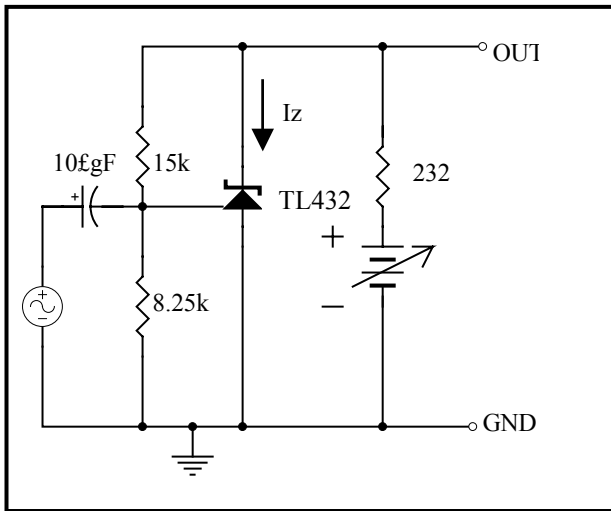
Stability Boundary Conditions



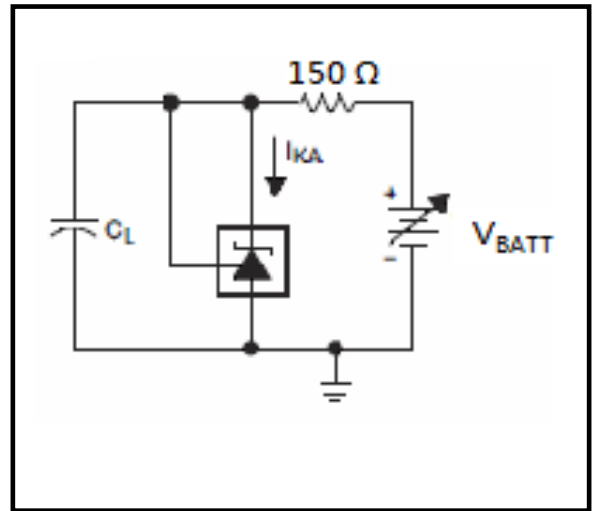
Power Derating Curves



Test Circuit-Small-Signal Gain and Phase



Test Circuit-Stability



Applications Information - Stability

Selection of load capacitance when using TL432K as a shunt regulator

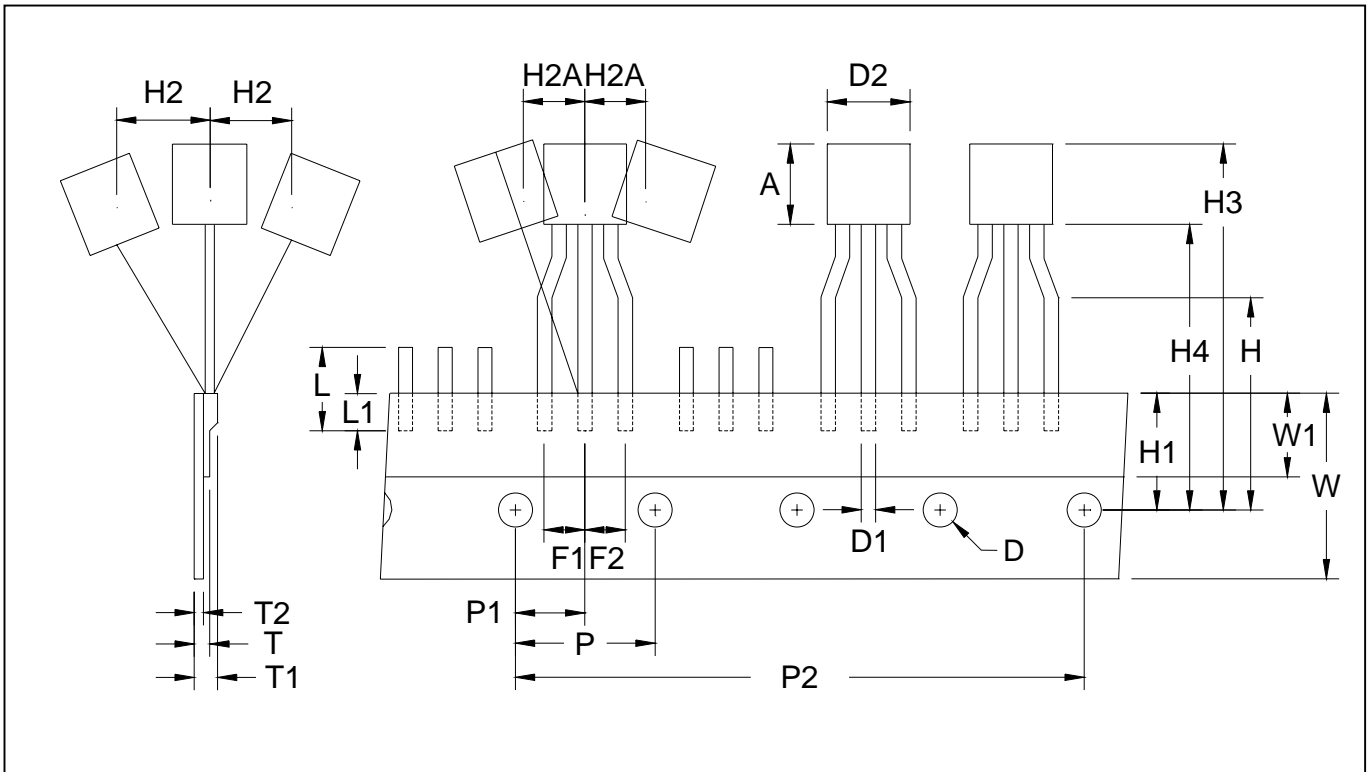
When the TL432K is used as a shunt regulator, two options for selection of C_L (see diagram on page 6) are recommended for optimal stability:

- 1) No load capacitance across the device, decouple at the load.
- 2) Large capacitance across the device, optimal decoupling at the load.

The reason for this is that TL432K exhibits instability with capacitances in the range of 47nF to 1µF (approx.) at light cathode currents(up to 0.5mA typical). The device is less stable the lower the cathode voltage has been set for. Therefore while the device will be perfectly stable operating at a cathode current of (say) 10mA with a 0.1µF capacitor across it, it will oscillate transiently during start-up as the cathode current passes through the instability region. Selecting a very low (or preferably, no) capacitance, or alternatively a high capacitance(such as 10µF) will avoid this issue altogether. Since the user will probably wish to have local decoupling at the load anyway, the most cost effective method is to use no capacitance at all directly across the device. PCB trace/via resistance and inductance prevent the local load decoupling from causing the oscillation during the transient start-up phase.

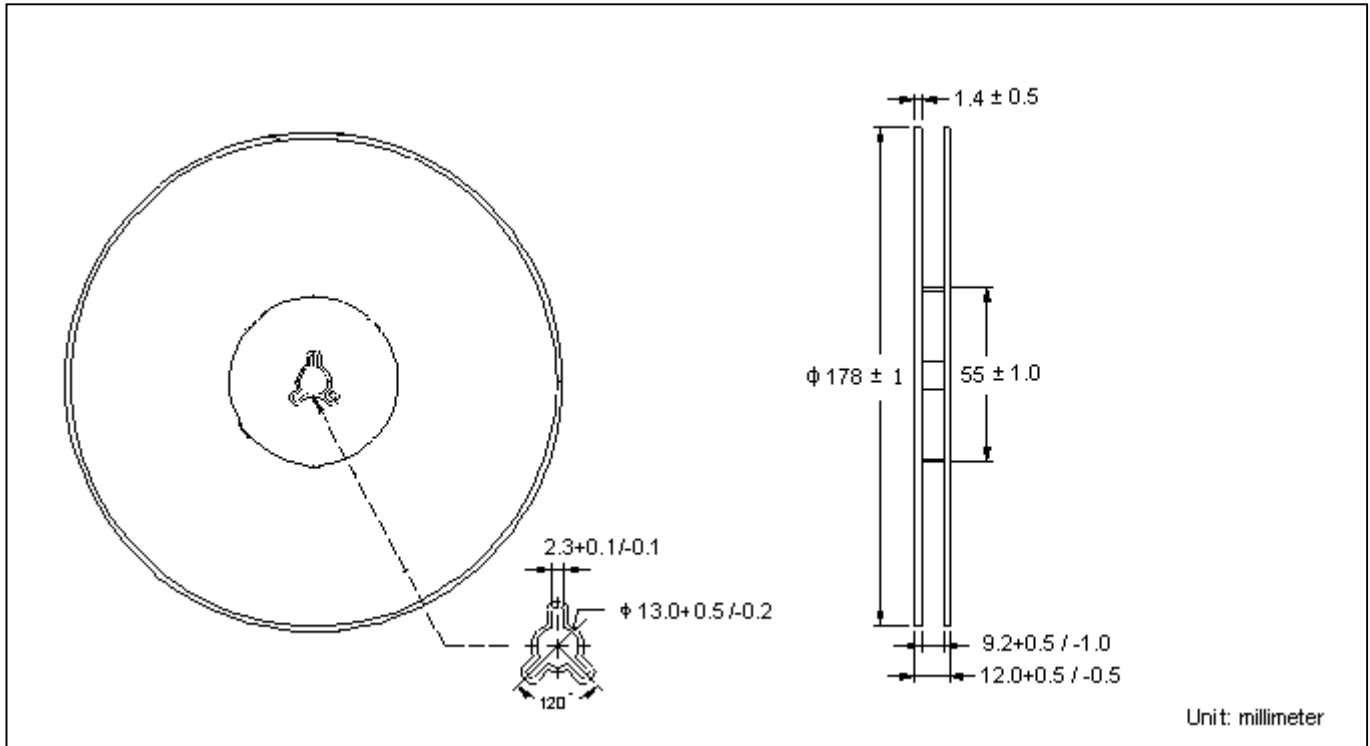
Note : if the TL432K is located right at the load, so the load decoupling capacitor is directly across it, then this capacitor will have to be $\leq 1\text{nF}$ or $\geq 10\mu\text{F}$.

TO-92 Taping Outline

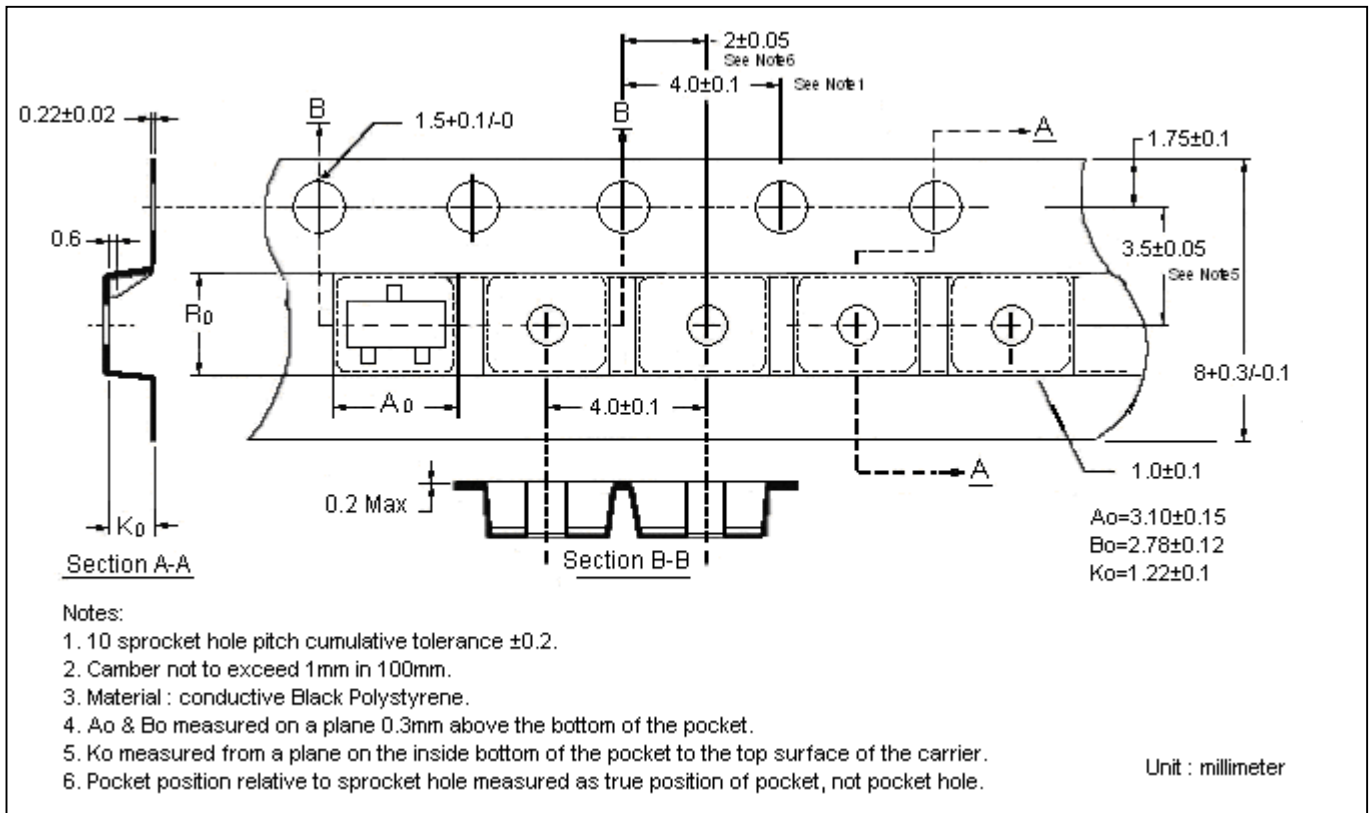


DIM	Item	Millimeters	
		Min.	Max.
A	Component body height	4.33	4.83
D	Tape Feed Diameter	3.80	4.20
D1	Lead Diameter	0.36	0.53
D2	Component Body Diameter	4.33	4.83
F1,F2	Component Lead Pitch	2.40	2.90
F1,F2	F1-F2	-	±0.3
H	Height Of Seating Plane	15.50	16.50
H1	Feed Hole Location	8.50	9.50
H2	Front To Rear Deflection	-	1
H2A	Deflection Left Or Right	-	1
H3	Component Height	-	27
H4	Feed Hole To Bottom Of Component	-	21
L	Lead Length After Component Removal	-	11
L1	Lead Wire Enclosure	2.50	-
P	Feed Hole Pitch	12.50	12.90
P1	Center Of Seating Plane Location	5.95	6.75
P2	4 Feed Hole Pitch	50.30	51.30
T	Over All Tape Thickness	-	0.55
T1	Total Taped Package Thickness	-	1.42
T2	Carrier Tape Thickness	0.36	0.68
W	Tape Width	17.50	19.00
W1	Adhesive Tape Width	5.00	7.00
-	20 pcs Pitch	253	255

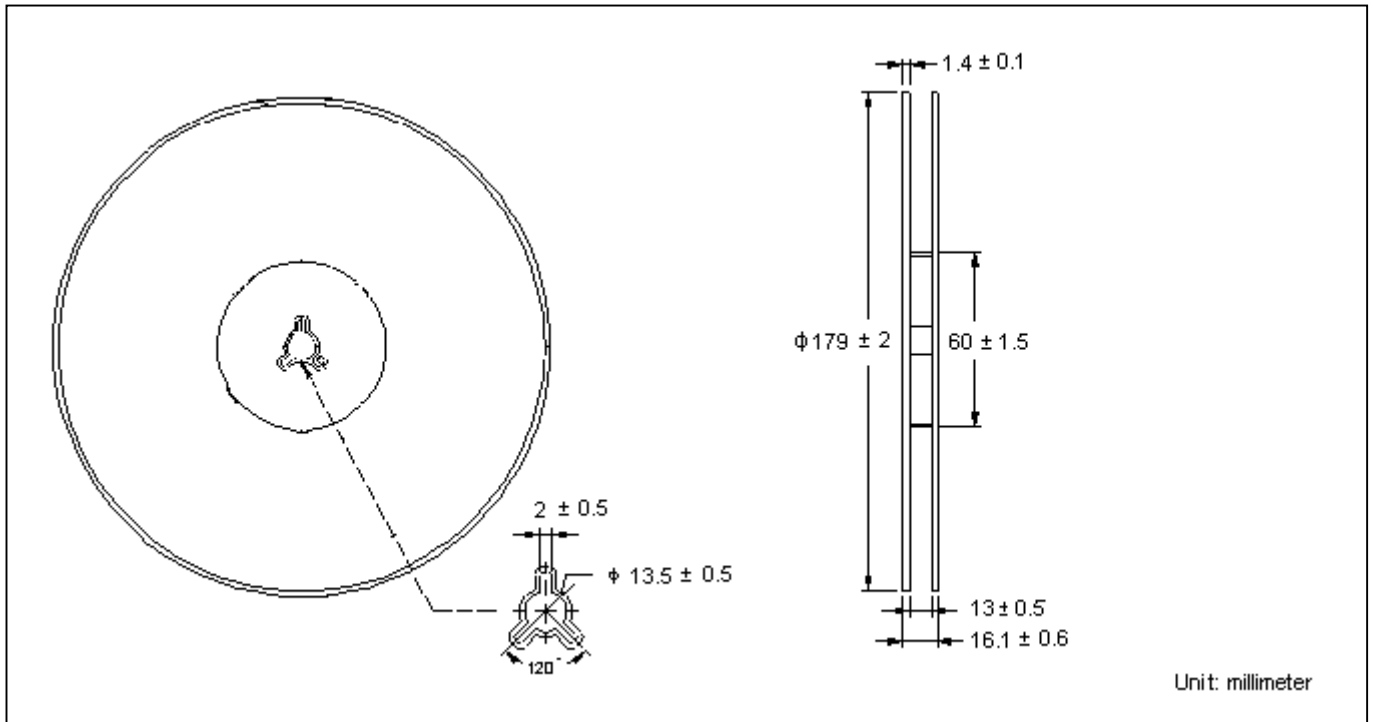
SOT-23 Reel Dimension



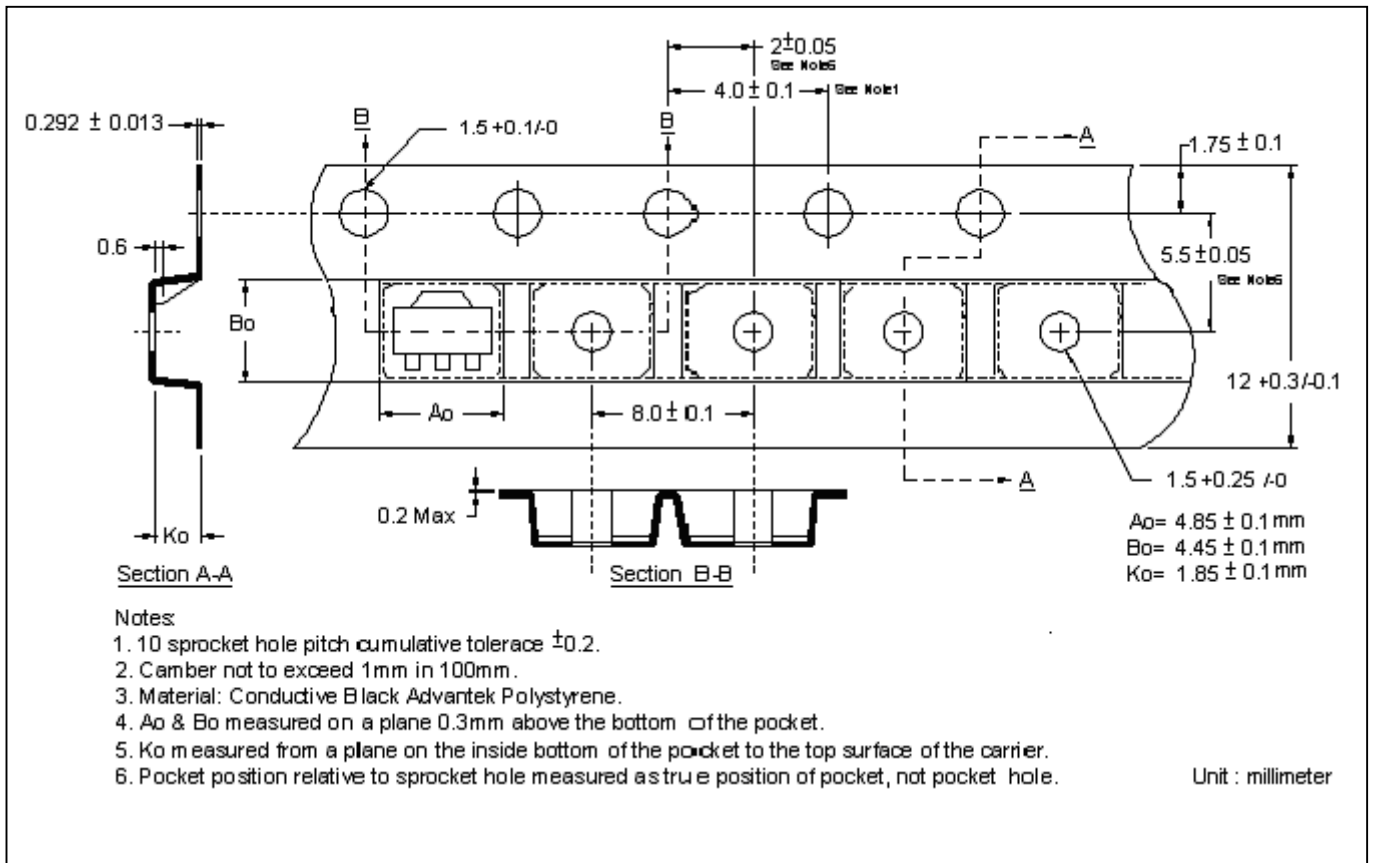
SOT-23 Carrier Tape Dimension



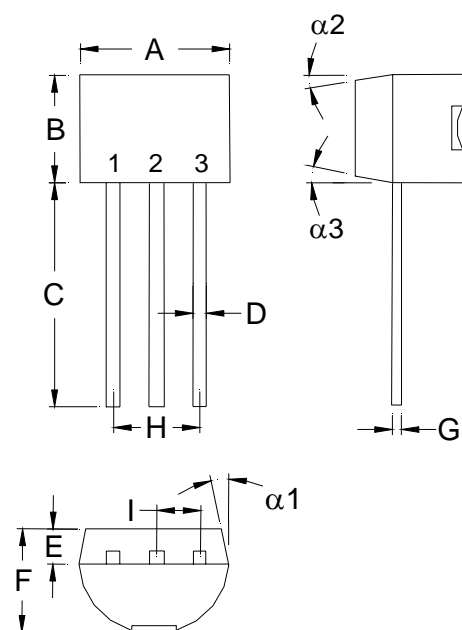
SOT-89 Reel Dimension



SOT-89 Carrier Tape Dimension



TO-92 Dimension



Marking:

TL
432K
Date Code → □ □

Style: Pin 1.Reference 2.Anode 3.Cathode

3-Lead TO-92 Plastic Package
 CYStek Package Code: A3

Date Code : Year Code (left character)+ Month Code (right character)
 Year Code : The last digit of Chriatian year
 Month Code : 1→Jan, 2→Feb, ..., 9→Sep, A→Oct, B→Nov, C→Dec

*: Typical

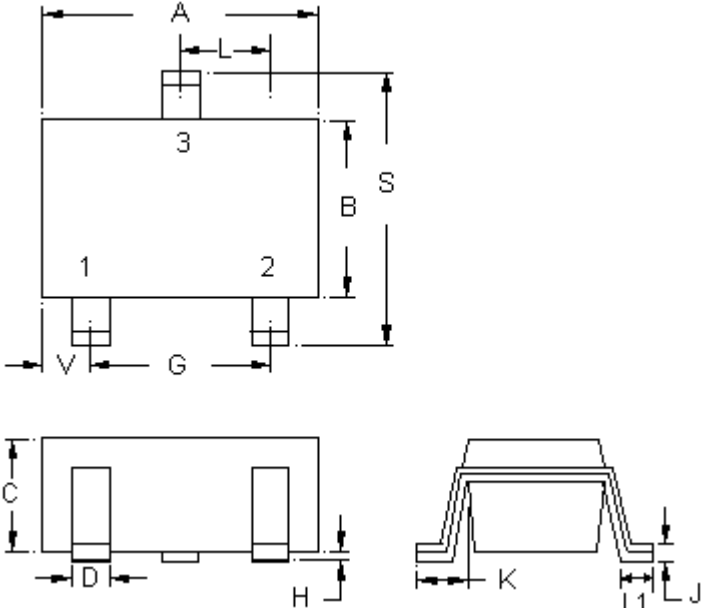
DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1704	0.1902	4.33	4.83	G	0.0142	0.0220	0.36	0.56
B	0.1704	0.1902	4.33	4.83	H	-	*0.1000	-	*2.54
C	0.5000	-	12.70	-	I	-	*0.0500	-	*1.27
D	0.0142	0.0220	0.36	0.56	$\alpha 1$	-	*5°	-	*5°
E	-	*0.0500	-	*1.27	$\alpha 2$	-	*2°	-	*2°
F	0.1323	0.1480	3.36	3.76	$\alpha 3$	-	*2°	-	*2°

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

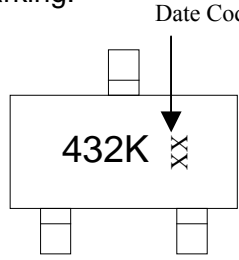
- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

SOT-23 Dimension



The diagram shows three views of the SOT-23 package: a top view with dimensions A, L, B, S, 1, 2, 3, V, and G; a side view with dimensions C, D, H, and J; and a perspective view with dimensions K, L1, and L2. The top view labels 1, 2, and 3 correspond to the Reference, Cathode, and Anode pins respectively.

Marking:



Date Code

3-Lead SOT-23 Plastic
 Surface Mounted Package
 CYStek Package Code: N3

Style: Pin 1.Reference 2.Cathode 3.Anode

Date Code : Year Code (bottom character)+ Month Code (top character)
 Year Code : The last digit of Christian year.
 Month Code : 1→Jan, 2→Feb, ..., 9→Sep, A→Oct, B→Nov, C→Dec

*: Typical

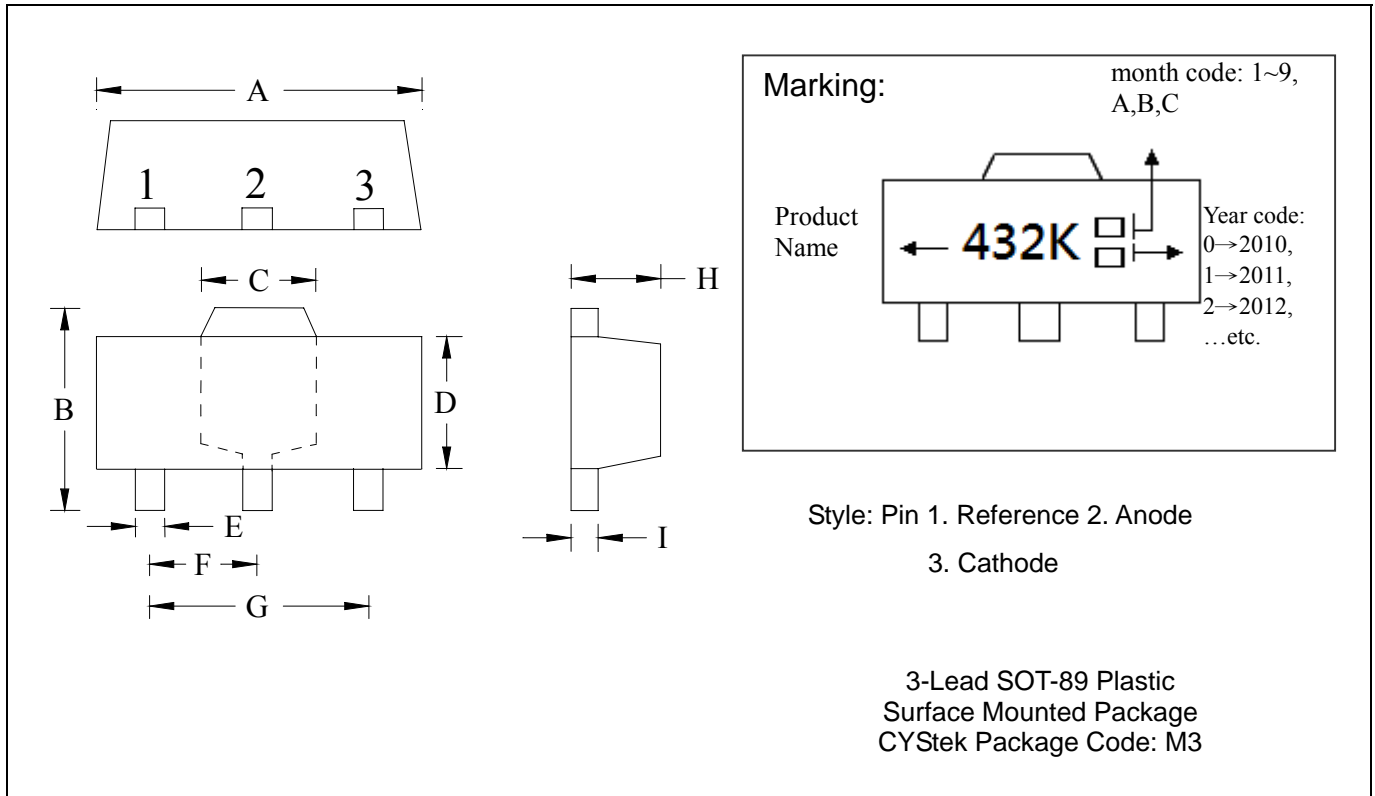
DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1102	0.1204	2.80	3.04	J	0.0032	0.0079	0.08	0.20
B	0.0472	0.0669	1.20	1.70	K	0.0118	0.0266	0.30	0.67
C	0.0335	0.0512	0.89	1.30	L	0.0335	0.0453	0.85	1.15
D	0.0118	0.0197	0.30	0.50	S	0.0830	0.1161	2.10	2.95
G	0.0669	0.0910	1.70	2.30	V	0.0098	0.0256	0.25	0.65
H	0.0000	0.0040	0.00	0.10	L1	0.0118	0.0197	0.30	0.50

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYCtek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

SOT-89 Dimension



*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1732	0.1811	4.40	4.60	F	0.0583	0.0598	1.48	1.527
B	0.1594	0.1673	4.05	4.25	G	0.1165	0.1197	2.96	3.04
C	0.0591	0.0663	1.50	1.70	H	0.0551	0.0630	1.40	1.60
D	0.0945	0.1024	2.40	2.60	I	0.0138	0.0161	0.35	0.41
E	0.01417	0.0201	0.36	0.51					

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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