

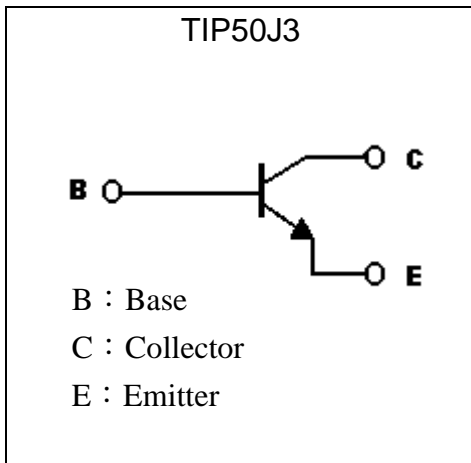
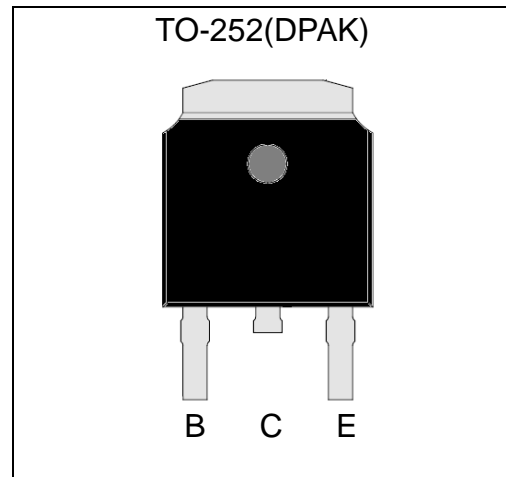
High Voltage NPN Power Transistor

TIP50J3

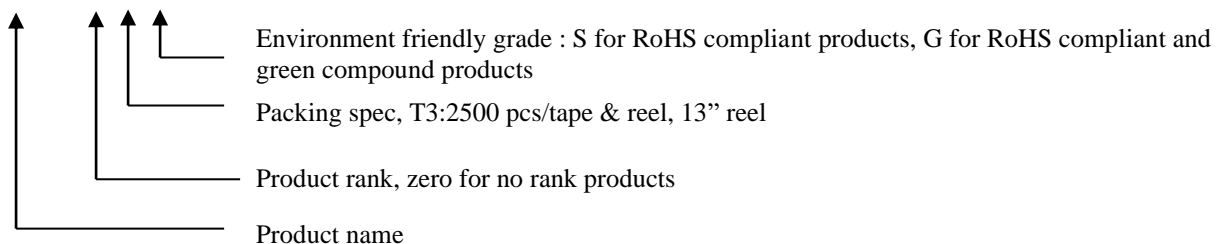
BV_{CEO}	400V
I_C	1.5A
R_{CESAT}	500m Ω (max.)

Features

- High breakdown voltage, $V_{CEO}=400V$ (min.)
- High collector current, $I_{C(max)}=1.5A$ (DC)
- Pb-free lead plating and halogen-free package

Symbol

Outline

Ordering Information

Device	Package	Shipping
TIP50J3-0-T3-G	TO-252 (Pb-free lead plating and halogen-free package)	2500 pcs / Tape & Reel





Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V _{CBO}	700	V
Collector-Emitter Voltage	V _{CEO}	400	
Emitter-Base Voltage	V _{EBO}	9	
Collector Current (DC)	I _C	1.5	A
Collector Current (Pulse)	I _{CM}	3 (Note 1)	
Base Current (DC)	I _B	0.5	
Base Current (Pulse)	I _{BM}	1.5 (Note 1)	
Power Dissipation @ T _A =25°C	P _D	1.56 (Note 2)	W
Power Dissipation @ T _C =25°C		15	
Thermal Resistance, Junction to Ambient	R _{θJA}	80 (Note 2)	°C/W
Thermal Resistance, Junction to Case	R _{θJC}	8.33	
Operating Junction Temperature Range	T _j	-55~+150	°C
Storage Temperature Range	T _{stg}	-65~+150	°C

Note : 1. Pulse test, P_w ≤ 5ms.

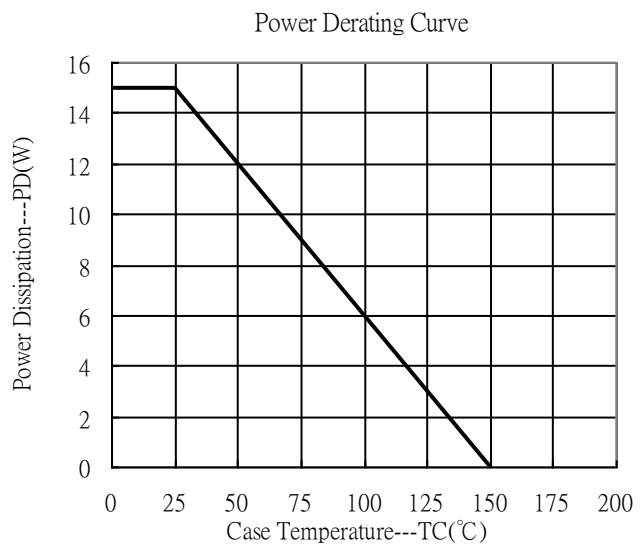
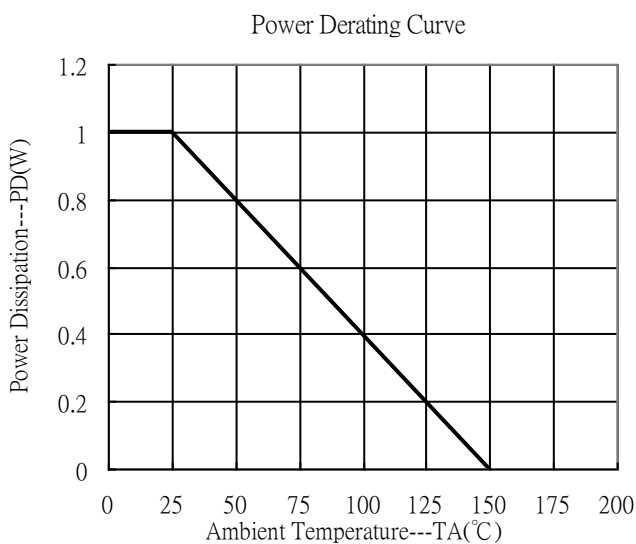
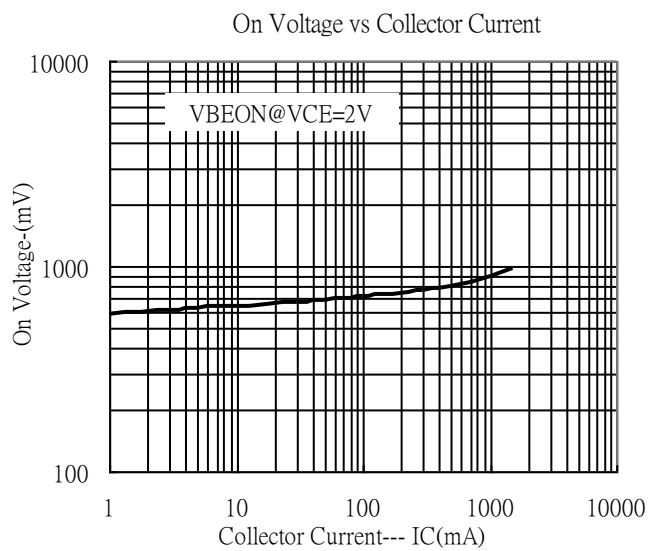
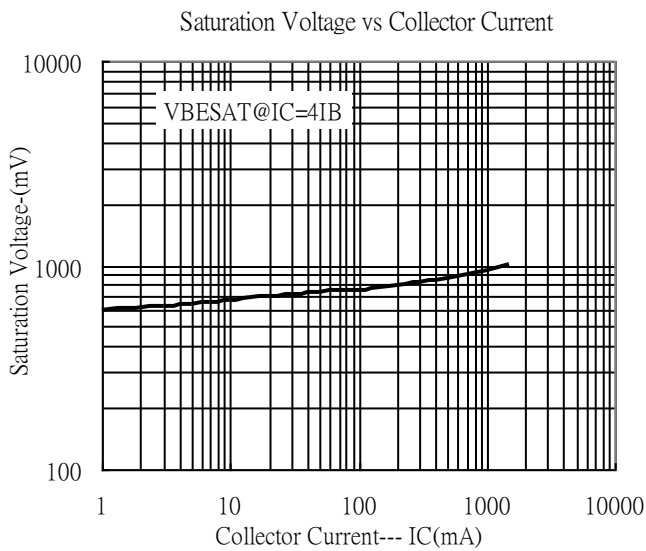
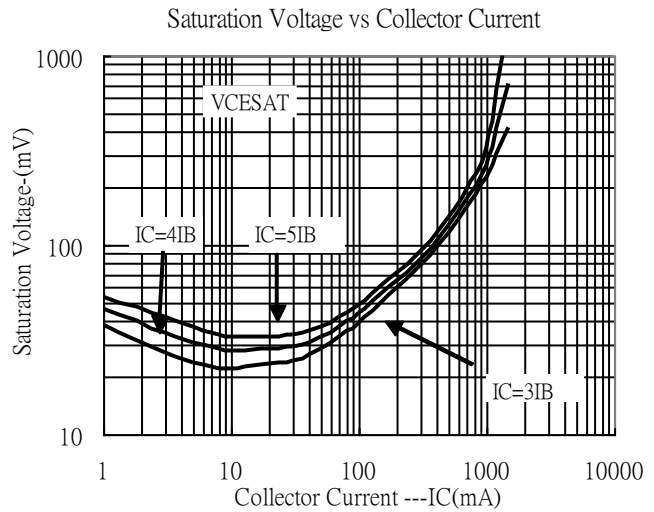
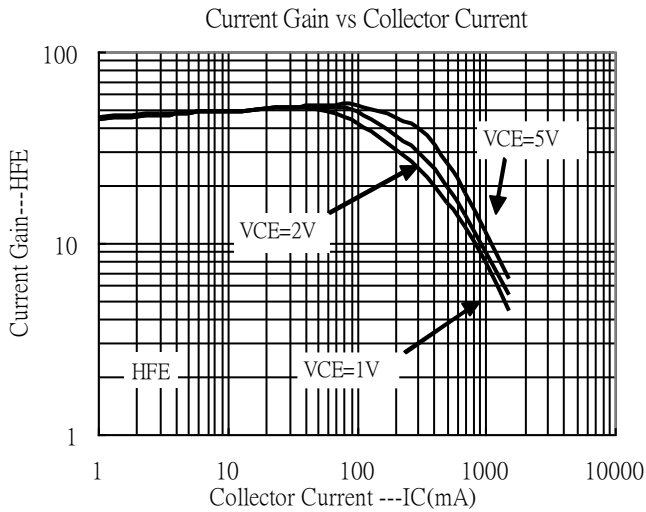
2. When the device is mounted on a FR-4 PCB with minimum pad size recommended.

Characteristics (Ta=25°C)

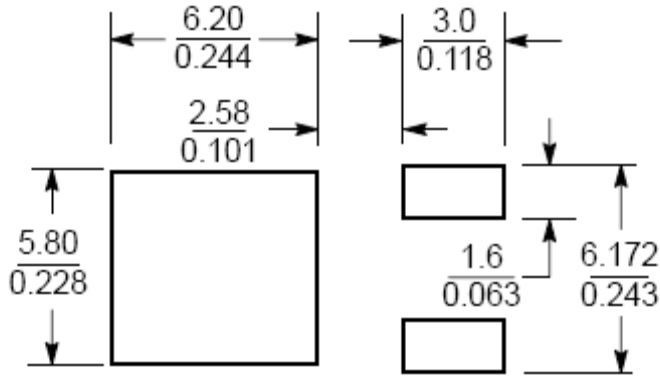
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CBO}	700	-	-	V	I _C =100μA
BV _{CEO}	400	-	-	V	I _C =10mA
BV _{EBO}	9	-	-	V	I _E =100μA
I _{CBO}	-	-	10	μA	V _{CB} =700V, I _E =0
I _{EBO}	-	-	10	μA	V _{EB} =9V, I _C =0
*V _{CE(SAT)}	-	-	0.3	V	I _C =500mA, I _B =100mA
*V _{CE(SAT)}	-	-	0.5	V	I _C =1 A, I _B =200mA
*V _{CE(SAT)}	-	-	0.8	V	I _C =1.5 A, I _B =500mA
*R _{CE(SAT)}	-	-	0.5	Ω	I _C =1 A, I _B =200mA
*V _{BE(SAT)}	-	-	1.2	V	I _C =1 A, I _B =200mA
*V _{BE(ON)}	-	-	1.2	V	V _{CE} =10V, I _C =1A
*h _{FE 1}	50	-	100	-	V _{CE} =10V, I _C =300mA
*h _{FE 2}	10	-	-	-	V _{CE} =10V, I _C =1A
f _T	10	-	-	MHz	V _{CE} =10V, I _C =100mA, f=100MHz
C _{ob}	-	21	-	pF	V _{CB} =10V, I _E =0A, f=1MHz
t _{on}	-	1.1	-	μs	V _{CC} =125V, R _L =125Ω, I _C =1A, I _{B1} =-I _{B2} =0.2A
t _{stg}	-	-	4		
t _f	-	-	0.7		

*Pulse Test: Pulse Width ≤380μs, Duty Cycle≤2%

Typical Characteristics

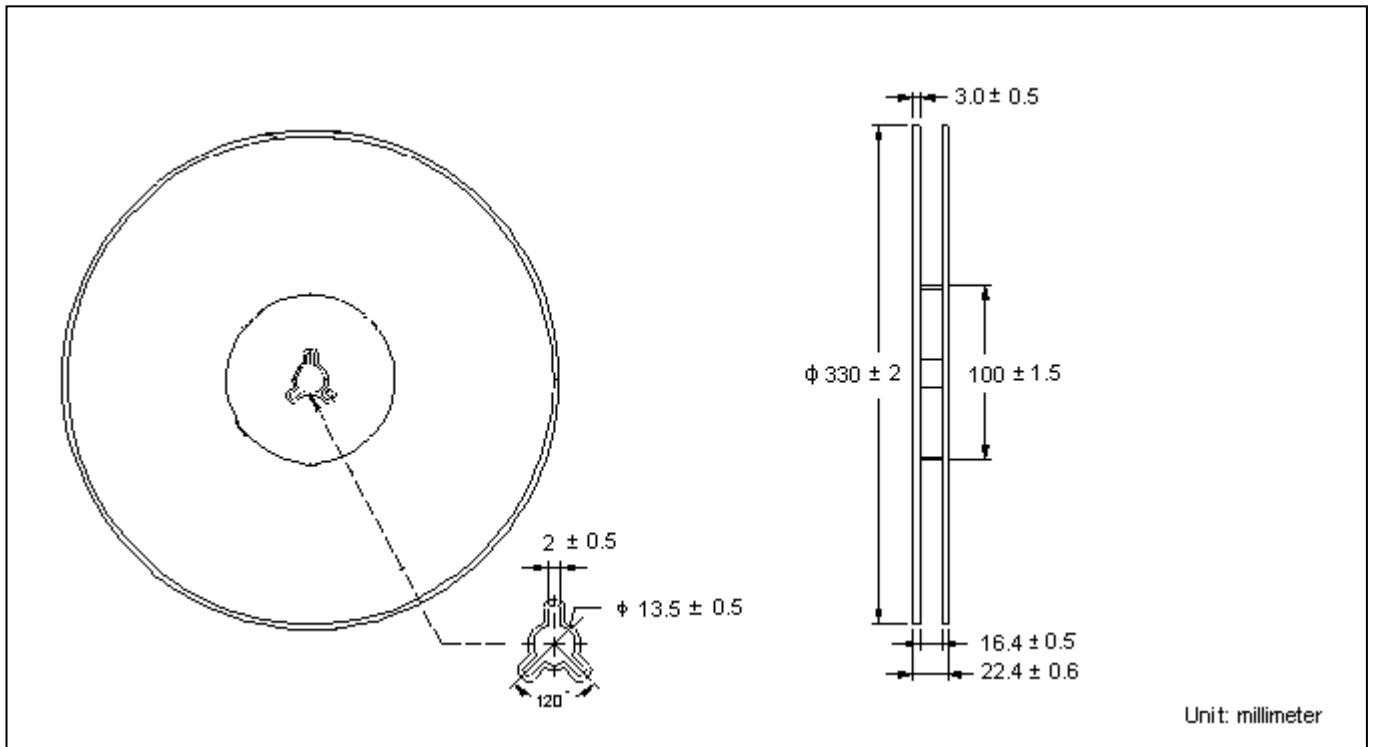


Recommended soldering footprint

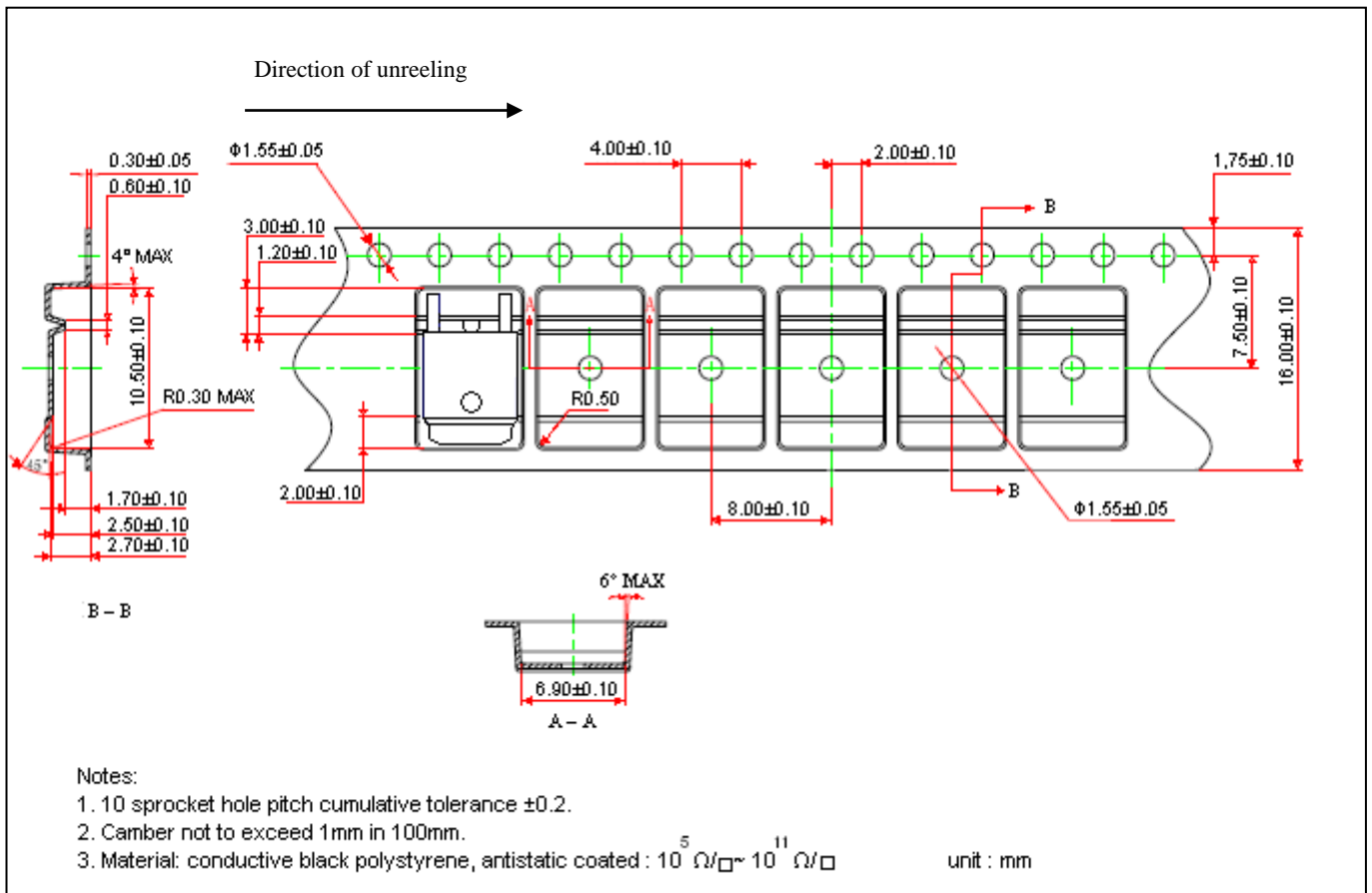


Unit ($\frac{\text{mm}}{\text{inch}}$)

Reel Dimension



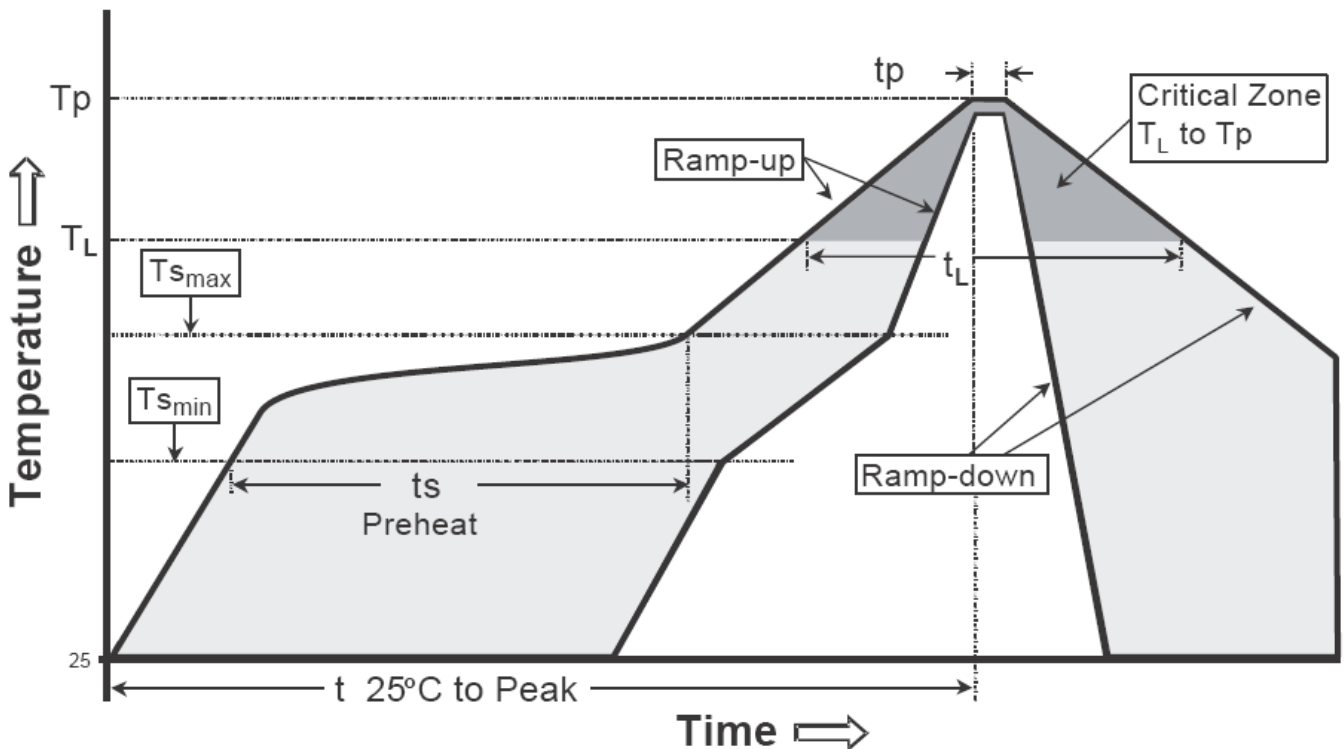
Carrier Tape Dimension



Recommended wave soldering condition

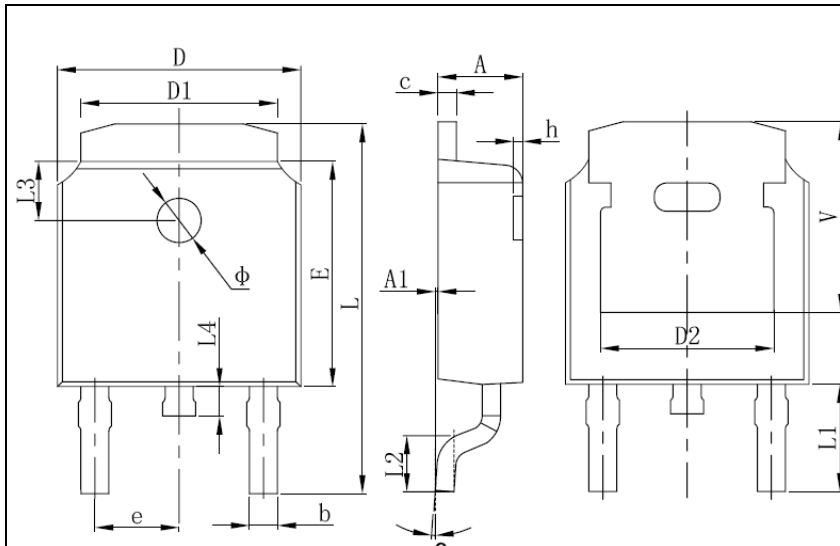
Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

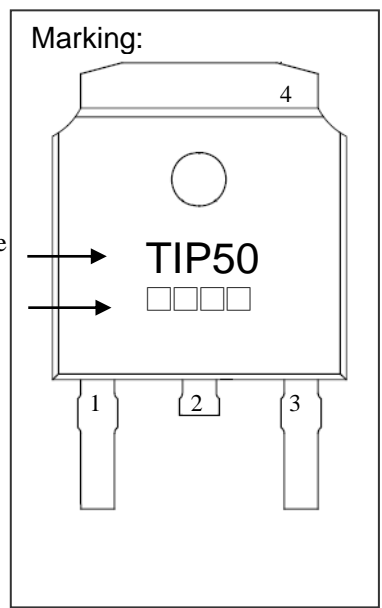
TO-252 Dimension



3-Lead TO-252 Plastic Surface Mount Package
 CYStek Package Code: J3

Date Code(counting from left to right) :
 1st code: year code, the last digit of Christian year
 2nd code : month code, Jan→A, Feb→B, Mar→C,
 Apr→D, May→E, Jun→F, Jul→G, Aug→H,
 Sep→J, Oct→K, Nov→L, Dec→M
 3rd and 4th codes : production serial number, 01~99

Marking:



Device Code →
 Date Code →

Style: Pin 1.Base 2.Collector 3.Emitter
 4.Collector

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.087	0.094	2.200	2.400	L	0.382	0.406	9.712	10.312
A1	0.000	0.005	0.000	0.127	L1	0.114	REF	2.900	REF
b	0.025	0.030	0.635	0.770	L2	0.055	0.067	1.400	1.700
c	0.018	0.023	0.460	0.580	L3	0.063	REF	1.600	REF
D	0.256	0.264	6.500	6.700	L4	0.024	0.039	0.600	1.000
D1	0.201	0.215	5.100	5.460	Φ	0.043	0.051	1.100	1.300
D2	0.190	REF	4.830	REF	θ	0°	8°	0°	8°
E	0.236	0.244	6.000	6.200	h	0.000	0.012	0.000	0.300
e	0.086	0.094	2.186	2.386	V	0.207	REF	5.250	REF

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead : Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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