

N-Channel Enhancement Mode Power MOSFET

MTN4N65BF3

BV_{DSS}	650V
I_D @ V_{GS}=10V, T_C=25°C	4A
I_D @ V_{GS}=10V, T_C=100°C	2.5A
R_{DS(ON)}@ V_{GS}=10V, I_D=2A	2Ω (typ)

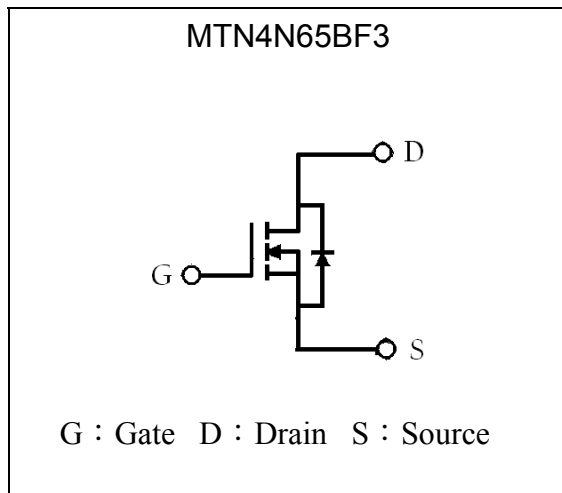
Features

- Low On Resistance
- Simple Drive Requirement
- Fast Switching Characteristic
- Pb-free lead plating and RoHS compliant package

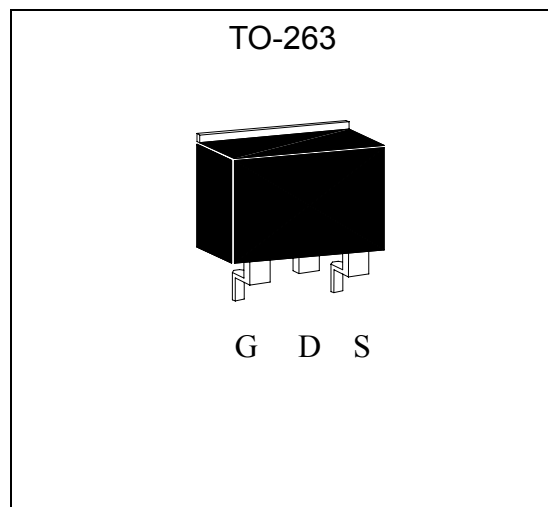
Applications

- Adapter
- Switching Mode Power Supply

Symbol

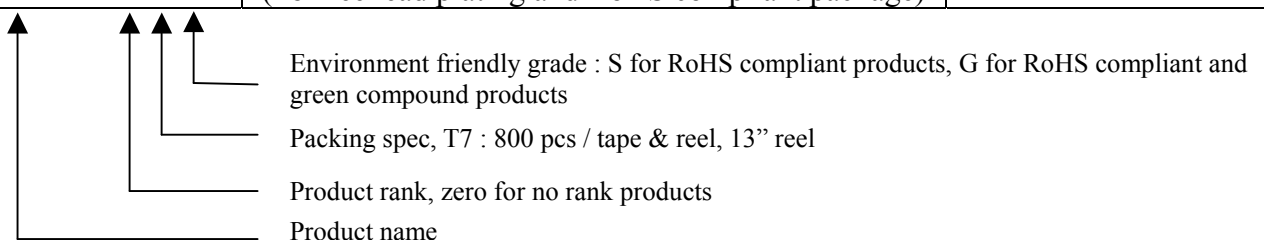


Outline



Ordering Information

Device	Package	Shipping
MTN4N65BF3-0-T7-X	TO-263 (Pb-free lead plating and RoHS compliant package)	800 pcs / Tape & Reel



**Absolute Maximum Ratings** ($T_C=25^{\circ}\text{C}$)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current @ $T_C=25^{\circ}\text{C}$, $V_{GS}=10\text{V}$	I_D	4*	A
Continuous Drain Current @ $T_C=100^{\circ}\text{C}$, $V_{GS}=10\text{V}$		2.5*	
Pulsed Drain Current @ $V_{GS}=10\text{V}$ (Note 1)	I_{DM}	16*	
Single Pulse Avalanche Energy (Note 2)	E_{AS}	64	mJ
Single Pulse Avalanche Current (Note 2)	I_{AS}	4	A
Repetitive Avalanche Energy (Note 1)	E_{AR}	3.4	mJ
Maximum Temperature for Soldering @ Lead at 0.125 in(0.318mm) from case for 10 seconds	T_L	300	$^{\circ}\text{C}$
Total Power Dissipation ($T_C=25^{\circ}\text{C}$)	P_D	100	W
Linear Derating Factor		0.8	W/ $^{\circ}\text{C}$
Operating Junction and Storage Temperature	T_j, T_{stg}	-55~+150	$^{\circ}\text{C}$

*Drain current limited by maximum junction temperature

Note : 1. Pulse width limited by maximum junction temperature.

2. $I_{AS}=4\text{A}$, $V_{DD}=50\text{V}$, $L=8\text{mH}$, $R_G=25\Omega$, starting $T_J=+25^{\circ}\text{C}$. 100% tested by conditions of $L=8\text{mH}$, $V_{GS}=10\text{V}$, $I_{AS}=2\text{A}$, $V_{DD}=50\text{V}$.

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{\theta JC}$	1.25	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-ambient, max	$R_{\theta JA}$	62.5	



Characteristics (Tj=25°C, unless otherwise specified)

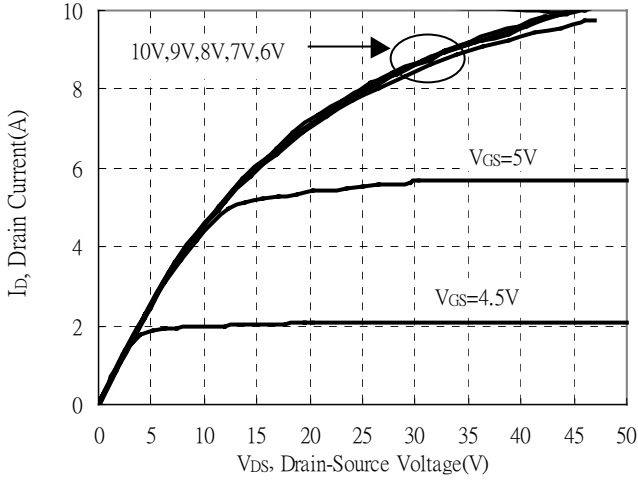
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	650	-	-	V	V _{GS} =0V, I _D =250μA, T _j =25°C
ΔBV _{DSS} /ΔT _j	-	0.6	-	V/°C	Reference to 25°C, I _D =250μA
V _{GS(th)}	2.0	-	4.0	V	V _{DS} = V _{GS} , I _D =250μA
*G _{FS}	-	5.3	-	S	V _{DS} =15V, I _D =2A
I _{GSS}	-	-	±100	nA	V _{GS} =±30V
I _{DSS}	-	-	1	μA	V _{DS} =650V, V _{GS} =0V
	-	-	10		V _{DS} =520V, V _{GS} =0V, T _C =125°C
*R _{DS(ON)}	-	2.0	2.6	Ω	V _{GS} =10V, I _D =2A
Dynamic					
*Q _g	-	18.8	-	nC	I _D =4A, V _{DD} =520V, V _{GS} =10V
*Q _{gs}	-	3.3	-		
*Q _{gd}	-	8.7	-		
*t _{d(ON)}	-	10.6	-	ns	V _{DD} =325V, I _D =4A, V _{GS} =10V, R _G =25Ω
*t _r	-	10.2	-		
*t _{d(OFF)}	-	40	-		
*t _f	-	32.8	-		
C _{iss}	-	575	-	pF	V _{GS} =0V, V _{DS} =25V, f=1MHz
C _{oss}	-	56	-		
C _{rss}	-	32	-		
Source-Drain Diode					
*V _{SD}	-	-	1.5	V	I _S =2A, V _{GS} =0V
*I _S	-	-	4	A	
*I _{SM}	-	-	16		
*t _{rr}	-	330	-	ns	V _{GS} =0V, I _F =4A, dI _F /dt=100A/μs
*Q _{rr}	-	1.27	-	μC	

*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

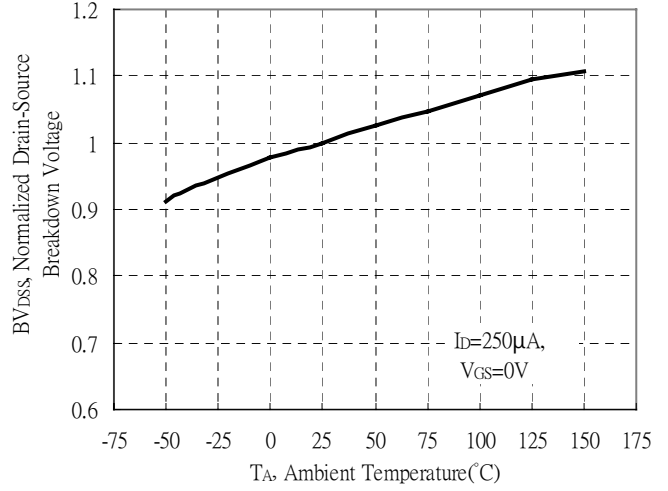


Typical Characteristics

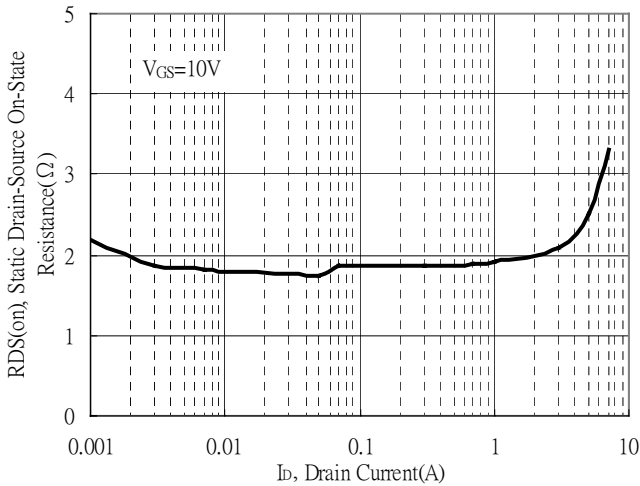
Typical Output Characteristics



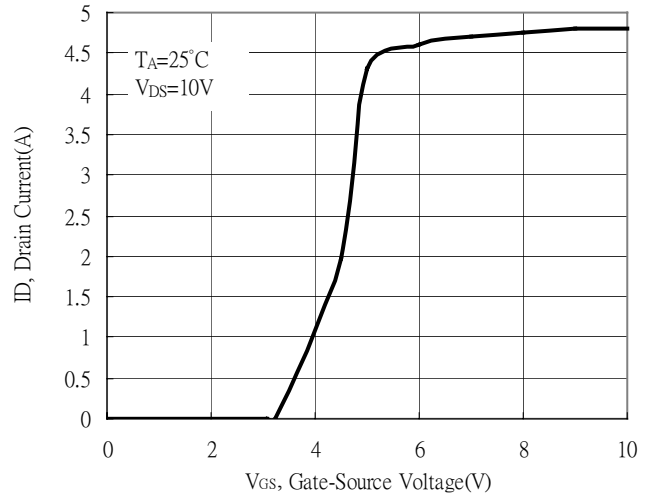
Brekdown Voltage vs Ambient Temperature



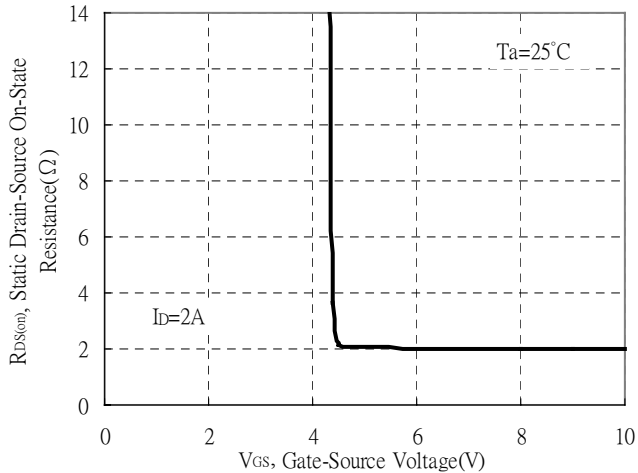
Static Drain-Source On-State resistance vs Drain Current



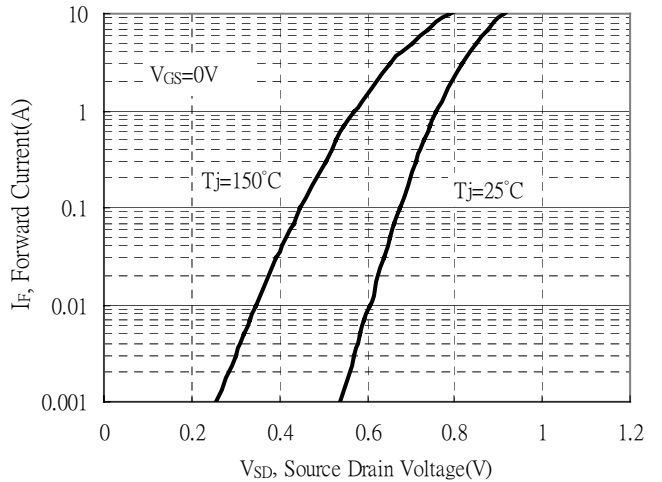
Drain Current vs Gate-Source Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

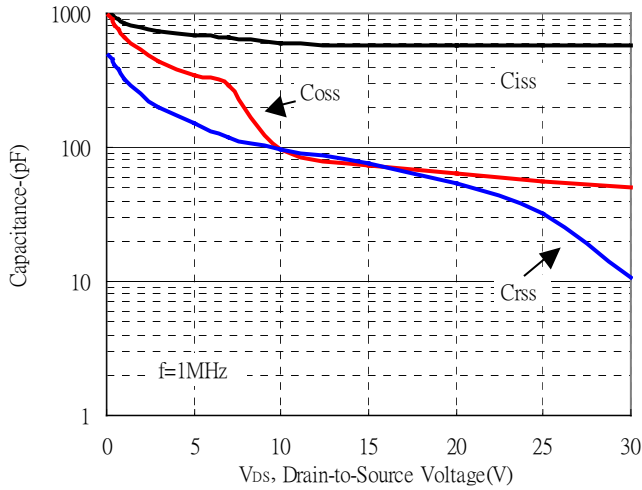


Forward Drain Current vs Source-Drain Voltage

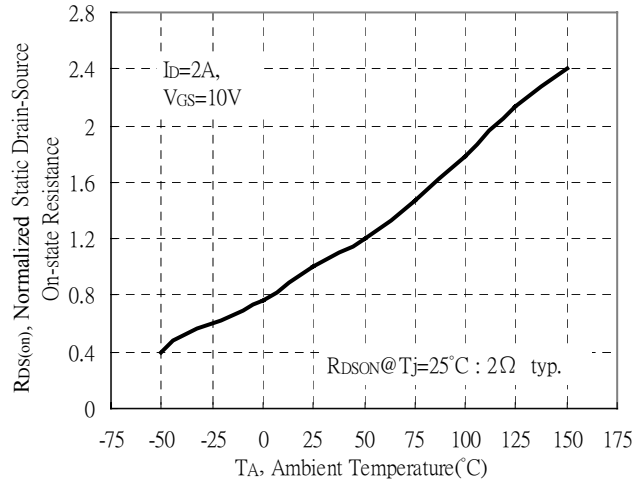


Typical Characteristics(Cont.)

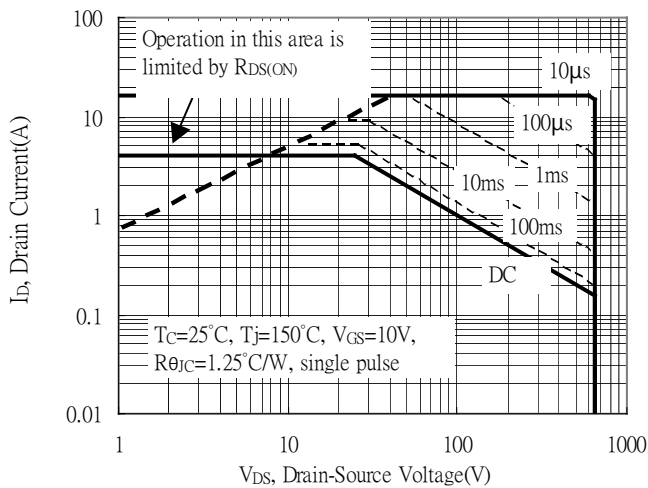
Capacitance vs Reverse Voltage



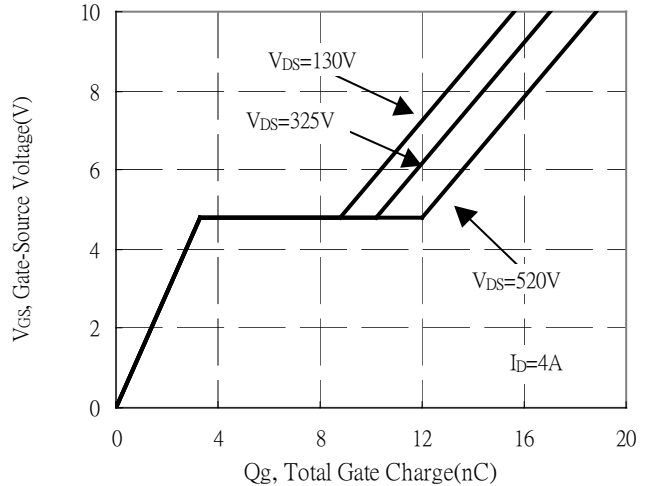
Static Drain-Source On-resistance vs Ambient Temperature



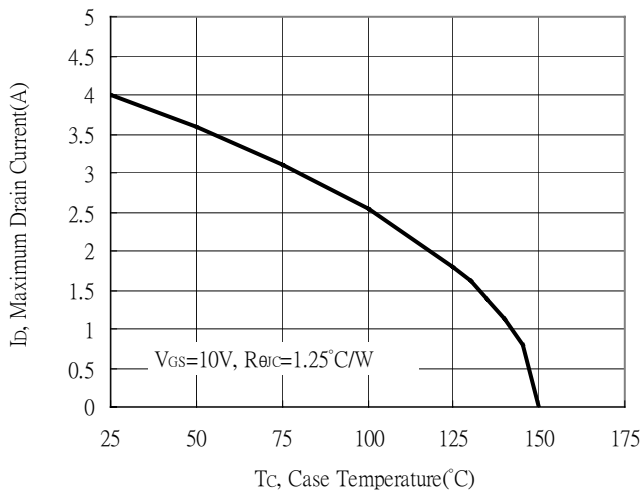
Maximum Safe Operating Area



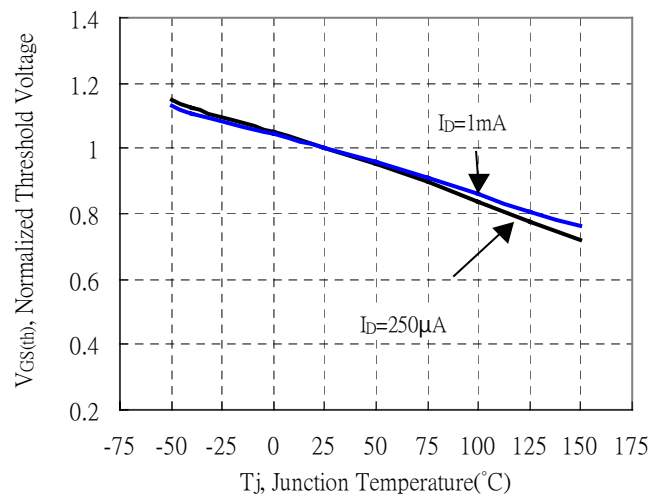
Gate Charge Characteristics



Maximum Drain Current vs Case Temperature



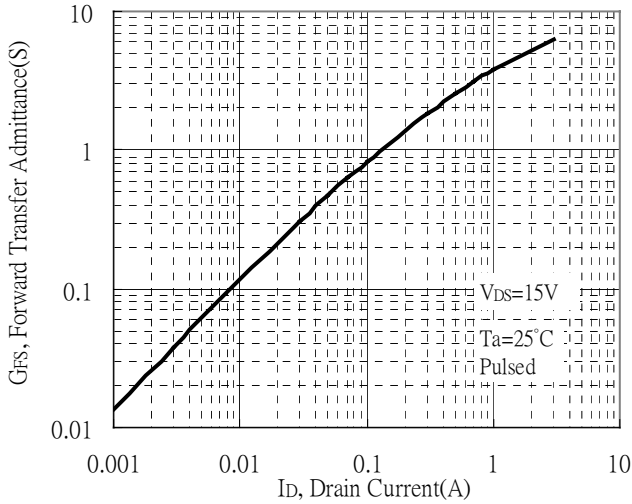
Threshold Voltage vs Junction Temperature



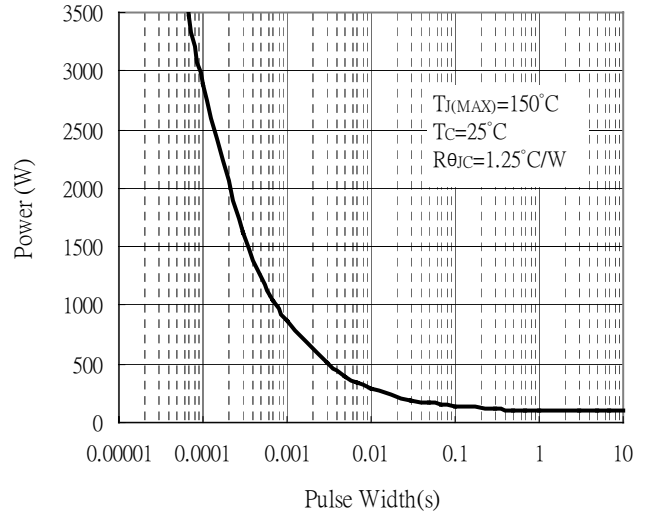


Typical Characteristics(Cont.)

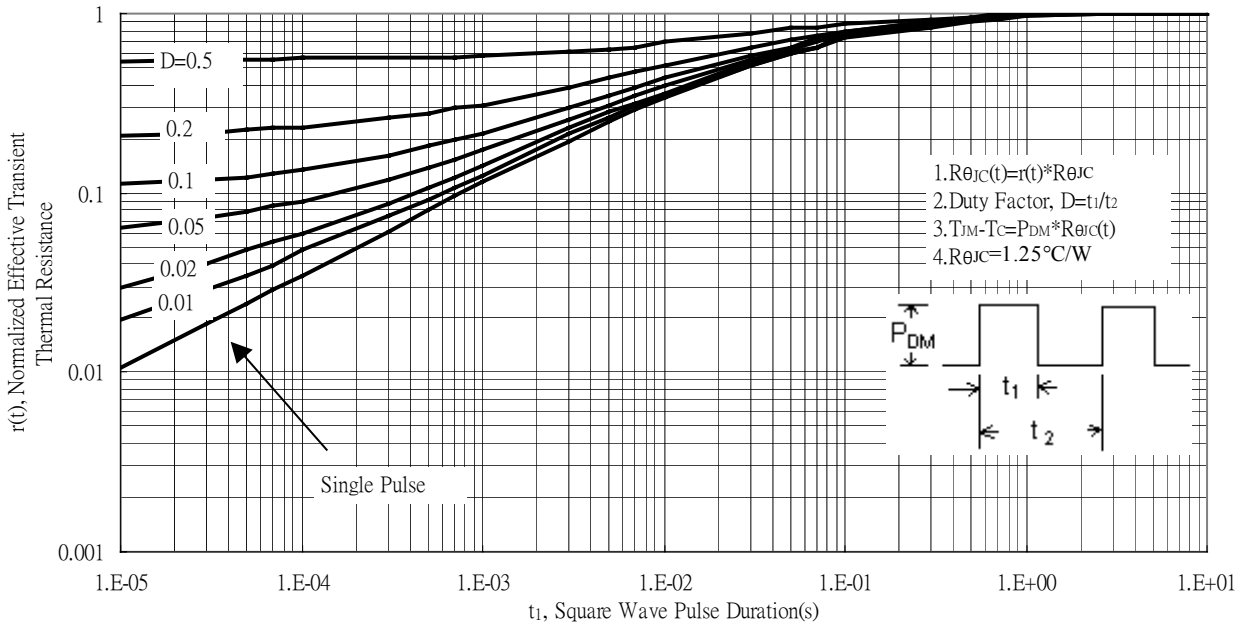
Forward Transfer Admittance vs Drain Current



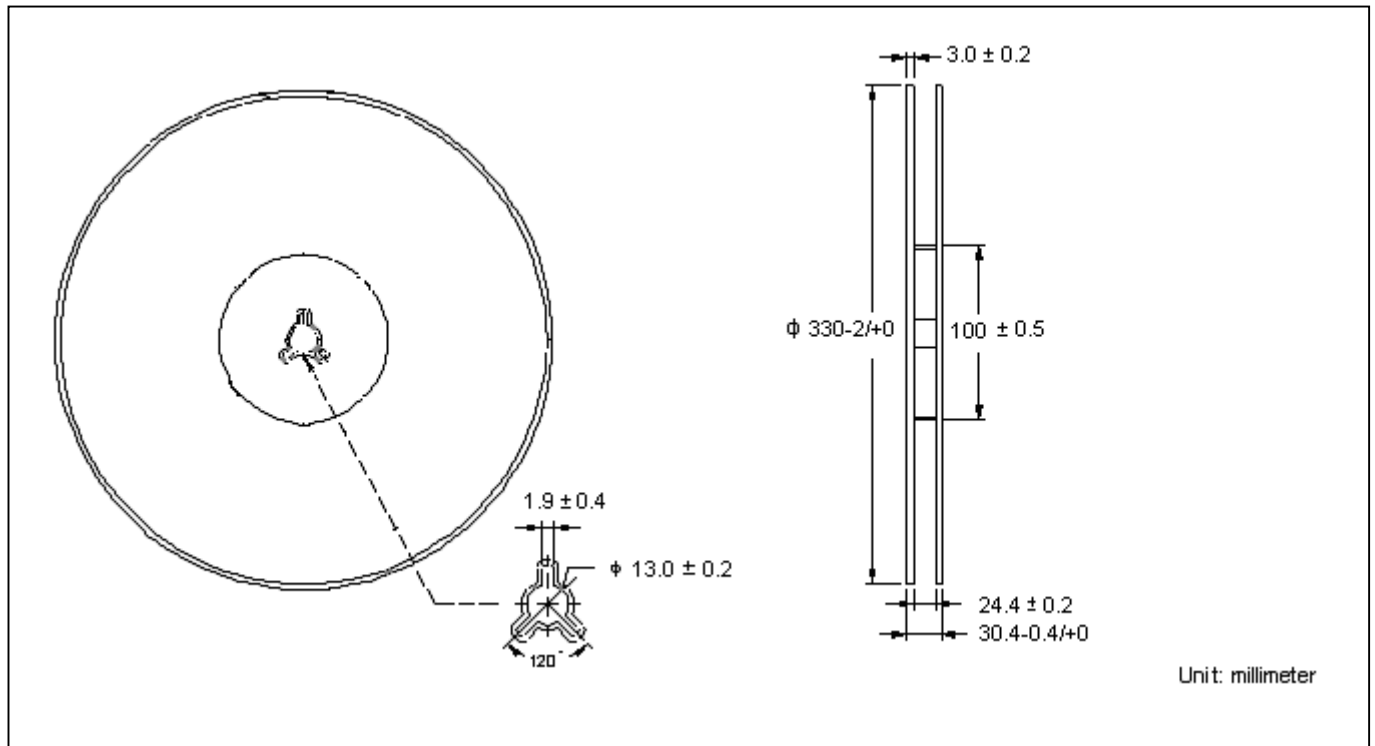
Single Pulse Power Rating, Junction to Case



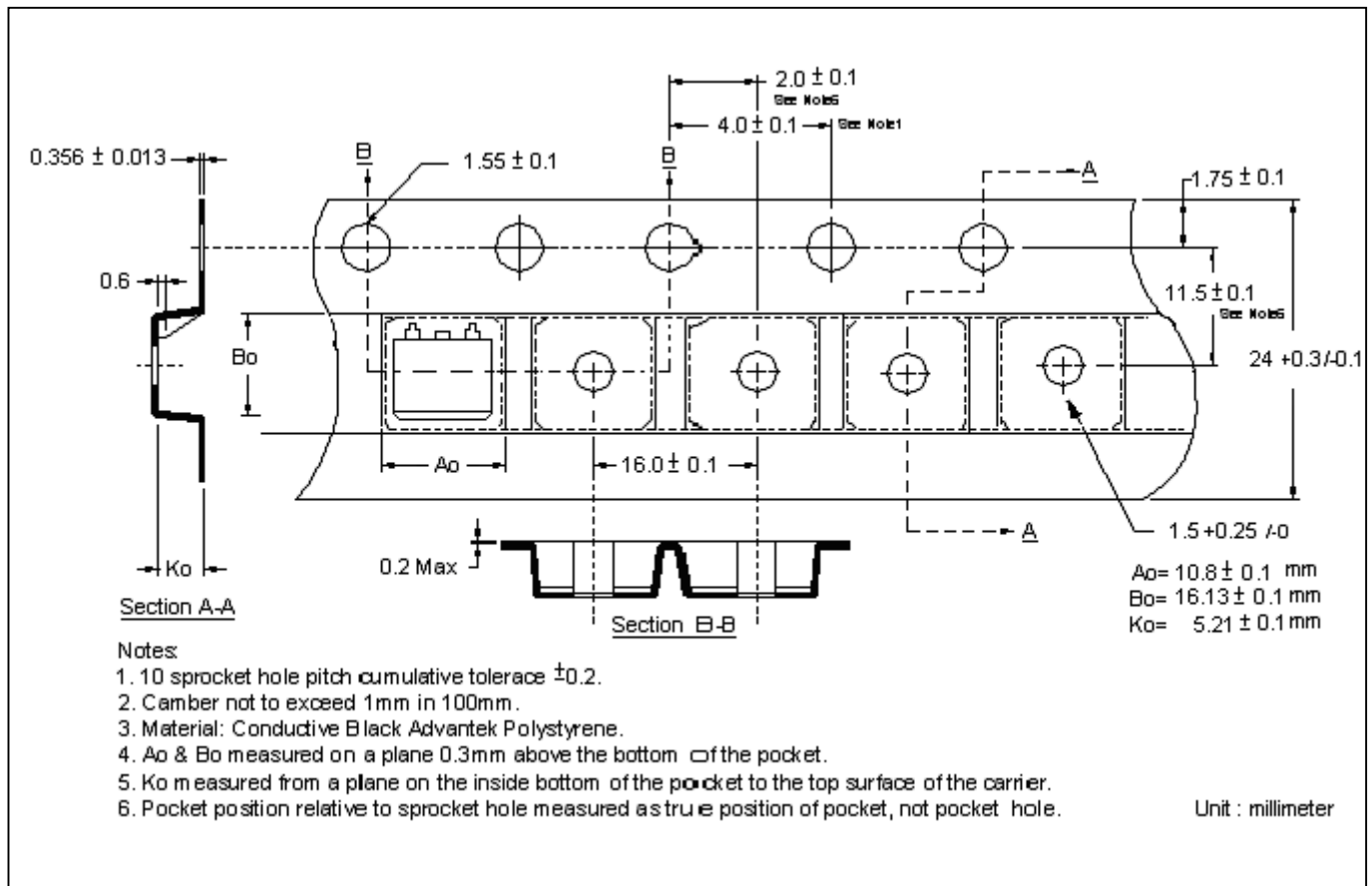
Transient Thermal Response Curves



Reel Dimension



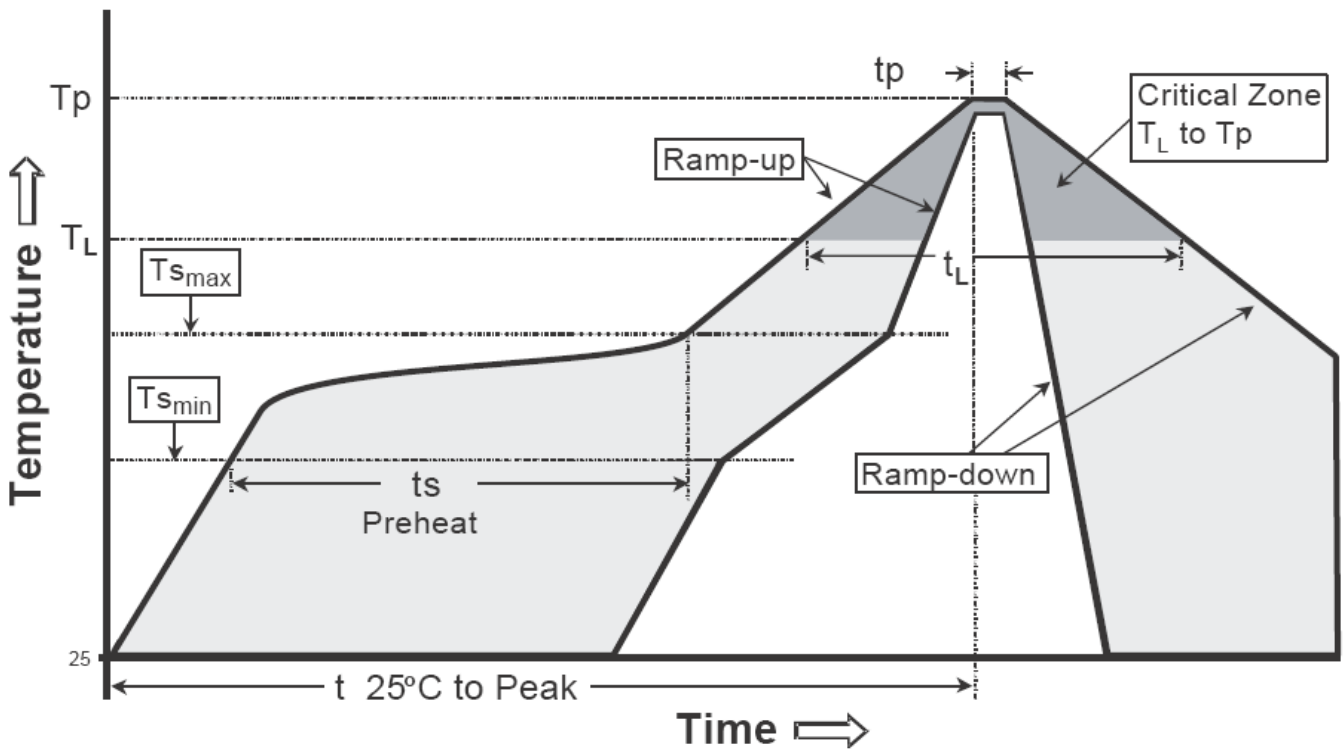
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

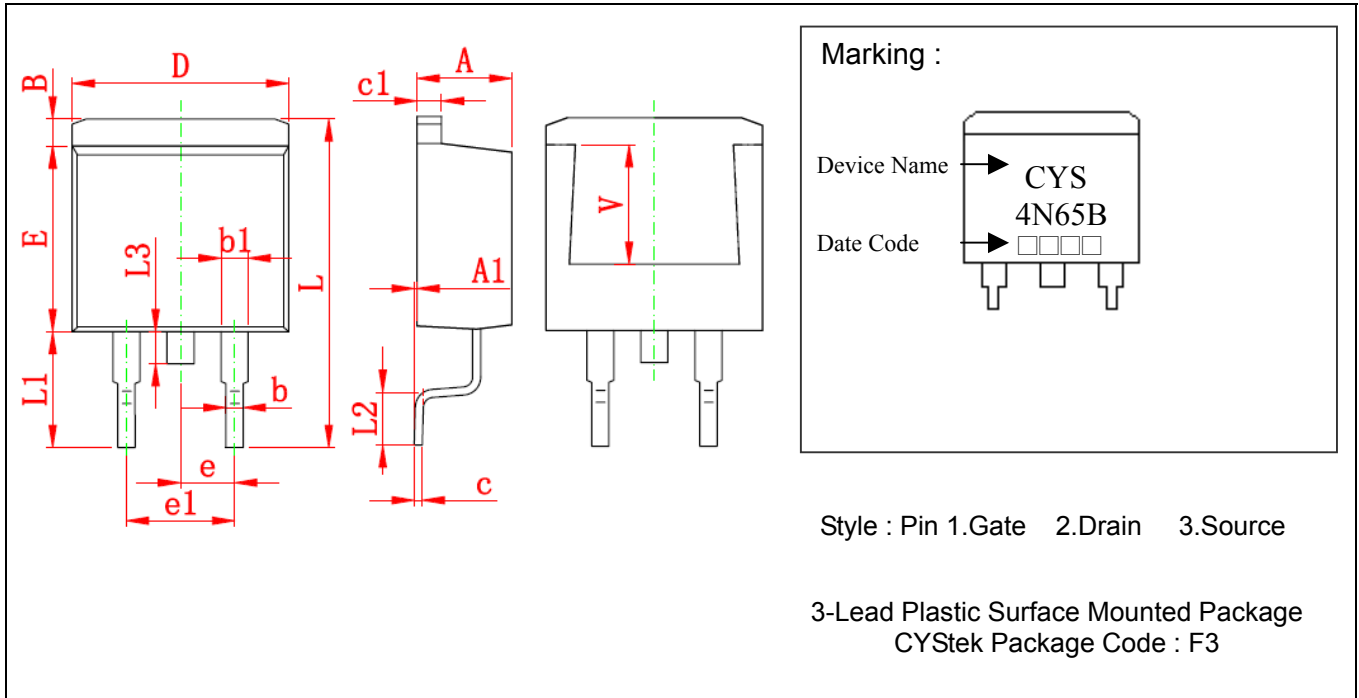
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-263 Dimension



Marking :

Device Name → **CYS**
 4N65B
 Date Code → □□□□

Style : Pin 1.Gate 2.Drain 3.Source

3-Lead Plastic Surface Mounted Package
 CYStek Package Code : F3

*:Typical

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	4.470	4.670	0.176	0.184	E	8.500	8.900	0.335	0.350
A1	0.000	0.150	0.000	0.006	e	*2.540		*0.100	
B	1.170	1.370	0.046	0.054	e1	4.980	5.180	0.196	0.204
b	0.710	0.910	0.028	0.036	L	15.050	15.450	0.593	0.608
b1	1.170	1.370	0.046	0.054	L1	5.080	5.480	0.200	0.216
c	0.310	0.530	0.012	0.021	L2	2.340	2.740	0.092	0.108
c1	1.170	1.370	0.046	0.054	L3	1.300	1.700	0.051	0.067
D	10.010	10.310	0.394	0.406	V	5.600	REF	0.220	REF

- Notes :**
- 1.Controlling dimension : millimeters.
 - 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 - 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

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