P-Channel Enhancement Mode Power MOSFET

MTEJ0P20V8

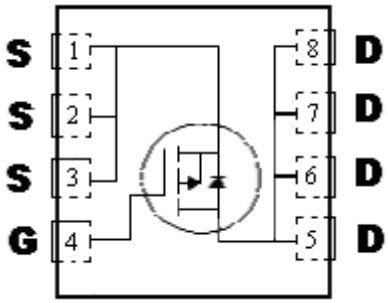
BV_{DSS}	-200V
I_D	-3.9A @ V_{GS}=-10V, T_C=25°C
$R_{DSON(Typ)}$	0.80Ω @ V_{GS}=-10V, I_D=-1A
	0.85Ω@ V_{GS}=-6V, I_D=-1A

Features

- Simple drive requirement
- Low on-resistance
- Fast switching speed
- Pb-free lead plating and halogen-free package

Equivalent Circuit

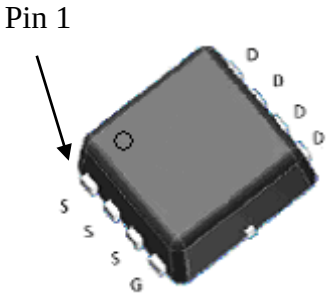
MTEJ0P20V8



G：Gate S：Source D：Drain

Outline

DFN3x3



Ordering Information

Device	Package	Shipping
MTEJ0P20V8-0-T6-G	DFN3x3 (Pb-free lead plating and halogen-free package)	3000 pcs / tape & reel

Environment friendly grade : S for RoHS compliant products, G for RoHS compliant and green compound products

Packing spec, T6 : 3000 pcs / tape & reel,13” reel

Product rank, zero for no rank products

Product name

Absolute Maximum Ratings (TC=25°C, unless otherwise noted)

Parameter		Symbol	Limits	Unit
Drain-Source Voltage		V_{DS}	-200	V
Gate-Source Voltage		V_{GS}	±30	
Continuous Drain Current @ T_C=25°C, V_{GS}=-10V		I_D	-3.9	A
Continuous Drain Current @ T_C=70°C, V_{GS}=-10V			-3.1	
Continuous Drain Current @ T_A=25°C, V_{GS}=-10V	*3, 4		-1.3	
Continuous Drain Current @ T_A=70°C, V_{GS}=-10V	*3, 4		-1.0	
Pulsed Drain Current	*1, 2	I_{DM}	-6.0	
Continuous Source-Drain Diode Current	T_C=25℃	I_S	-5	
	T_A=25℃		-3	
Avalanche Current		I_{AS}	-5	
Avalanche Energy @ L=2mH, I_D=-5A, R_G=25Ω		E_{AS}	25	mJ
Maximum Power Dissipation	T_C=25℃	P_D	33	W
	T_C=70℃		21	
	T_A=25℃ *3, 4		3.7	
	T_A=70℃ *3, 4		2.4	
Operating Junction and Storage Temperature Range		Tj, Tstg	-55~+150	℃

Thermal Data

Parameter		Symbol	Typ	Maximum	Unit
Thermal Resistance, Junction-to-ambient *3	t≤10s	$R_{th,j-a}$	28	34	°C/W
	Steady State		65	81	
Thermal Resistance, Junction-to-case		$R_{th,j-c}$	2.9	3.8	

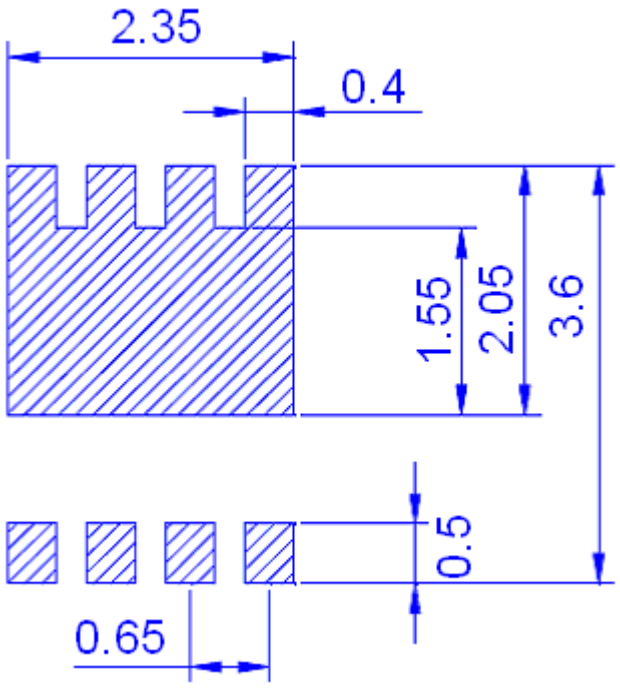
Note : 1. Pulse width limited by maximum junction temperature.
2. Duty cycle≤1%.
3. Surface mounted on 1 in² copper pad of FR-4 board.
4. t≤10s.

Characteristics (Tc=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV_{DSS}	-200	-	-	V	V_{GS}=0V, I_D=-250μA
$\Delta BV_{DSS}/T_J$	-	-160	-	mV/°C	I_D=-250μA
$\Delta V_{GS(th)}/T_J$	-	-7.3	-		
$V_{GS(th)}$	-2	-3	-4	V	V_{DS} =V_{GS}, I_D=-250μA
I_{GSS}	-	-	±100	nA	V_{GS}=±30V, V_{DS}=0V
I_{DSS}	-	-	-1	μA	V_{DS} =-200V, V_{GS} =0V
	-	-	-10		V_{DS} =-200V, V_{GS} =0V, T_J=55°C
$R_{DS(ON)}$ *1	-	0.80	1.0	Ω	V_{GS} =-10V, I_D=-1A
	-	0.85	1.1		V_{GS} =-6V, I_D=-1A
G_{FS} *1	-	2	-	S	V_{DS} =-15V, I_D=-1A
Dynamic					
Qg(V_{GS}=-10V) *1, 2	-	11	18	nC	V_{DS}=-100V, I_D=-1A,V_{GS}=-10V
Qg(V_{GS}=-6V) *1, 2	-	7.7	12		
Qgs *1, 2	-	2.0	-		
Qgd *1, 2	-	4.2	-		
$t_{d(ON)}$ *1, 2	-	13	20	ns	V_{DS}=-100V, I_D=-1A, V_{GS}=-10V, R_G=1Ω
tr *1, 2	-	7	11		
$t_{d(OFF)}$ *1, 2	-	21	32		
t_f *1, 2	-	11	17		
$t_{d(ON)}$ *1, 2	-	13	20	ns	V_{DS}=-100V, I_D=-1A, V_{GS}=-6V, R_G=1Ω
tr *1, 2	-	20	30		
$t_{d(OFF)}$ *1, 2	-	15	23		
t_f *1, 2	-	11	17		
Ciss	-	765	-	pF	V_{DS}=-50V, V_{GS}=0V, f=1MHz
Coss	-	29	-		
Crss	-	12	-		
Rg	-	13	16	Ω	f=1MHz
Source-Drain Diode					
I_S *1	-	-	-5	A	T_C=25°C
I_{SM} *3	-	-	-5		
V_{SD} *1	-	-0.79	-1.2	V	I_F=-1A, V_{GS}=0V
trr	-	72	100	ns	I_F=-4A, dI_F/dt=100A/μs
Qrr	-	240	310	nC	
ta		52		ns	
tb		20			

Note : *1.Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%
*2.Independent of operating temperature
*3.Pulse width limited by maximum junction temperature.

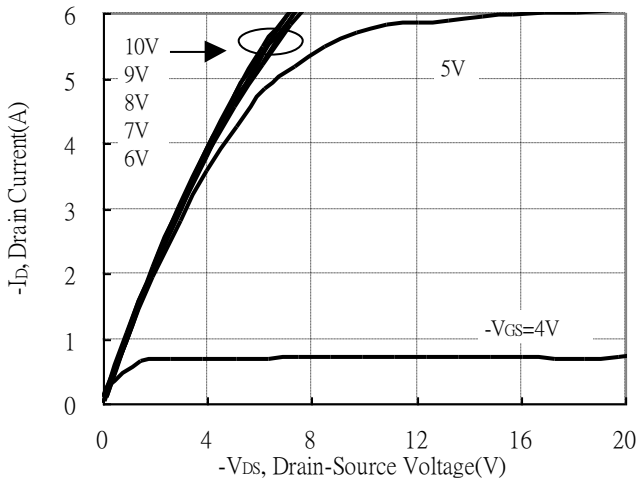
Recommended Soldering Footprint



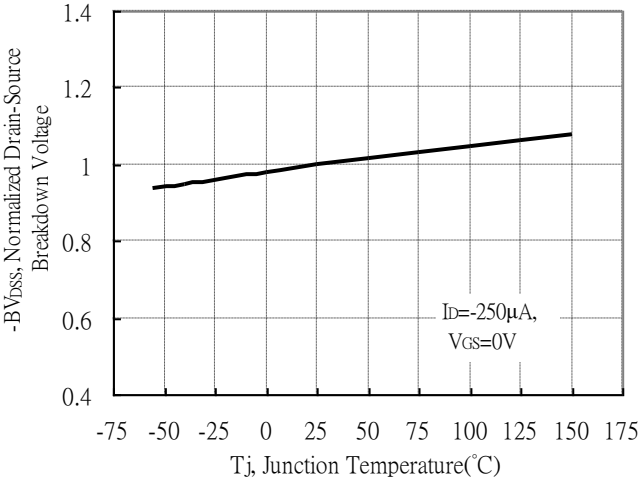
unit : mm

Typical Characteristics

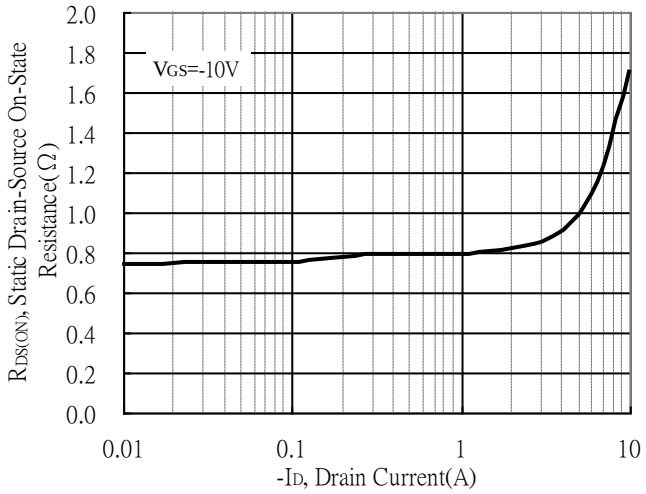
Typical Output Characteristics



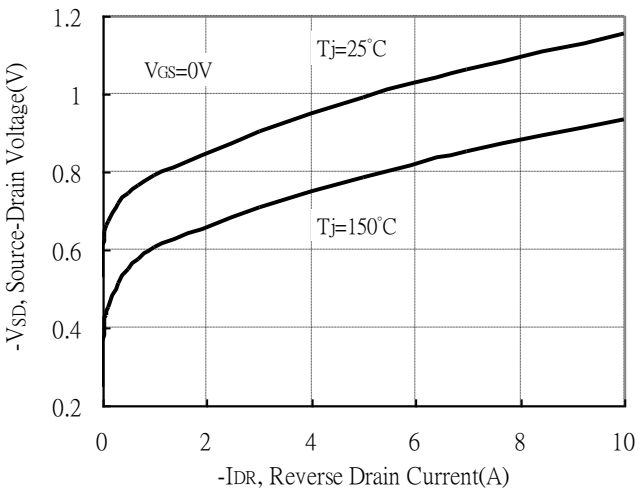
Brekdown Voltage vs Ambient Temperature



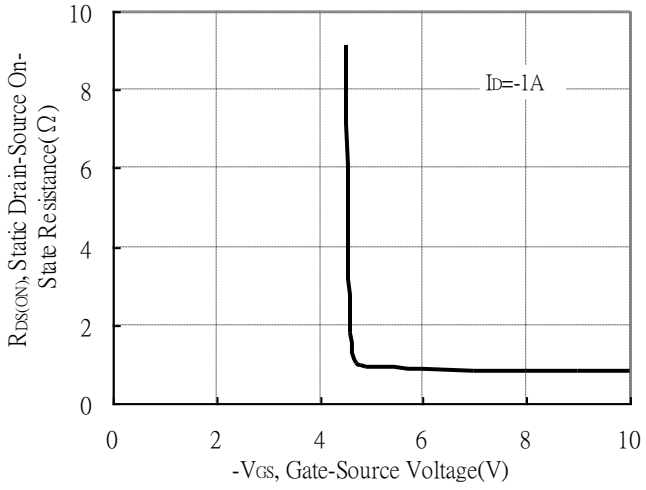
Static Drain-Source On-State resistance vs Drain Current



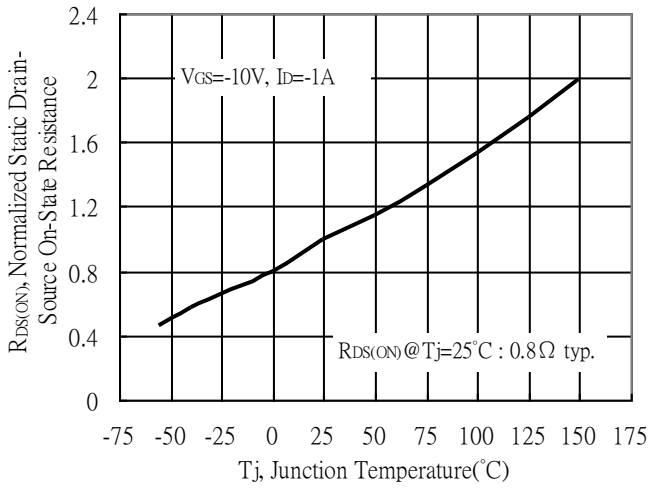
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

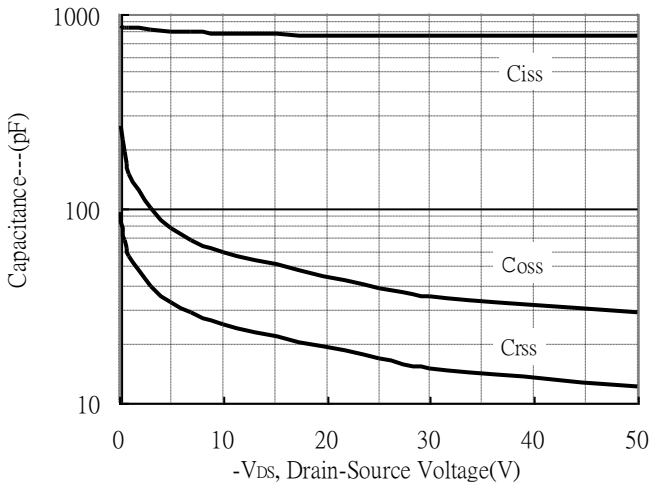


Drain-Source On-State Resistance vs Junction Tempearture

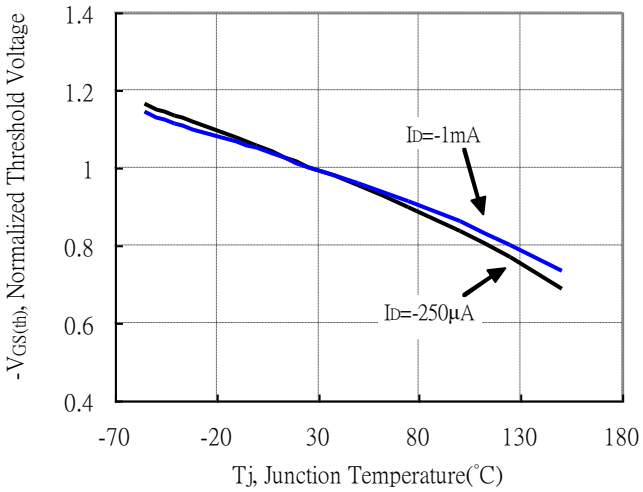


Typical Characteristics(Cont.)

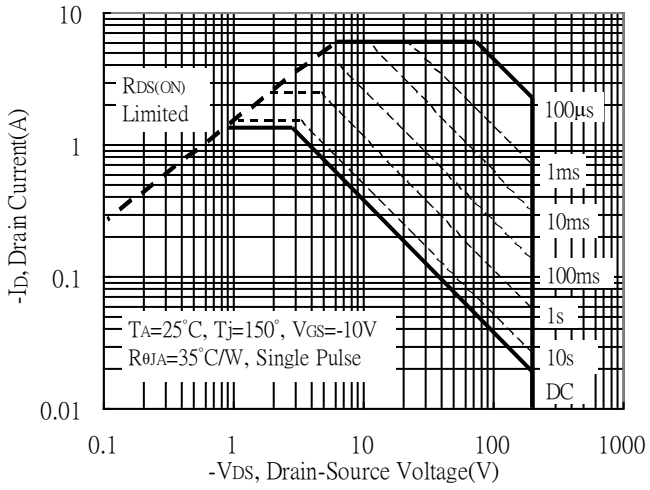
Capacitance vs Drain-to-Source Voltage



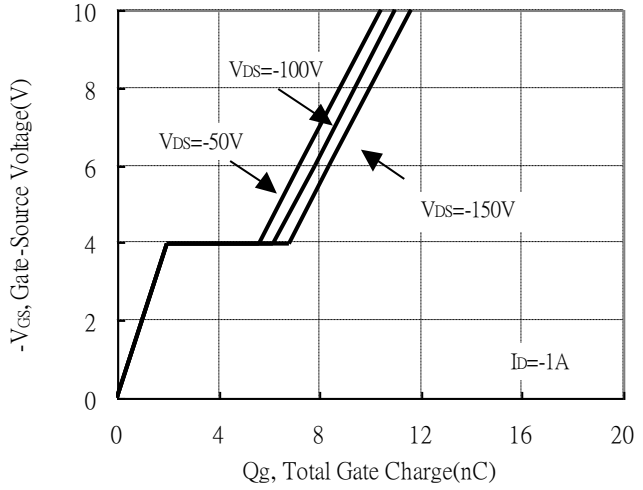
Threshold Voltage vs Junction Tempearture



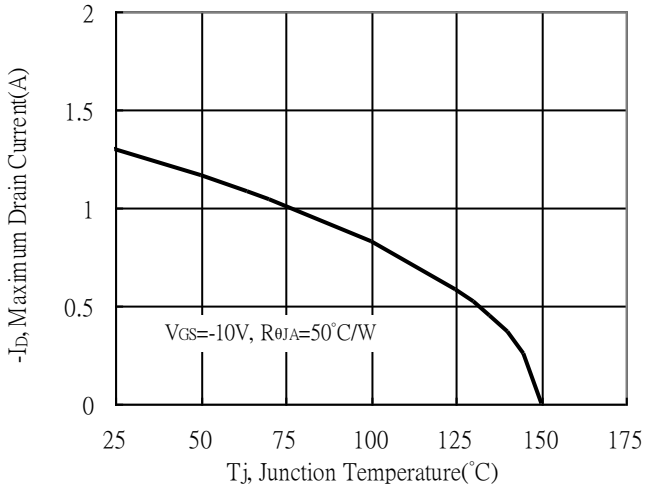
Maximum Safe Operating Area



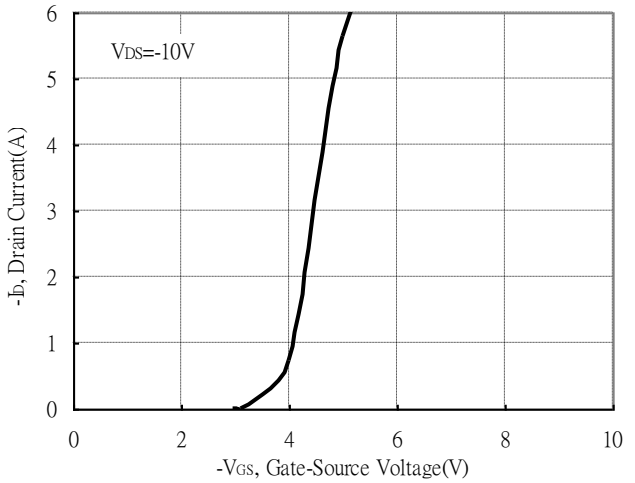
Gate Charge Characteristics



Maximum Drain Current vs Junction Temperature

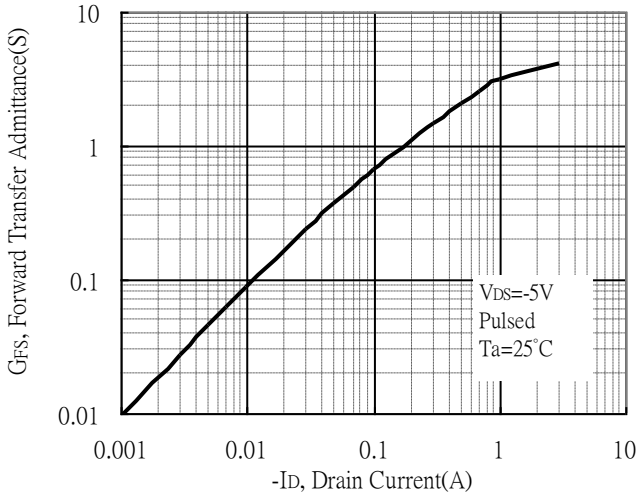


Typical Transfer Characteristics

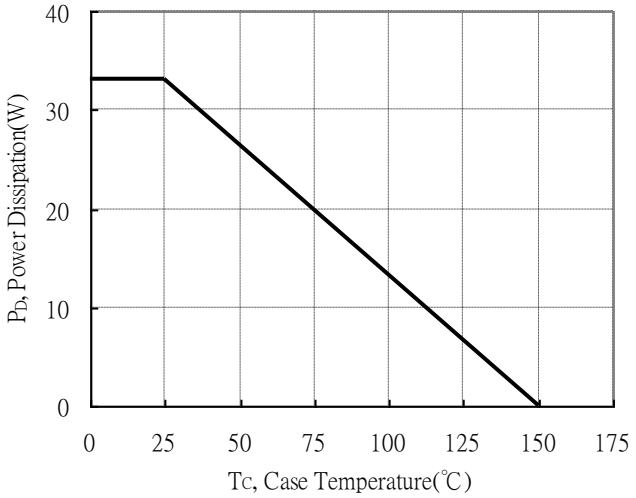


Typical Characteristics(Cont.)

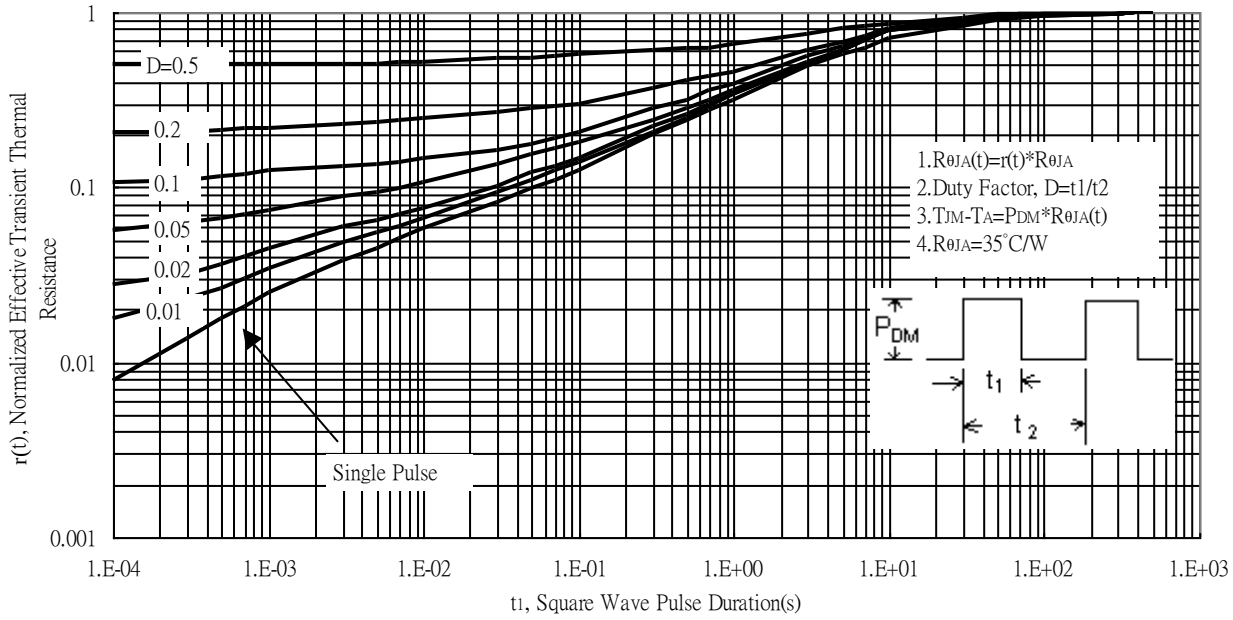
Forward Transfer Admittance vs Drain Current



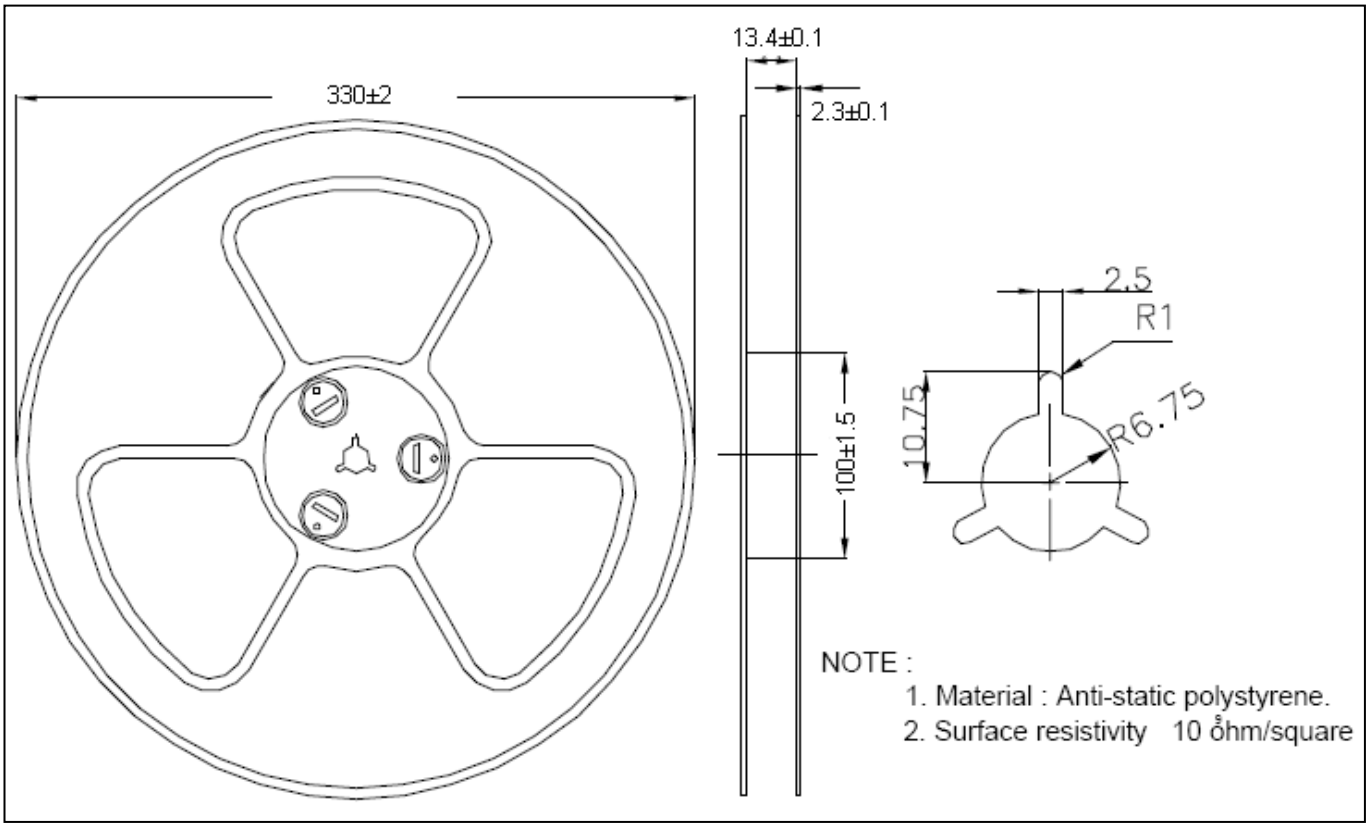
Power Derating Curve



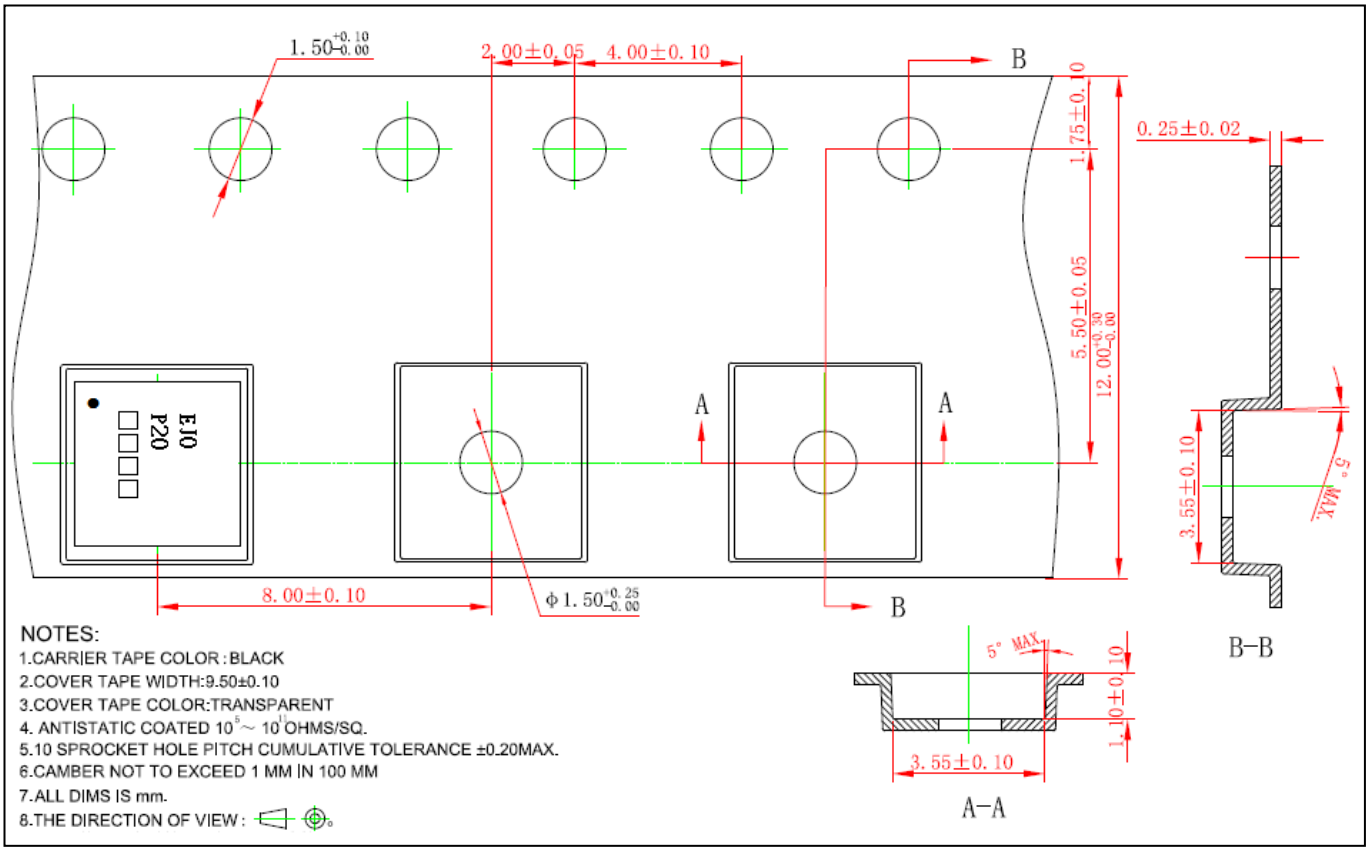
Transient Thermal Response Curves



Reel Dimension



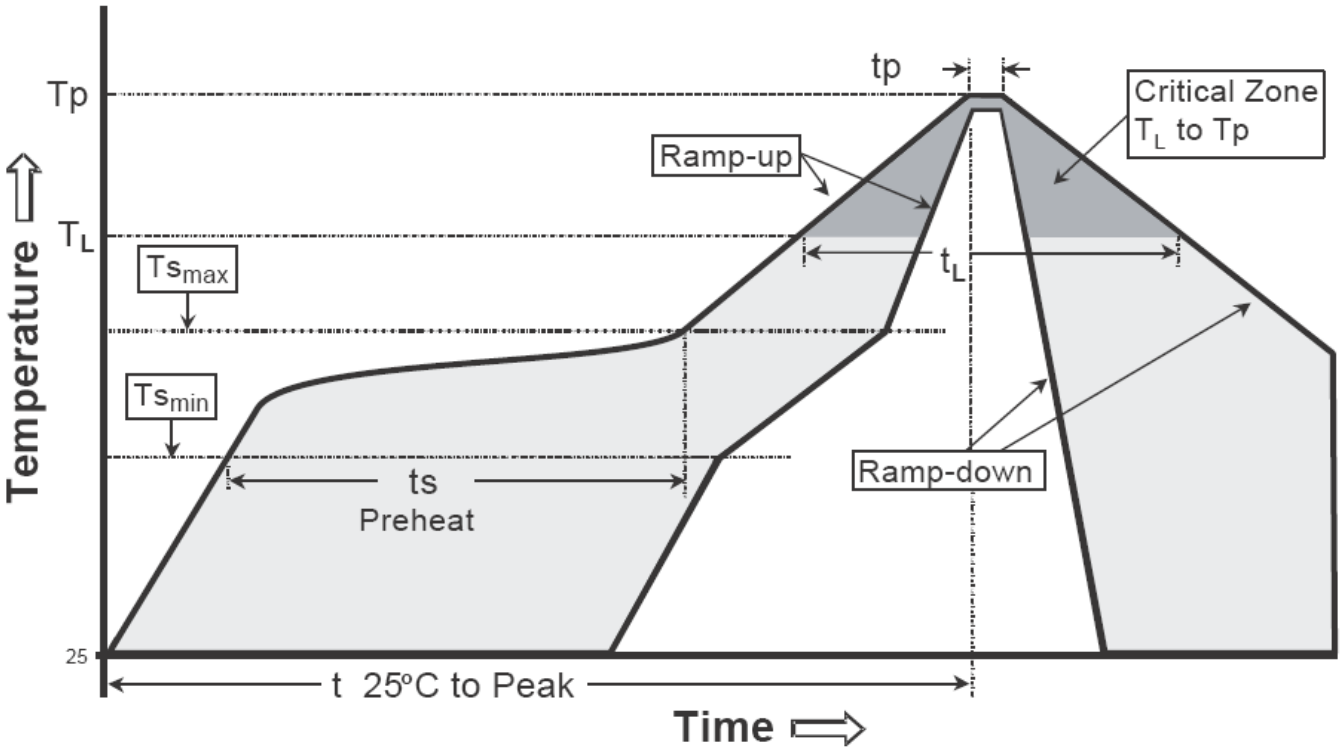
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

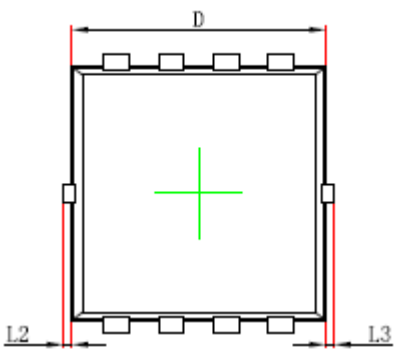
Recommended temperature profile for IR reflow



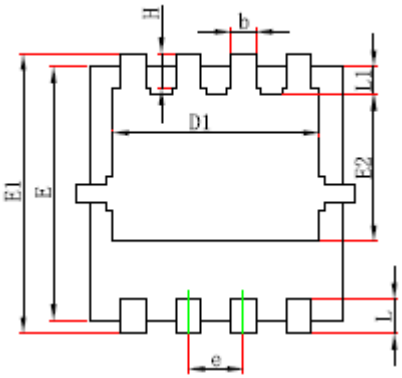
Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(T_S min) −Temperature Max(T_S max) −Time($t_{s\ min}$ to $t_{s\ max}$)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (T_L) − Time (t_L)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(T_P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

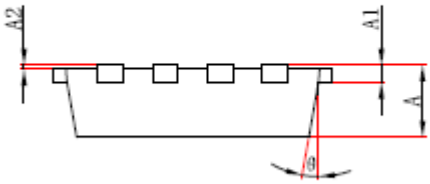
DFN3x3 Dimension



Top View



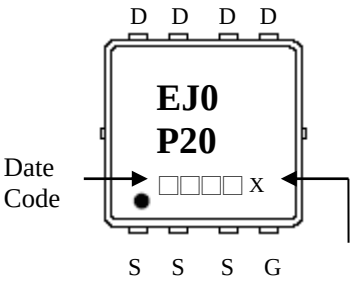
Bottom View



Side View

8-Lead DFN3x3 Plastic Package
CYStek Package Code: V8

Marking:



Assembly site code :
blank →site 1
G→site 2

Date Code(counting from left to right) :
1st code: year code, the last digit of Christian year
2nd code : month code, Jan→A, Feb→B, Mar→C, Apr→D
May→E, Jun→F, Jul→G, Aug→H, Sep→J,
Oct→K, Nov→L, Dec→M
3rd and 4th codes : production serial number, 01~99

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.026	0.033	0.650	0.850	b	0.008	0.016	0.200	0.400
A1	0.006	REF	0.152	REF	e	0.022	0.030	0.550	0.750
A2	0.000	0.002	0.000	0.050	L	0.012	0.020	0.300	0.500
D	0.114	0.126	2.900	3.200	L1	0.007	0.019	0.180	0.480
D1	0.091	0.102	2.300	2.600	L2	0.000	0.006	0.000	0.150
E	0.114	0.126	2.900	3.200	L3	0.000	0.006	0.000	0.150
E1	0.124	0.136	3.150	3.450	H	0.012	0.020	0.300	0.515
E2	0.058	0.076	1.480	1.935	θ	8°	13°	8°	13°

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.