

**N-Channel Enhancement Mode Power MOSFET**

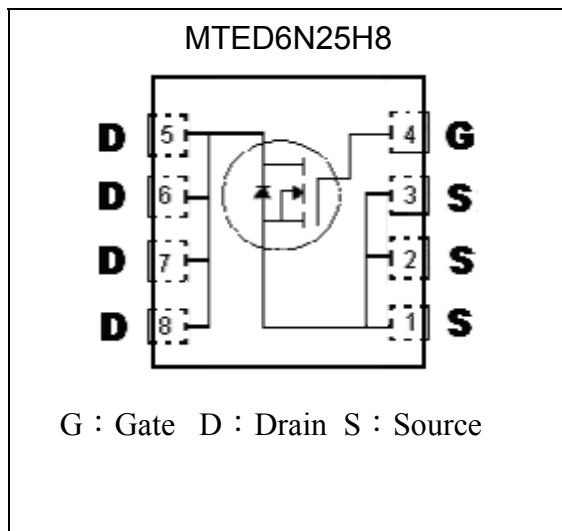
# MTED6N25H8

BV <sub>DSS</sub>	250V
I <sub>D</sub> @V <sub>GS</sub> =10V, T <sub>C</sub> =25°C	4.6A
I <sub>D</sub> @V <sub>GS</sub> =10V, T <sub>A</sub> =25°C	1.2A
R <sub>DS(on)(TYP)</sub>   V <sub>GS</sub> =10V, I <sub>D</sub> =5A	426mΩ

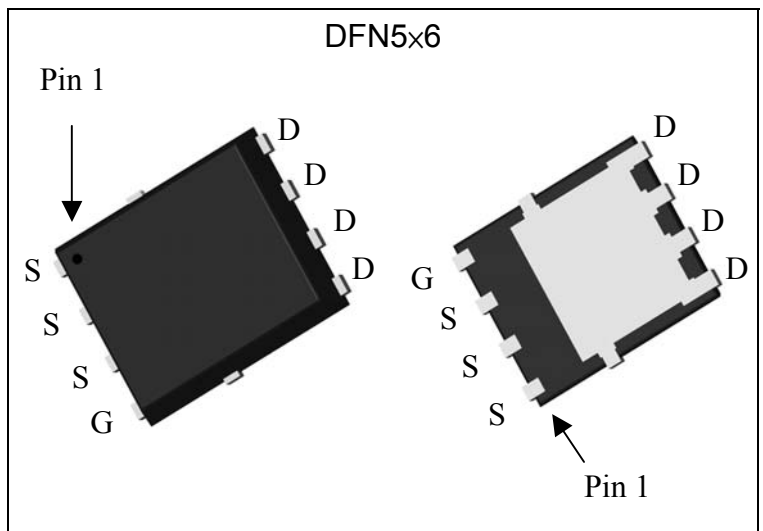
**Features**

- Single Drive Requirement
- Low On-resistance
- Fast Switching Characteristic
- Repetitive Avalanche Rated
- Pb-free lead plating and Halogen-free package

**Symbol**

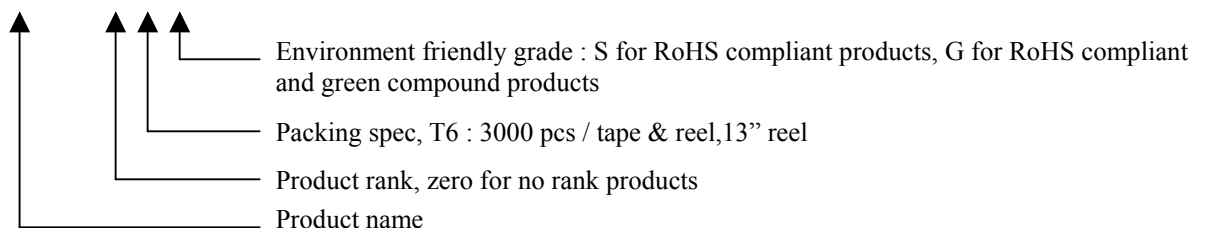


**Outline**



**Ordering Information**

Device	Package	Shipping
MTED6N25H8-0-T6-G	DFN 5 x6 (Pb-free lead plating and halogen-free package)	3000 pcs / tape & reel





**Absolute Maximum Ratings (Ta=25°C)**

Parameter	Symbol	Limits	Unit	
Drain-Source Voltage	V <sub>DS</sub>	250	V	
Gate-Source Voltage	V <sub>GS</sub>	±30		
Continuous Drain Current @ T <sub>C</sub> =25°C, V <sub>GS</sub> =10V (Note 1)	I <sub>D</sub>	4.6	A	
Continuous Drain Current @ T <sub>C</sub> =100°C, V <sub>GS</sub> =10V (Note 1)		3.3		
Continuous Drain Current @ T <sub>A</sub> =25°C, V <sub>GS</sub> =10V (Note 2)	I <sub>DSM</sub>	1.2 *3		
Continuous Drain Current @ T <sub>A</sub> =70°C, V <sub>GS</sub> =10V (Note 2)		1.0 *3		
Pulsed Drain Current (Note 3)	I <sub>DM</sub>	18.4 *1		
Avalanche Current (Note 3)	I <sub>AS</sub>	9		
Avalanche Energy @ L=10mH, I <sub>D</sub> =4.6A, V <sub>DD</sub> =50V (Note 5)	E <sub>AS</sub>	106	mJ	
Repetitive Avalanche Energy @ L=0.05mH (Note 3)	E <sub>AR</sub>	3 *2		
Total Power Dissipation	P <sub>D</sub>	T <sub>C</sub> =25°C (Note 1)	30	W
		T <sub>C</sub> =100°C (Note 1)	15	
	P <sub>D</sub> SM	T <sub>A</sub> =25°C (Note 2)	1.9	
		T <sub>A</sub> =70°C (Note 2)	1.2	
Operating Junction and Storage Temperature Range	T <sub>j</sub> , T <sub>stg</sub>	-55~+175	°C	

**Thermal Data**

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	R <sub>θJC</sub>	5	°C/W
Thermal Resistance, Junction-to-ambient, max (Note 2)	R <sub>θJA</sub>	65	
Thermal Resistance, Junction-to-ambient, max (Note 4)		125	

- Note : 1. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175 °C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
2. The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2 oz. copper, in a still air environment with T<sub>A</sub>=25 °C. The power dissipation P<sub>D</sub>SM is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
3. Pulse width limited by junction temperature T<sub>J(MAX)</sub>=175 °C. Ratings are based on low frequency and low duty cycles to keep initial T<sub>J</sub>=25°C.
4. When mounted on the minimum pad size recommended (PCB mount), t<sub>≤</sub>10s.
5. 100% tested by conditions of L=2mH, I<sub>AS</sub>=2A, V<sub>GS</sub>=10V, V<sub>DD</sub>=50V

**Characteristics (Tc=25°C, unless otherwise specified)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
<b>Static</b>					
BV <sub>DSS</sub>	250	-	-	V	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA
ΔBV <sub>DSS</sub> /ΔT <sub>j</sub>	-	0.2	-	V/°C	Reference to 25°C, I <sub>D</sub> =250μA
V <sub>GS(th)</sub>	2	-	4	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA
G <sub>FS</sub> *1	-	5.6	-	S	V <sub>DS</sub> =15V, I <sub>D</sub> =5A
I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> =±30V
I <sub>DSS</sub>	-	-	1	μA	V <sub>DS</sub> =200V, V <sub>GS</sub> =0V
	-	-	25		V <sub>DS</sub> =160V, V <sub>GS</sub> =0V, T <sub>j</sub> =125°C
R <sub>DS(ON)</sub> *1	-	426	550	mΩ	V <sub>GS</sub> =10V, I <sub>D</sub> =5A



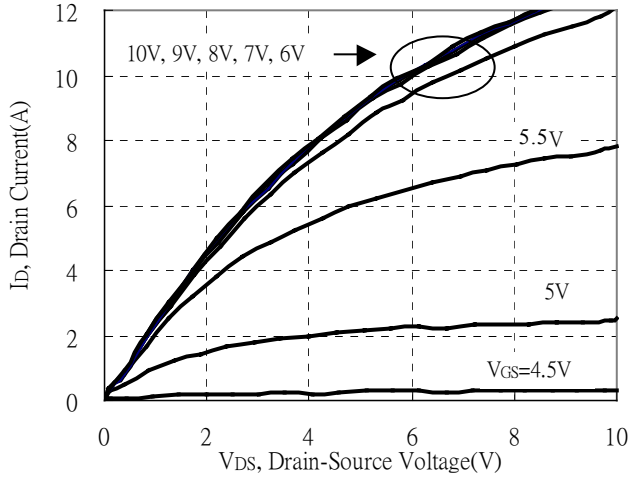
<b>Dynamic</b>					
Ciss	-	468	-	pF	V <sub>GS</sub> =0V, V <sub>DS</sub> =50V, f=1MHz
Coss	-	39	-		
Crss	-	22	-		
Qg *1, 2	-	13.2	-	nC	I <sub>D</sub> =5A, V <sub>DS</sub> =200V, V <sub>GS</sub> =10V
Qgs *1, 2	-	2.5	-		
Qgd *1, 2	-	5.4	-		
t <sub>d(ON)</sub> *1, 2	-	10.2	-	ns	V <sub>DS</sub> =125V, I <sub>D</sub> =5A, V <sub>GS</sub> =10V, R <sub>G</sub> =2.7Ω
t <sub>r</sub> *1, 2	-	18.2	-		
t <sub>d(OFF)</sub> *1, 2	-	22.4	-		
t <sub>f</sub> *1, 2	-	15.4	-		
Rg	-	3.8	-	Ω	f=1MHz
<b>Source-Drain Diode</b>					
I <sub>S</sub> *1	-	-	4.6	A	
I <sub>SM</sub> *3	-	-	18.4		
V <sub>SD</sub> *1	-	0.75	1.2	V	I <sub>S</sub> =1A, V <sub>GS</sub> =0V
t <sub>rr</sub>	-	74.6	-	ns	I <sub>F</sub> =5A, dI <sub>F</sub> /dt=100A/μs
Q <sub>rr</sub>	-	183.7	-	nC	

Note : \*1.Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%  
 \*2.Independent of operating temperature  
 \*3.Pulse width limited by maximum junction temperature.

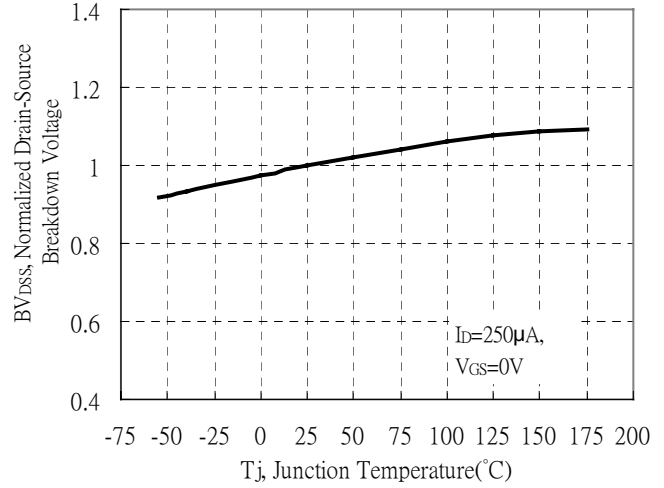


**Typical Characteristics**

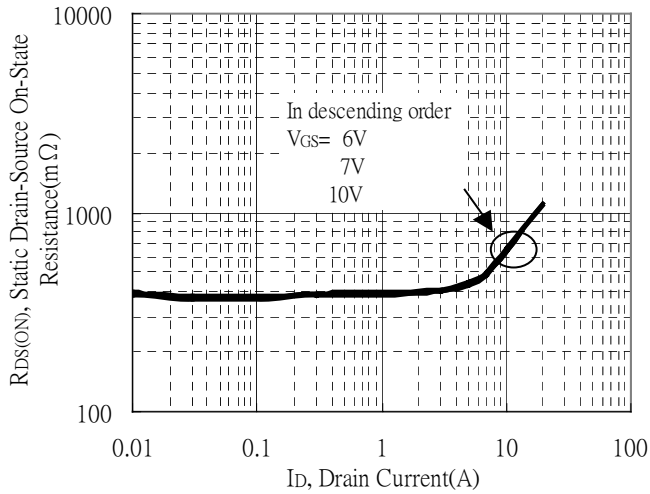
Typical Output Characteristics



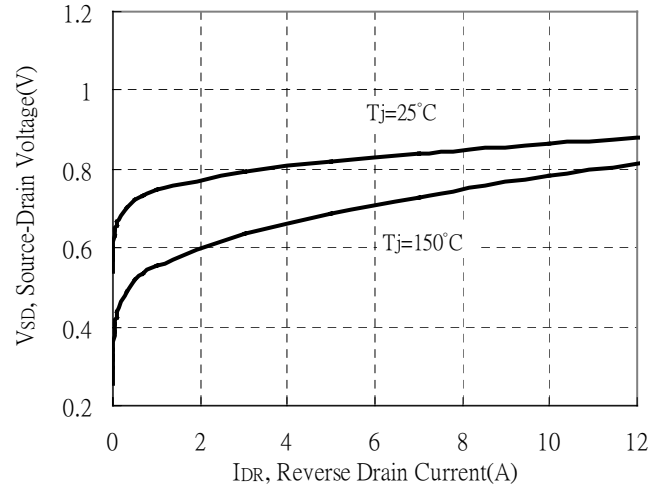
Brekdown Voltage vs Ambient Temperature



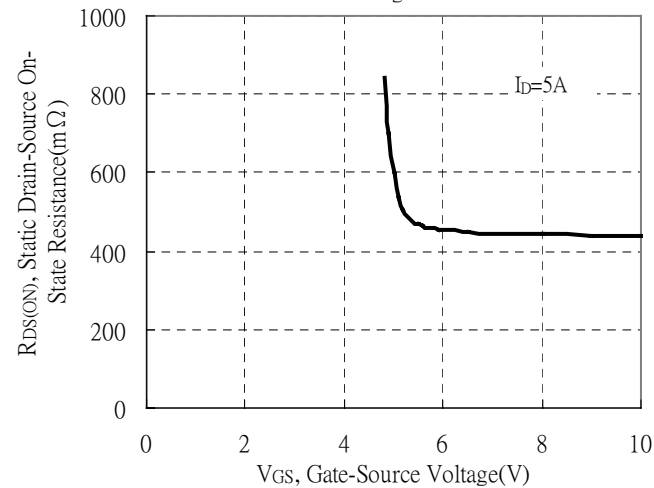
Static Drain-Source On-State resistance vs Drain Current



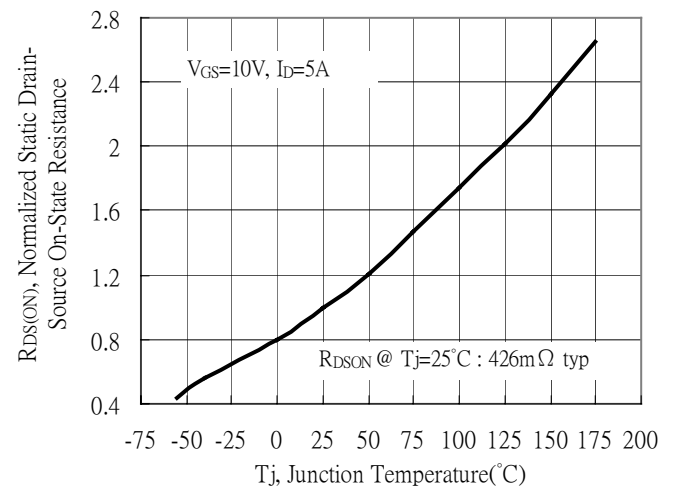
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage



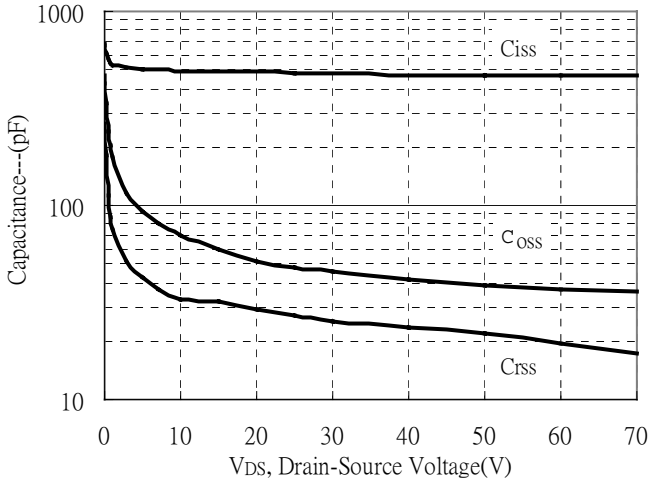
Drain-Source On-State Resistance vs Junction Temperature



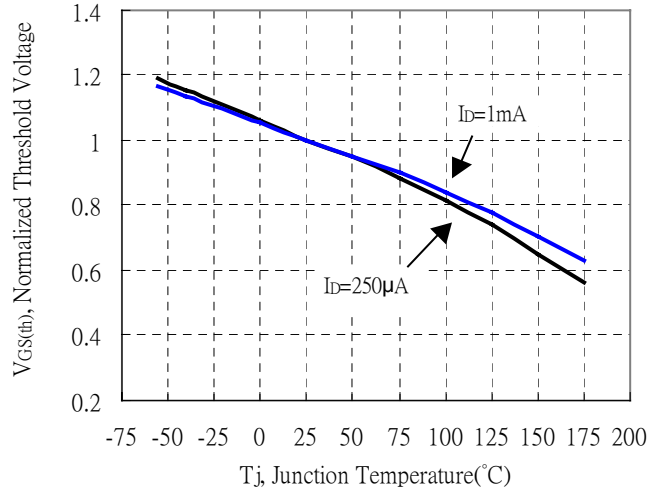


**Typical Characteristics(Cont.)**

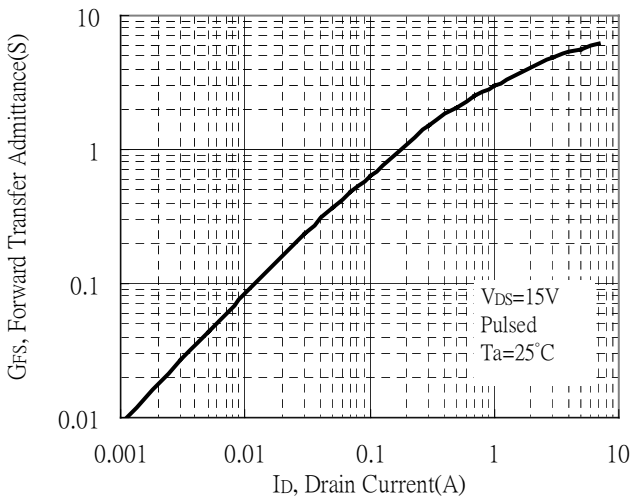
Capacitance vs Drain-to-Source Voltage



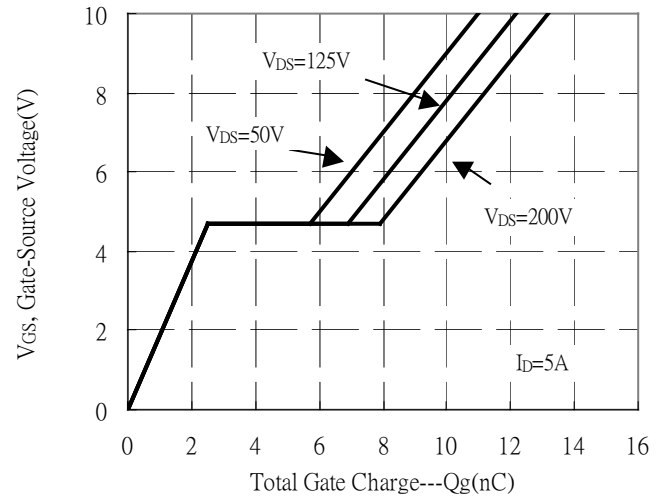
Normalized Threshold Voltage vs Junction Temperature



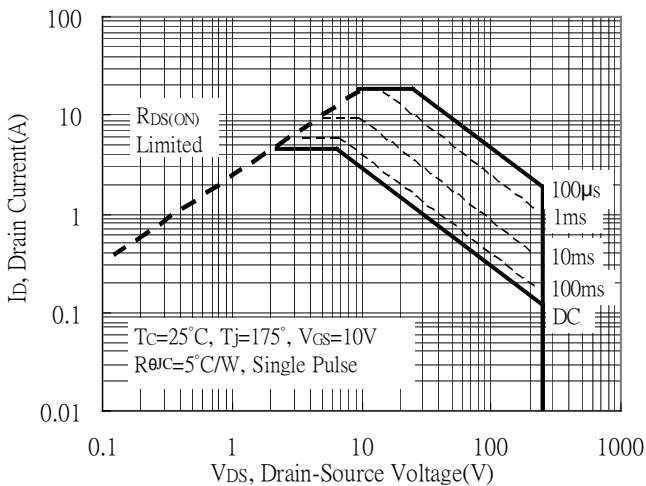
Forward Transfer Admittance vs Drain Current



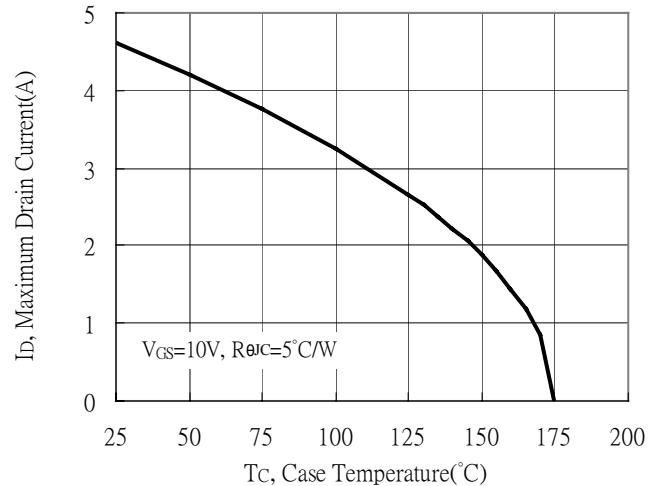
Gate Charge Characteristics



Maximum Safe Operating Area



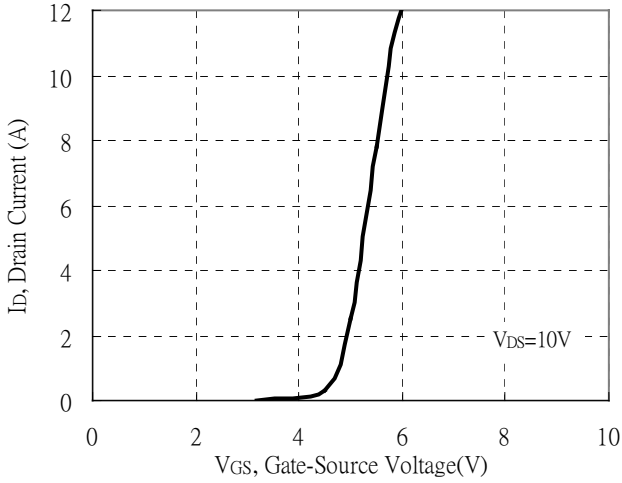
Maximum Drain Current vs Case Temperature



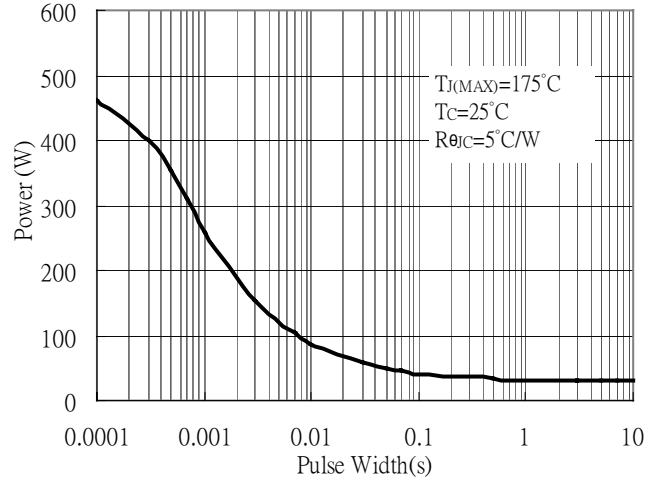


### Typical Characteristics(Cont.)

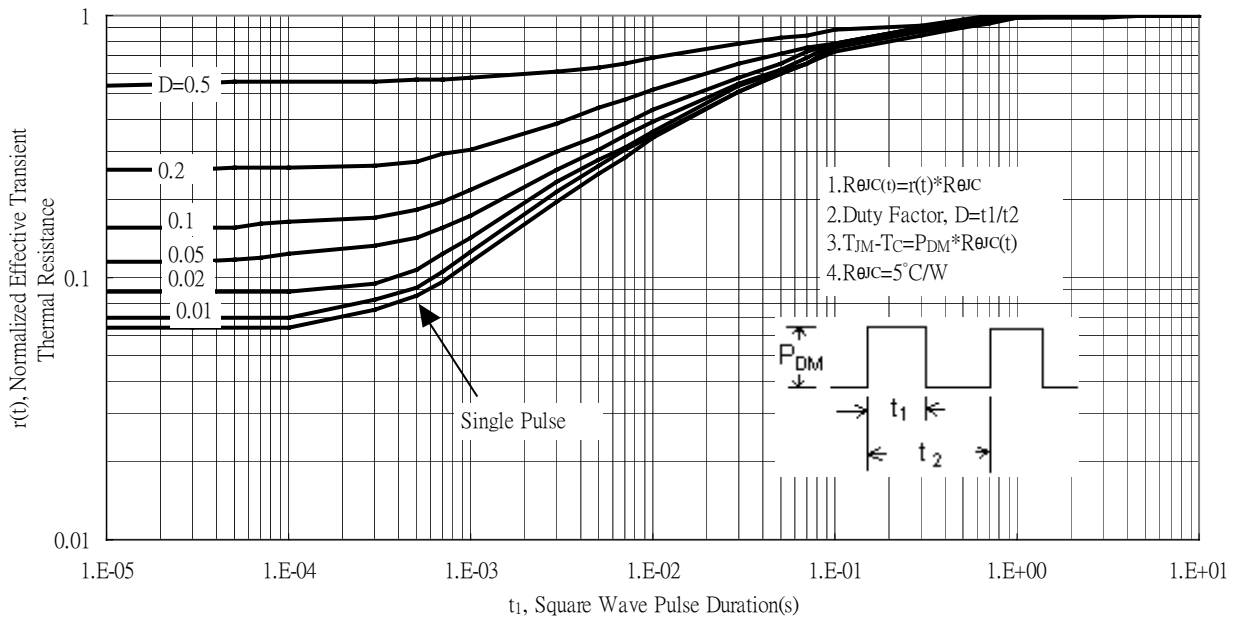
Typical Transfer Characteristics



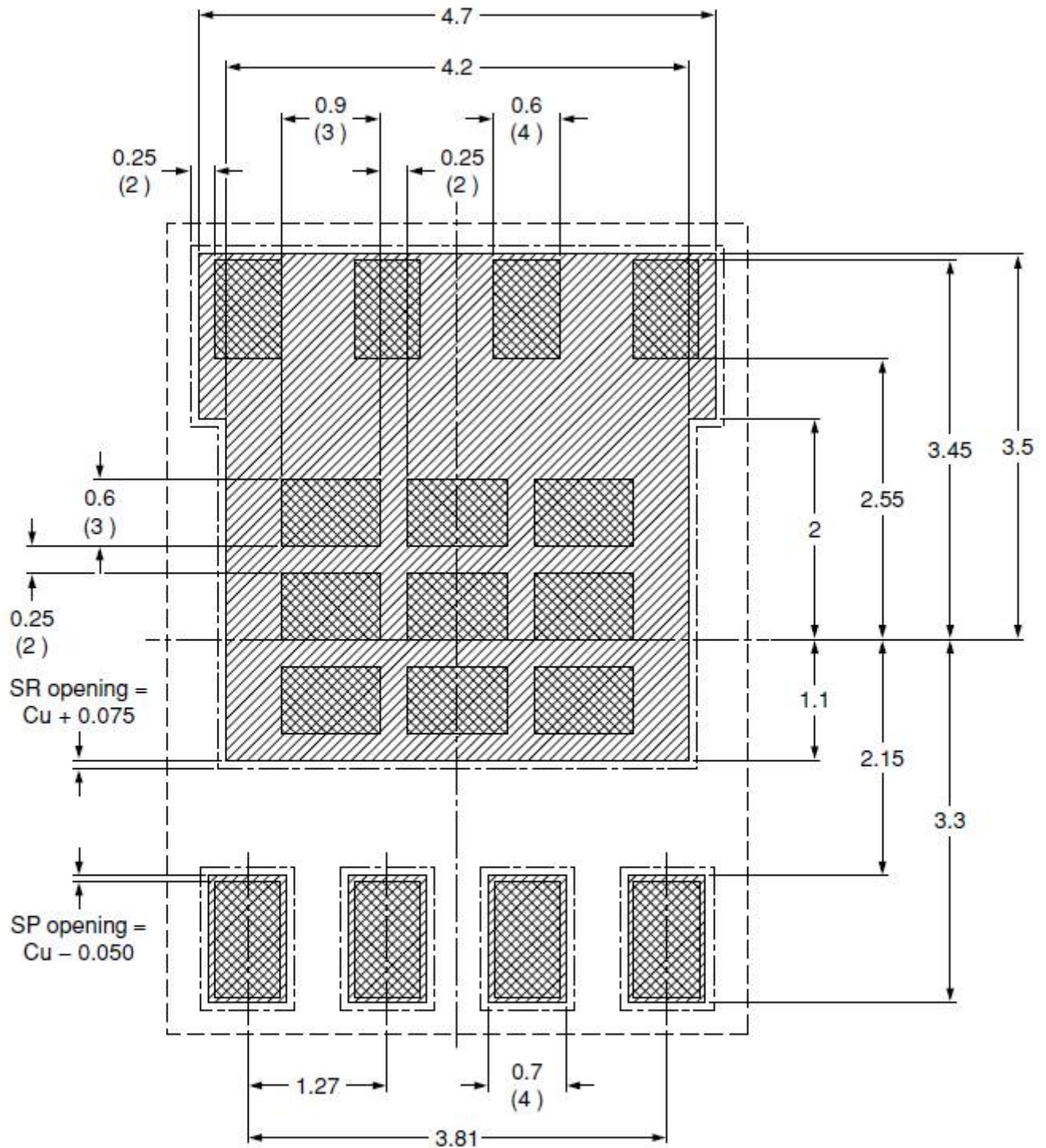
Single Pulse Maximum Power Dissipation



Transient Thermal Response Curves

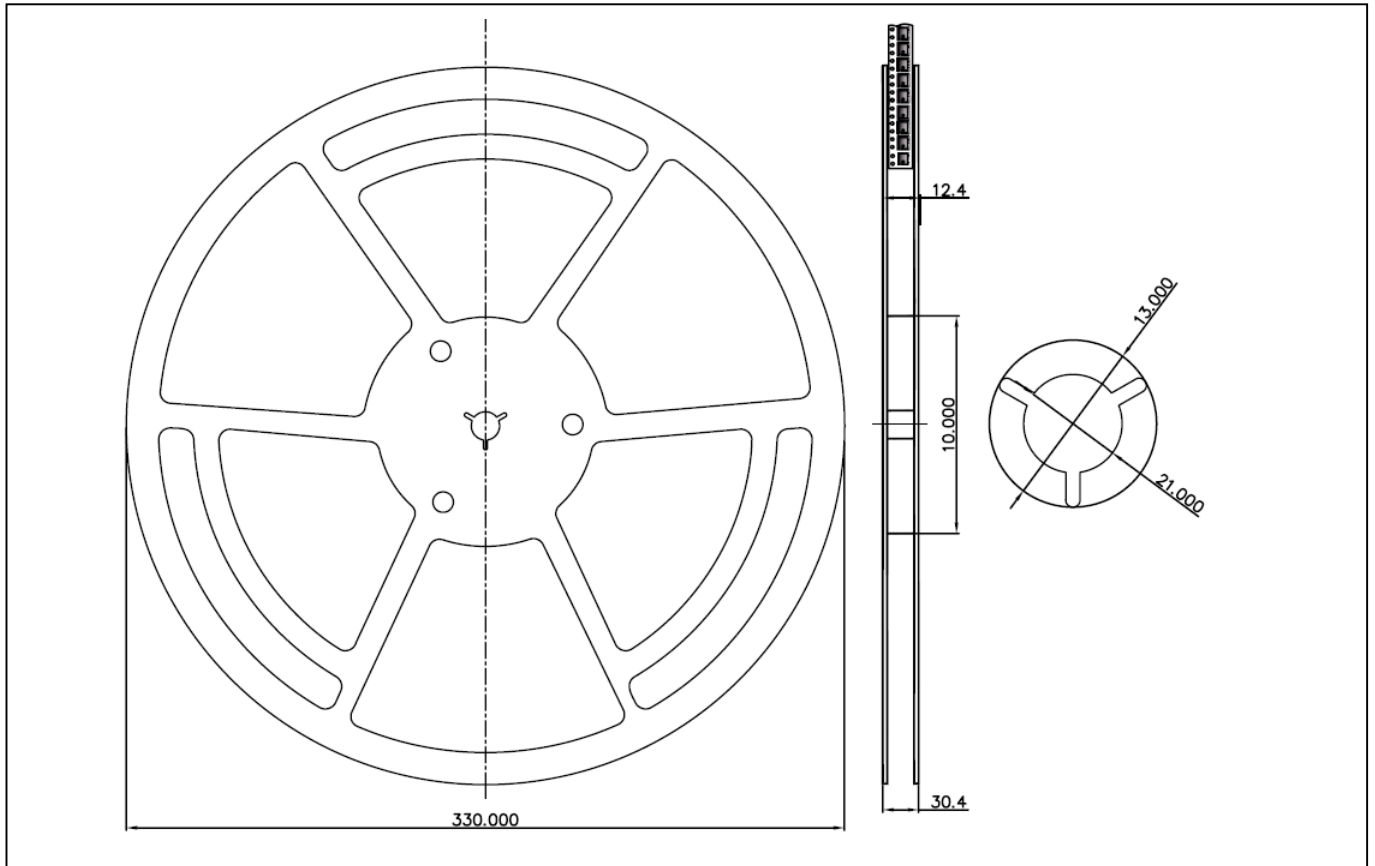


**Recommended Soldering Footprint & Stencil Design**

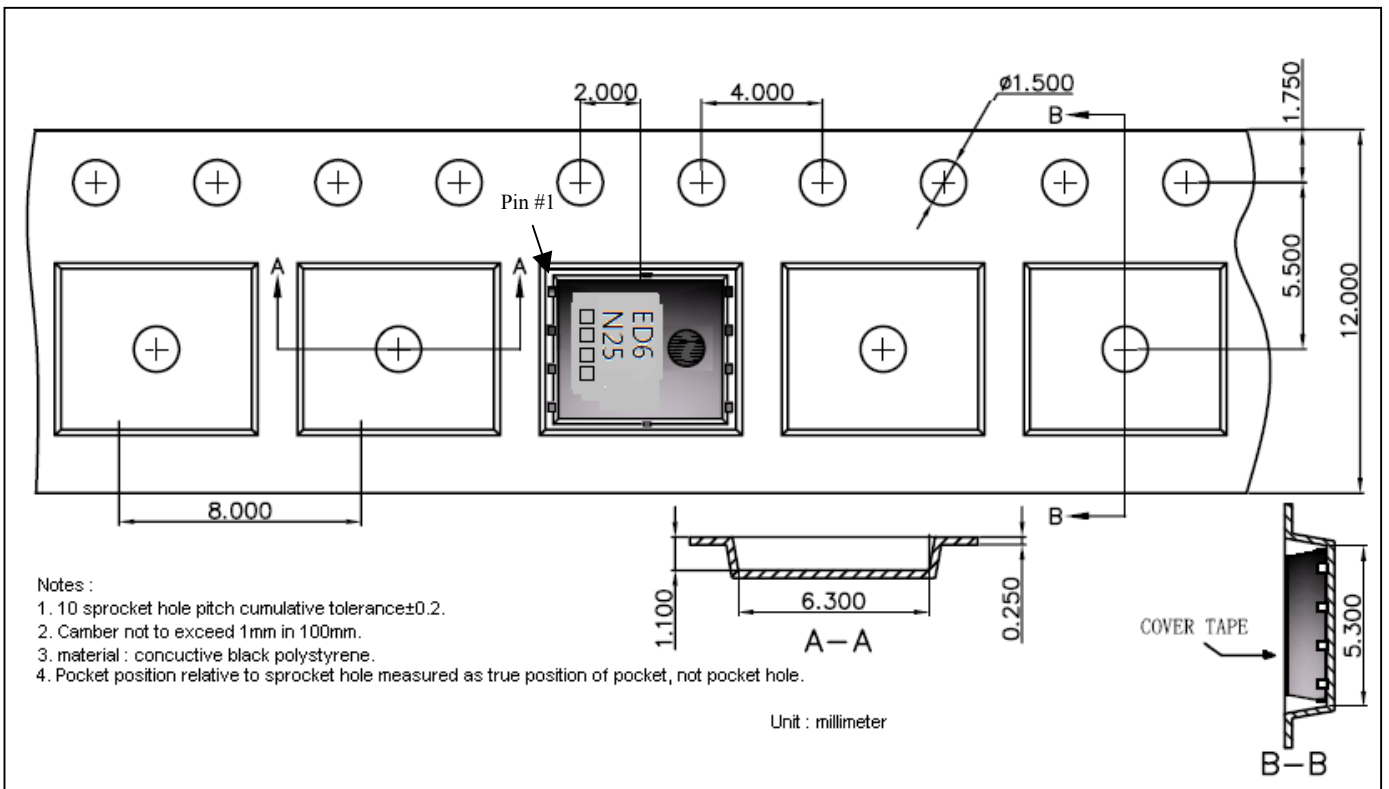


unit : mm

**Reel Dimension**



**Carrier Tape Dimension**



Notes :

1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.2$ .
2. Camber not to exceed 1mm in 100mm.
3. material : conductive black polystyrene.
4. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

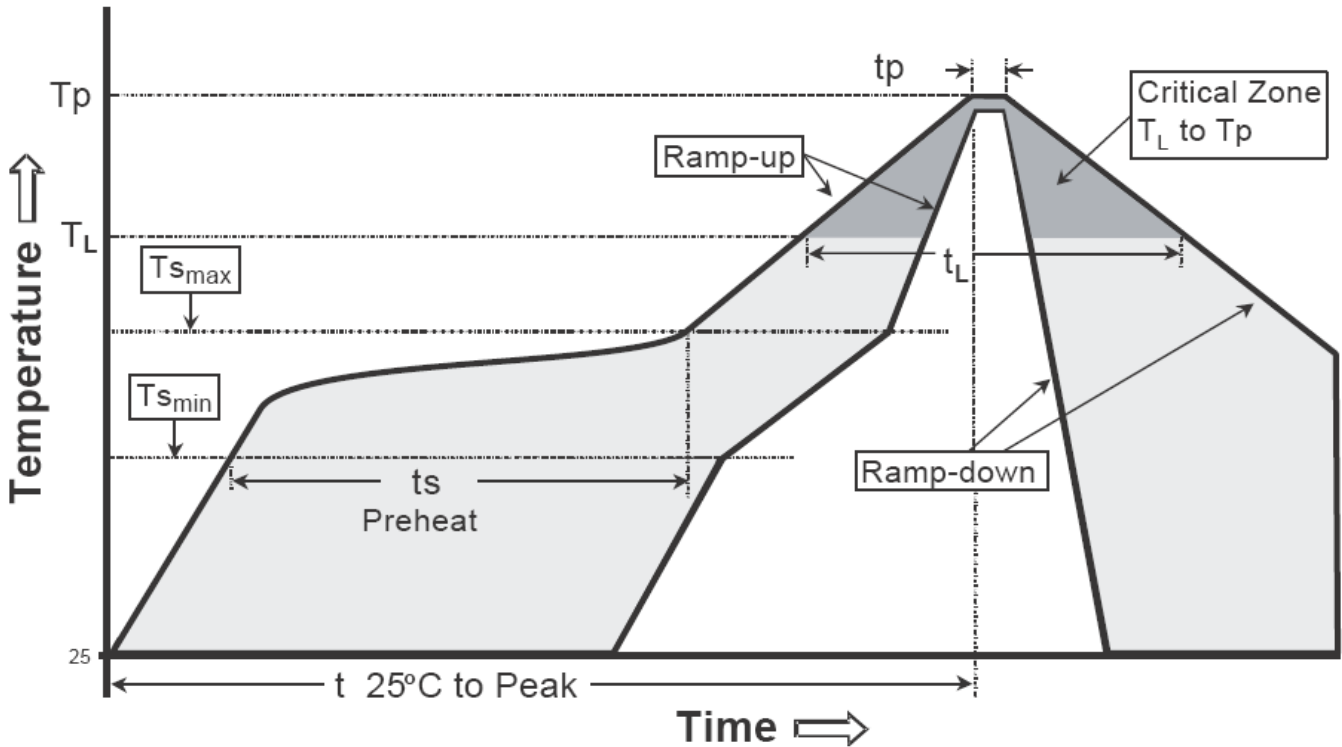
Unit : millimeter



**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

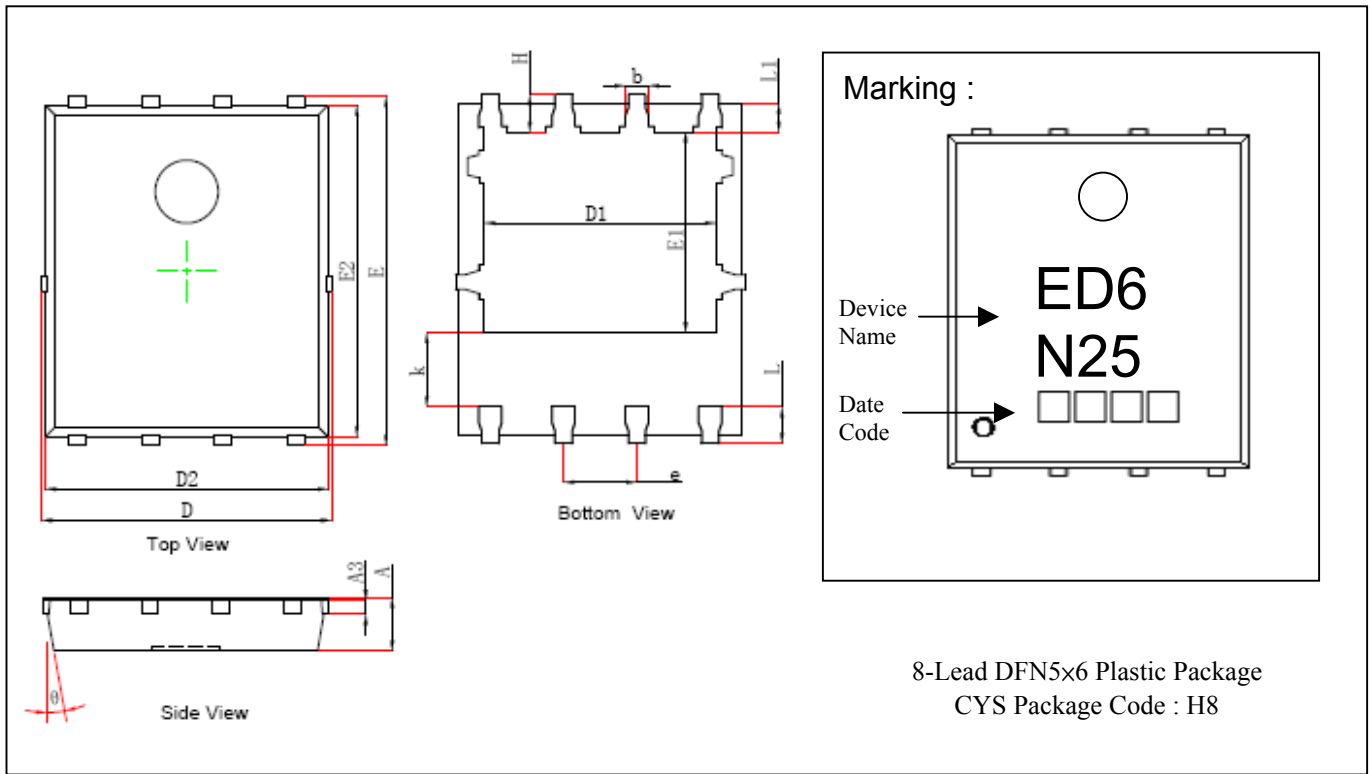
**Recommended temperature profile for IR reflow**



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

**DFN5x6 Dimension**



DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039	k	1.190	1.390	0.047	0.055
A3	0.254	REF	0.010	REF	b	0.350	0.450	0.014	0.018
D	4.944	5.096	0.195	0.201	e	1.270	TYP.	0.050	TYP.
E	5.974	6.126	0.235	0.241	L	0.559	0.711	0.022	0.028
D1	3.910	4.110	0.154	0.162	L1	0.424	0.576	0.017	0.023
E1	3.375	3.575	0.133	0.141	H	0.574	0.726	0.023	0.029
D2	4.824	4.976	0.190	0.196	θ	10°	12°	10°	12°
E2	5.674	5.826	0.223	0.229					

**Notes:** 1.Controlling dimension: millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

**Important Notice:**

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.