

# P-Channel Enhancement Mode MOSFET

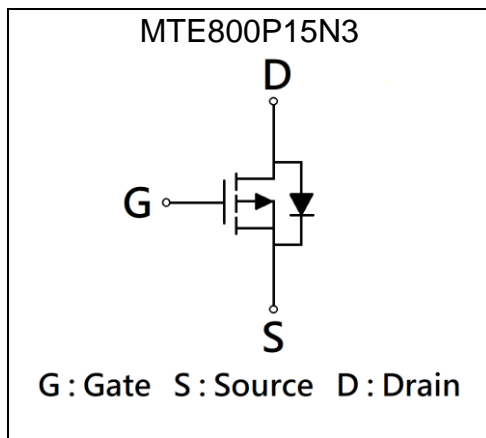
## MTE800P15N3

### Features

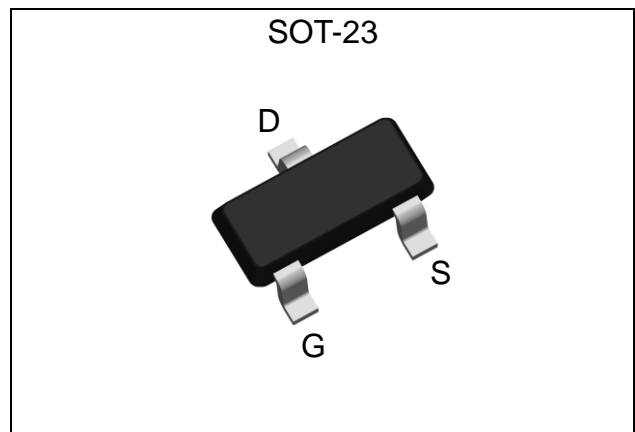
- Advanced trench process technology
- High density cell design for ultra low on resistance
- Pb-free lead plating and halogen-free package

$BV_{DSS}$	-150V	
$I_D @ V_{GS}=-10V, T_A=25^{\circ}C$	-0.77A	
$R_{DSON(TYP)}$	$V_{GS}=-10V, I_D=-0.5A$	$0.8\Omega$

### Equivalent Circuit

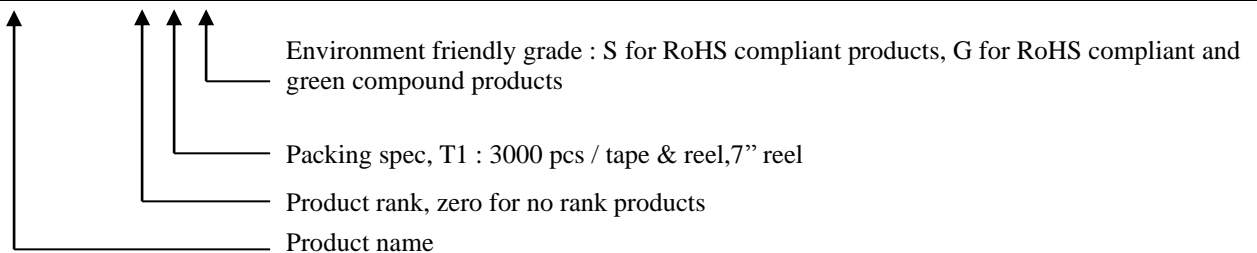


### Outline



### Ordering Information

Device	Package	Shipping
MTE800P15N3-0-T1-G	SOT-23 (Pb-free lead plating and halogen-free package)	3000 pcs / tape & reel





**Absolute Maximum Ratings (Ta=25°C)**

Parameter	Symbol	Limits	Unit	
Drain-Source Voltage	V <sub>DS</sub>	-150	V	
Gate-Source Voltage	V <sub>GS</sub>	±20		
Continuous Drain Current @ V <sub>GS</sub> =-10V	I <sub>D</sub>	T <sub>A</sub> =25°C	-0.77 (Note 4)	A
		T <sub>A</sub> =70°C	-0.62 (Note 4)	
Pulsed Drain Current	I <sub>DM</sub>	-3.2		
Maximum Power Dissipation	P <sub>D</sub>	T <sub>A</sub> =25°C	1.25	W
		T <sub>A</sub> =70°C	0.8	
Operating Junction and Storage Temperature	T <sub>j</sub> , T <sub>stg</sub>	-55~+150	°C	

**Thermal Performance**

Parameter	Symbol	Limit	Unit
Thermal Resistance, Junction-to-Case , max	R <sub>θJC</sub>	50	°C/W
Thermal Resistance, Junction-to-Ambient , max (Note 4)	R <sub>θJA</sub>	100	

Note : 1. Pulse width limited by maximum junction temperature.

2. Pulse width ≤ 300μs, duty cycle ≤ 2%

3. Human body model, 1.5kΩ in series with 100pF.

4. Surface mounted on 1 in<sup>2</sup> copper pad of FR-4 board, t ≤ 5s; 120°C/W at steady state; 417°C/W when mounted on minimum copper pad.

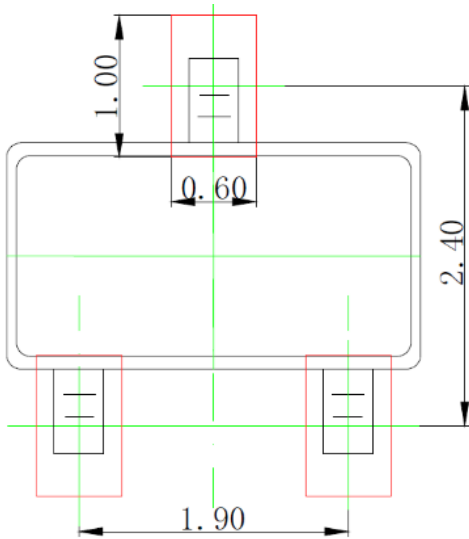
**Electrical Characteristics (T<sub>j</sub>=25°C, unless otherwise specified)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
<b>Static</b>					
BV <sub>DSS</sub>	-150	-	-	V	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA
V <sub>GS(th)</sub>	-2.0	-	-4.0		V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA
I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V
I <sub>DSS</sub>	-	-	-1	μA	V <sub>DS</sub> =-120V, V <sub>GS</sub> =0V
*R <sub>DS(ON)</sub>	-	0.8	1.15	Ω	V <sub>GS</sub> =-10V, I <sub>D</sub> =-0.5A
*G <sub>FS</sub>	-	1.6	-	S	V <sub>DS</sub> =-10V, I <sub>D</sub> =-0.5A
<b>Dynamic</b>					
C <sub>iss</sub>	-	283	-	pF	V <sub>DS</sub> =-75V, V <sub>GS</sub> =0V, f=1MHz
C <sub>oss</sub>	-	21	-		
C <sub>rss</sub>	-	21	-		
*t <sub>d(ON)</sub>	-	7	-	ns	V <sub>DS</sub> =-75V, I <sub>D</sub> =-0.5A, V <sub>GS</sub> =-10V, R <sub>G</sub> =6Ω
*t <sub>r</sub>	-	16.5	-		
*t <sub>d(OFF)</sub>	-	17.5	-		
*t <sub>f</sub>	-	17.8	-		

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
*Qg	-	6.8	-	nC	V <sub>DS</sub> =-75V, I <sub>D</sub> =-0.5A, V <sub>GS</sub> =-10V
*Qgs	-	1.6	-		
*Qgd	-	1.7	-		
Rg	-	5.6	-	Ω	f=1MHz
<b>Source-Drain Diode</b>					
I <sub>S</sub>	-	-	-0.77	A	
I <sub>SM</sub>	-	-	-3.2		
*V <sub>SD</sub>	-	-0.81	-1.2	V	V <sub>GS</sub> =0V, I <sub>S</sub> =-1A
*trr	-	26.6	-	ns	I <sub>F</sub> =-0.5A, V <sub>GS</sub> =0V, dI <sub>F</sub> /dt=100A/μs
*Qrr	-	25	-	nC	

\*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

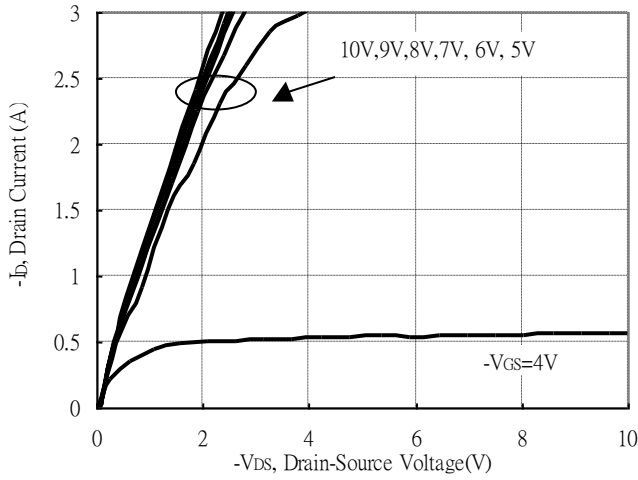
**Recommended Soldering Footprint**



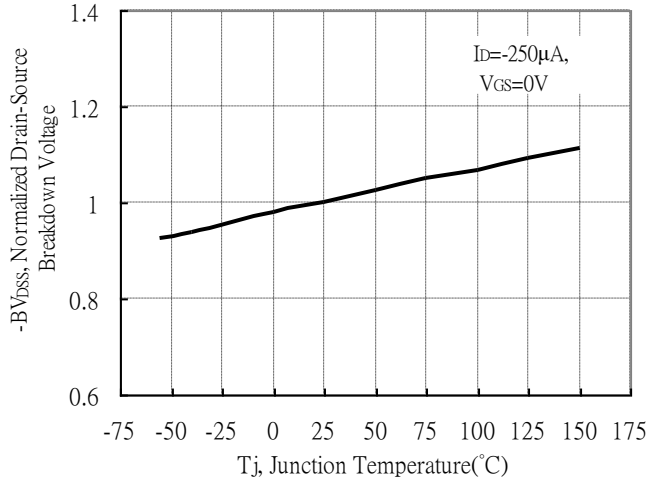
Unit : mm

**Typical Characteristics**

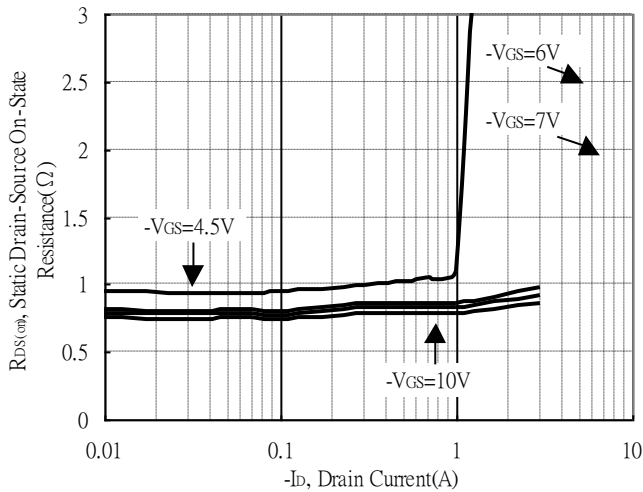
Typical Output Characteristics



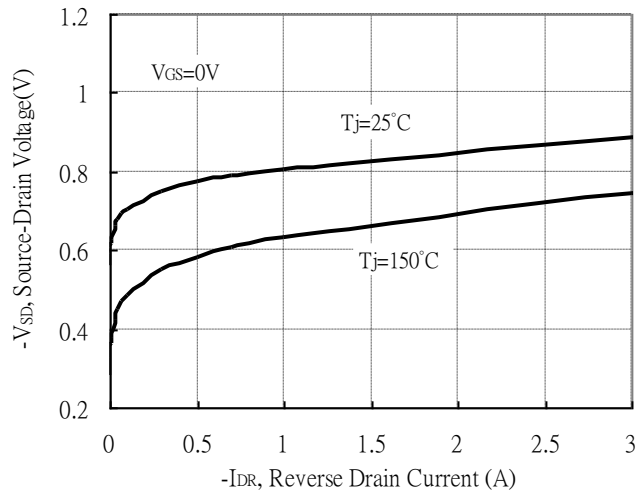
Breakdown Voltage vs Ambient Temperature



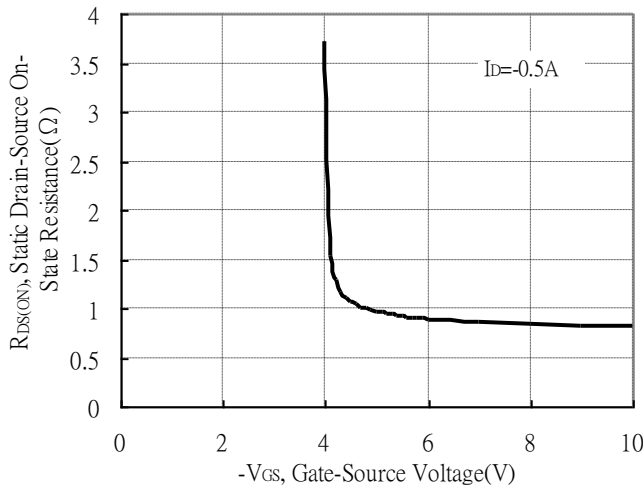
Static Drain-Source On-State resistance vs Drain Current



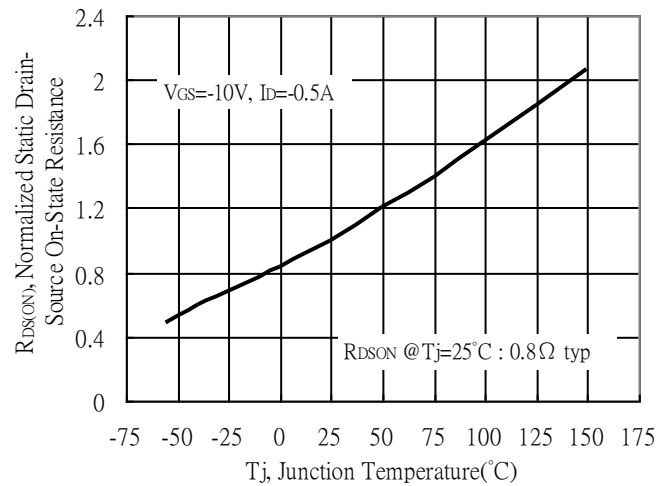
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

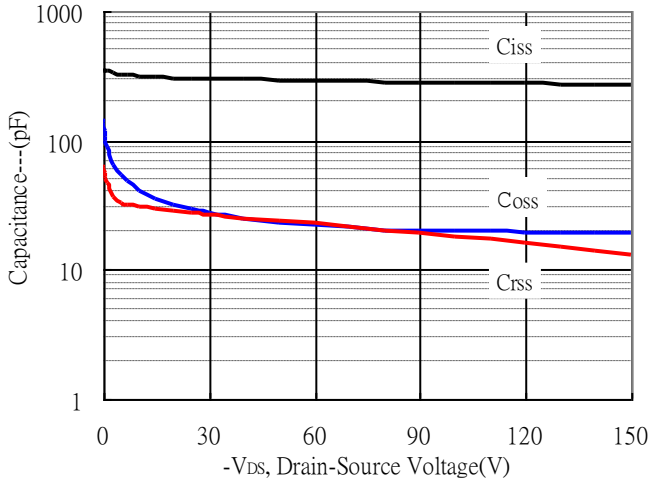


Drain-Source On-State Resistance vs Junction Temperature

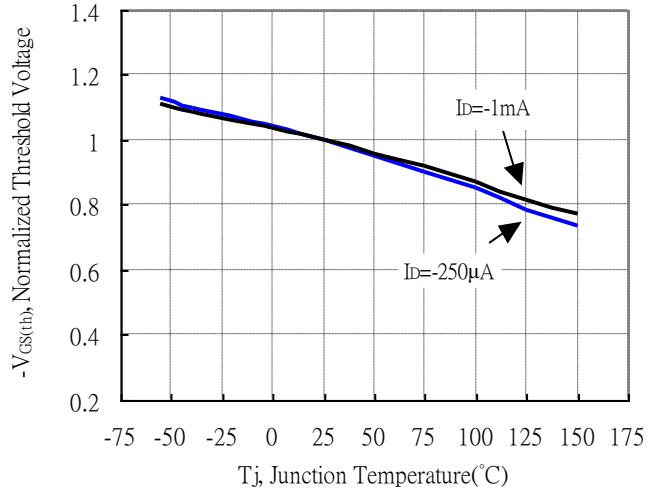


## Typical Characteristics (Cont.)

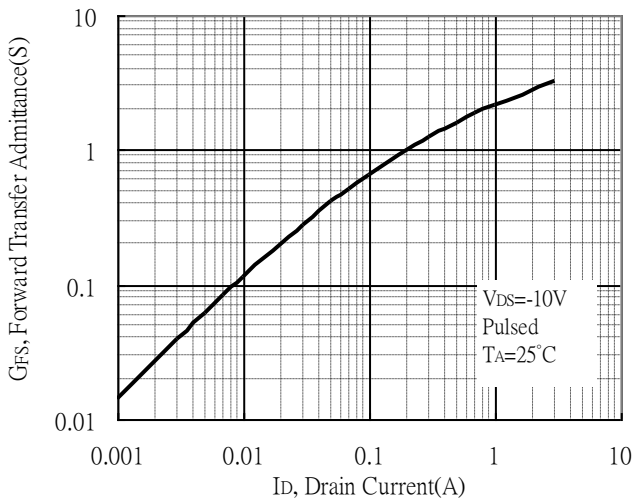
Capacitance vs Drain-to-Source Voltage



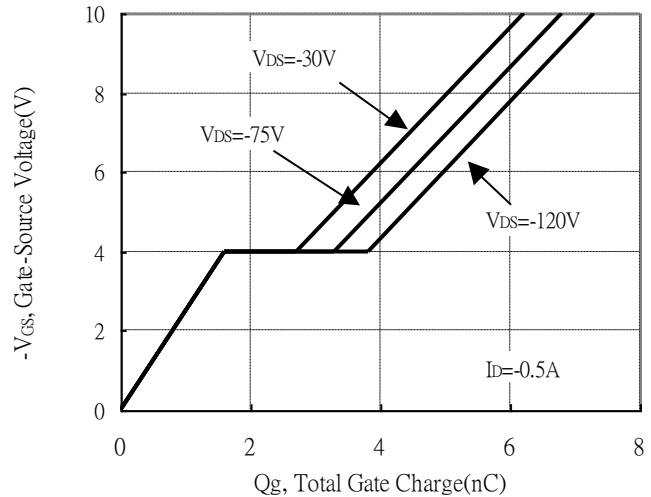
Threshold Voltage vs Junction Temperature



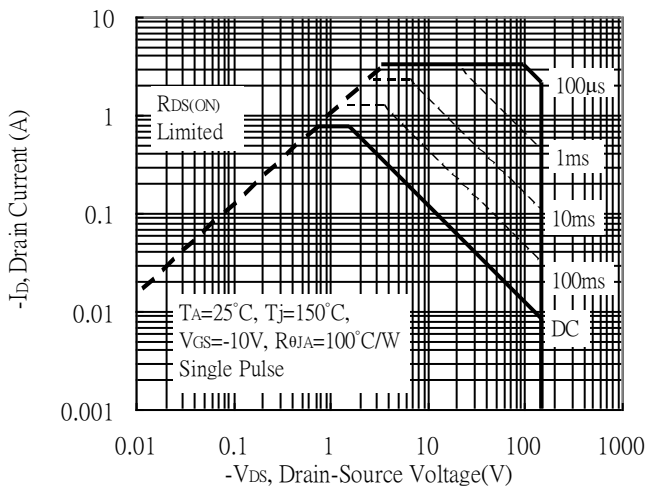
Forward Transfer Admittance vs Drain Current



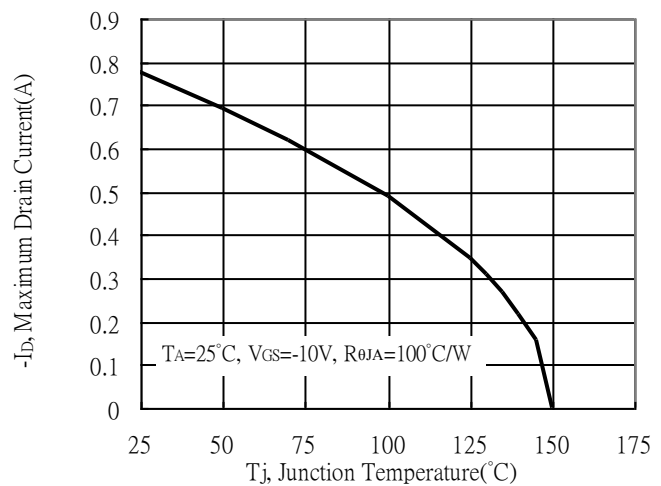
Gate Charge Characteristics



Maximum Safe Operating Area

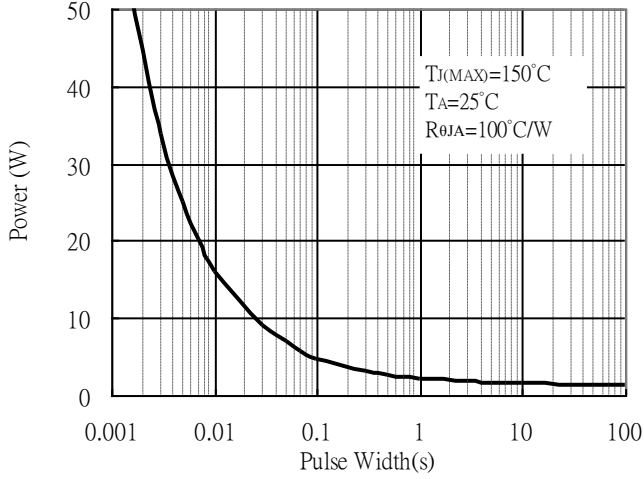


Maximum Drain Current vs Junction Temperature

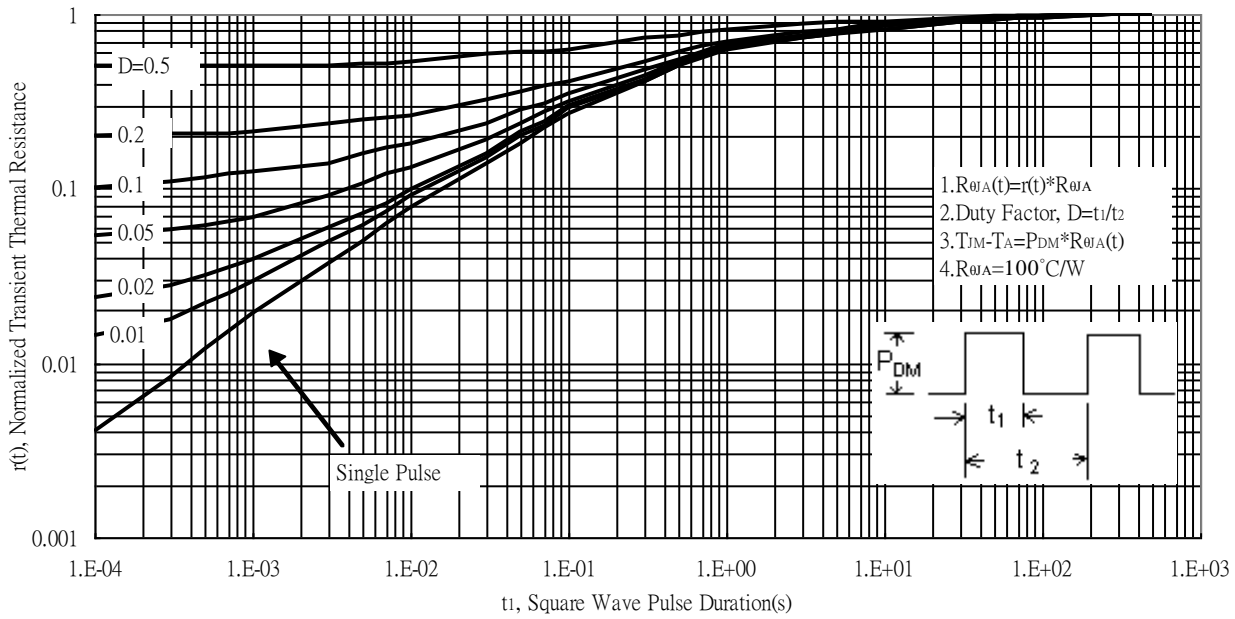


**Typical Characteristics (Cont.)**

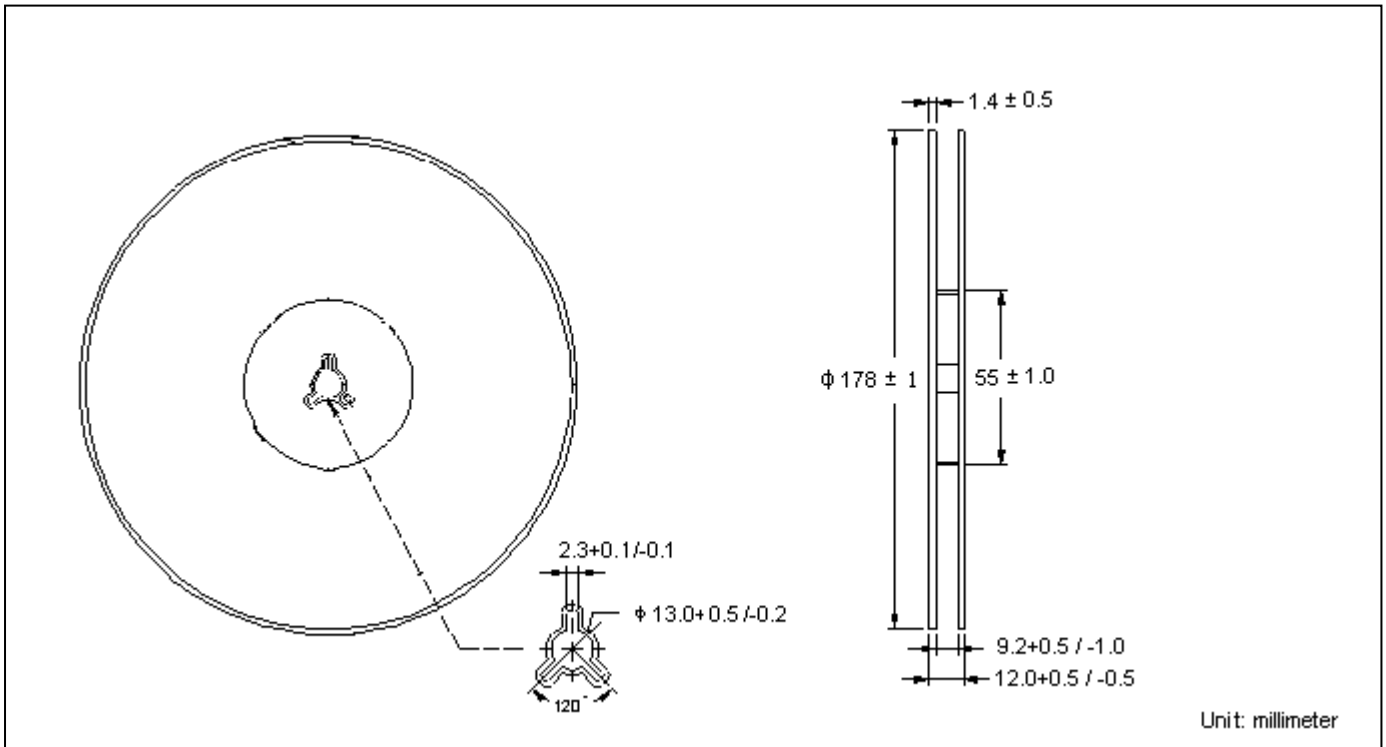
Single Pulse Power Rating, Junction to Ambient  
 (Note on page 2)



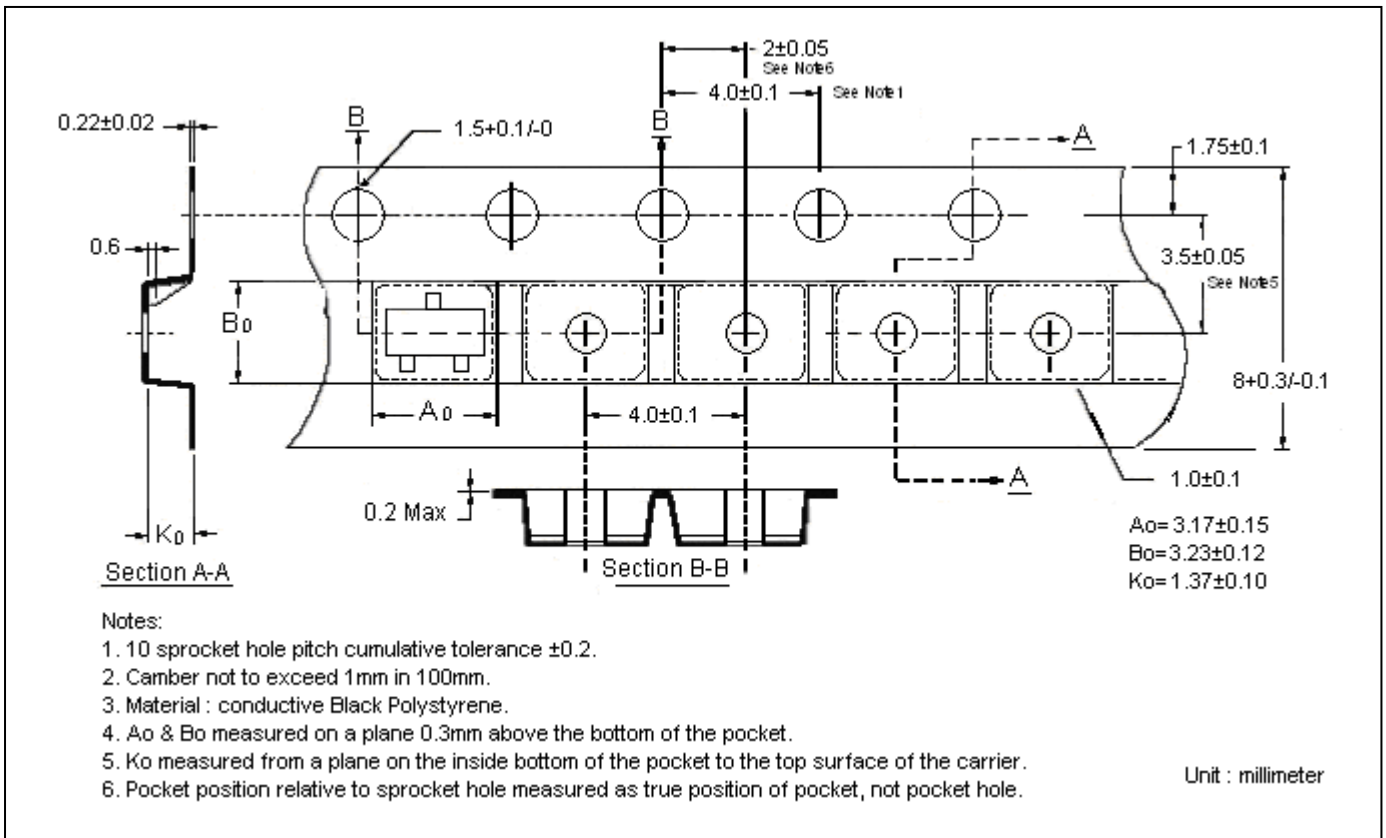
Transient Thermal Response Curves



**Reel Dimension**



**Carrier Tape Dimension**



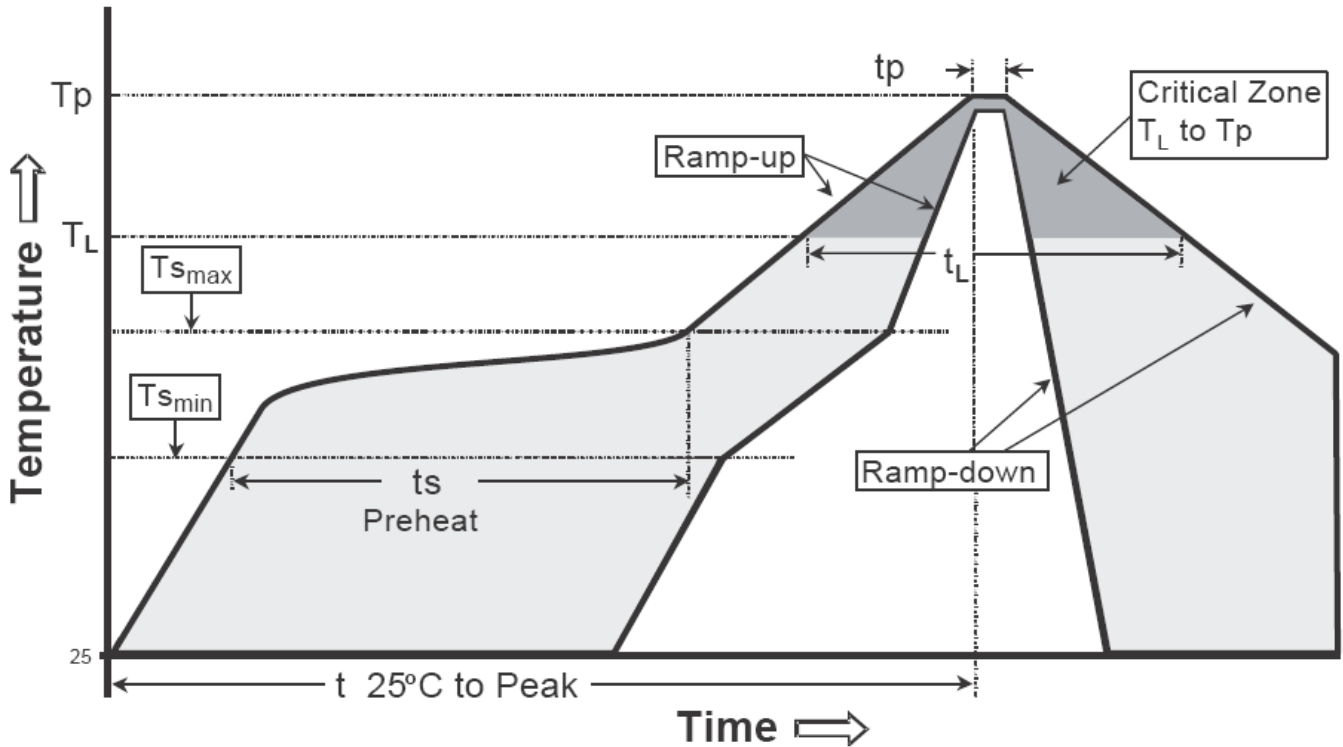
**Notes:**

1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.2$ .
2. Camber not to exceed 1mm in 100mm.
3. Material : conductive Black Polystyrene.
4.  $A_0$  &  $B_0$  measured on a plane 0.3mm above the bottom of the pocket.
5.  $K_0$  measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

**Recommended temperature profile for IR reflow**

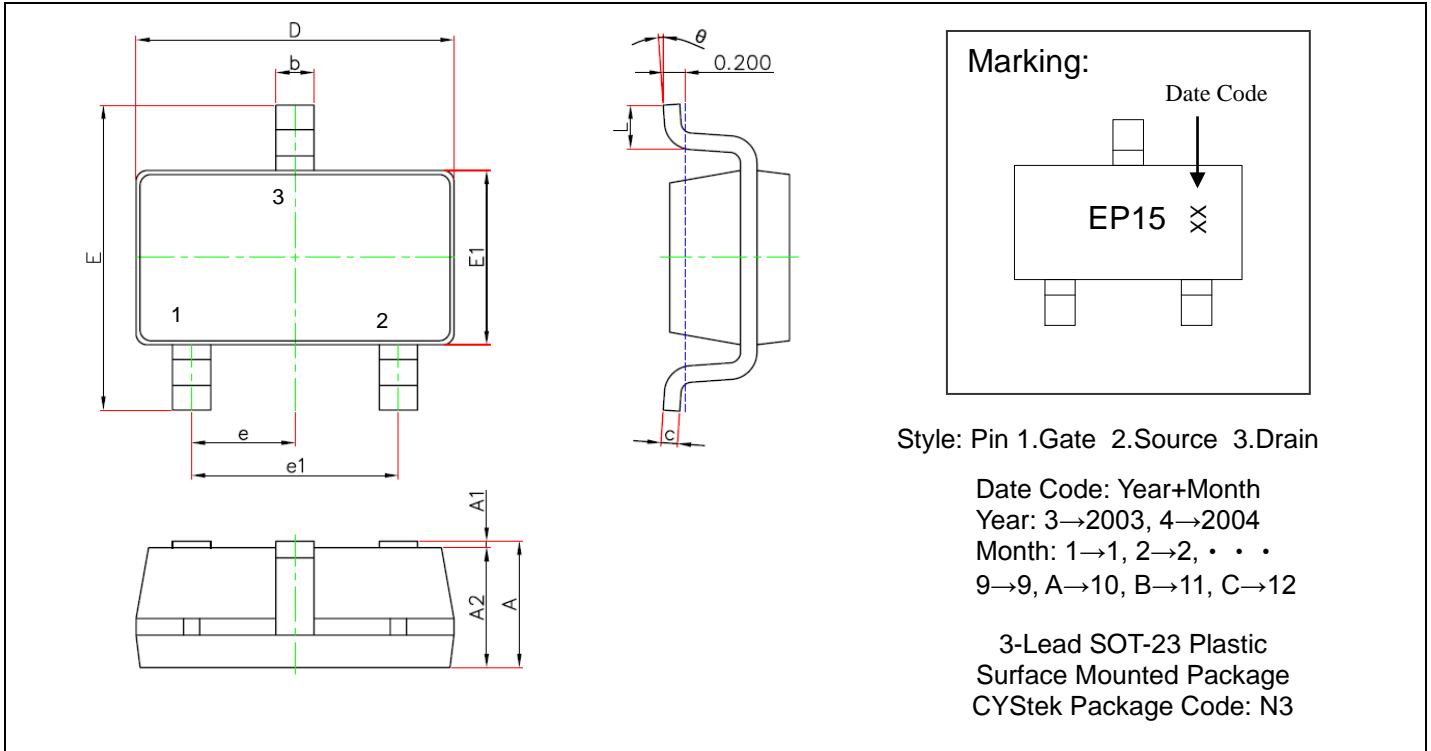


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (Tl)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.



**SOT-23 Dimension**



**Marking:**

Date Code

EP15 x x

Style: Pin 1.Gate 2.Source 3.Drain

Date Code: Year+Month  
 Year: 3→2003, 4→2004  
 Month: 1→1, 2→2, . . .  
 9→9, A→10, B→11, C→12

3-Lead SOT-23 Plastic  
 Surface Mounted Package  
 CYStek Package Code: N3

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.041	0.049	1.05	1.25	E1	0.059	0.067	1.50	1.70
A1	0.000	0.004	0.00	0.10	E	0.104	0.116	2.65	2.95
A2	0.041	0.045	1.05	1.15	e	0.037 BSC		0.95 BSC	
b	0.012	0.020	0.30	0.50	e1	0.071	0.079	1.80	2.00
c	0.004	0.008	0.10	0.20	L	0.012	0.024	0.30	0.60
D	0.111	0.119	2.82	3.02	θ	0°	8°	0°	8°

Notes: 1.Controlling dimension: millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

**Important Notice:**

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.