

Dual N-Channel Enhancement Mode Power MOSFET

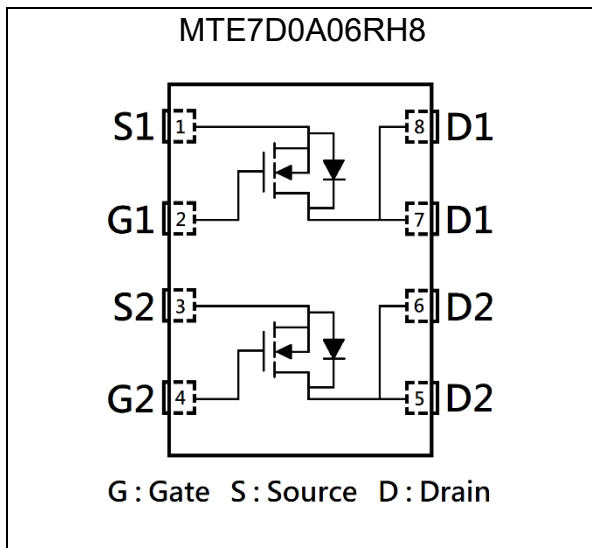
MTE7D0A06RH8

Features

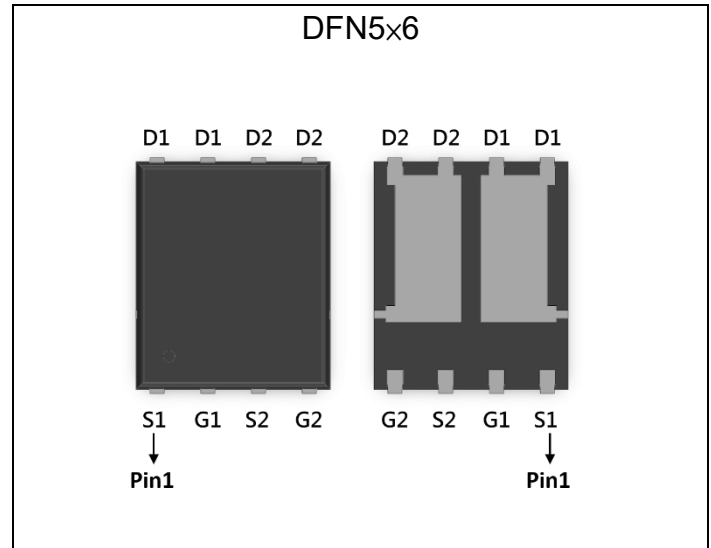
- Low On Resistance
- Low Gate Charge
- Fast Switching Characteristic

BV_{DSS}	60V
$I_D@V_{GS}=10V, T_C=25^\circ C$	20A
$I_D@V_{GS}=10V, T_A=25^\circ C$	12A
$R_{DS(ON) typ. @ V_{GS}=10V, I_D=10A}$	7mΩ

Equivalent Circuit

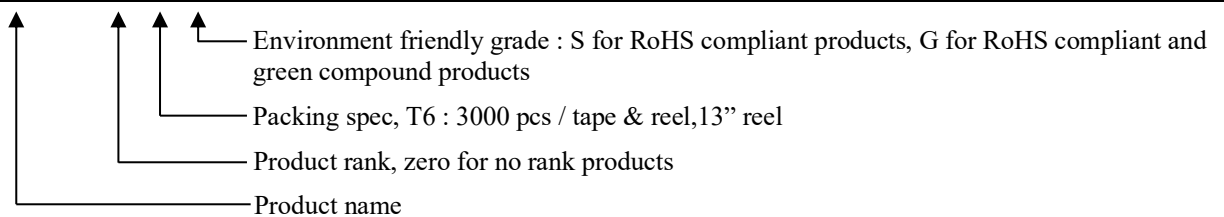


Outline



Ordering Information

Device	Package	Shipping
MTE7D0A06RH8-0-T6-G	DFN5x6 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel



**Absolute Maximum Ratings (T_A=25°C)**

Parameter	Symbol	Limits	Unit	
Drain-Source Voltage	V _{DS}	60	V	
Gate-Source Voltage	V _{GS}	±20		
Continuous Drain Current @ V _{GS} =10V, T _C =25°C (silicon limit) *a	I _D	45	A	
Continuous Drain Current @ V _{GS} =10V, T _C =25°C (package limit) *a		20		
Continuous Drain Current @ V _{GS} =10V, T _C =100°C *a		20		
Continuous Drain Current @ V _{GS} =10V, T _A =25°C *b		12		
Continuous Drain Current @ V _{GS} =10V, T _A =70°C *b		9.6		
Pulsed Drain Current *c		I _{DM}		80
Continuous Body Diode Forward Current @ T _C =25°C *a	I _S	20		
Avalanche Current @ L=0.1mH	I _{AS}	15		
Avalanche Energy @ L=0.5mH	E _{AS}	56	mJ	
Total Power Dissipation	P _D	T _C =25°C *a	45	W
		T _C =100°C *a	18	
		T _A =25°C *b	3	
		T _A =70°C *b	2	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55~+150	°C	

Thermal Data

Parameter	Symbol	Steady State	Unit
Thermal Resistance, Junction-to-case	R _{θJC}	2.8	°C/W
Thermal Resistance, Junction-to-ambient *b	R _{θJA}	42	

Note:

- *a. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- *b. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2 oz. copper, in a still air environment with T_A=25°C. The power dissipation P_D is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
- *c. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and low duty cycles to keep initial T_J=25°C.



Electrical Characteristics (T_A=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	60	-	-	V	V _{GS} =0V, I _D =250μA
V _{GS(th)}	2	-	4		V _{DS} =V _{GS} , I _D =250μA
G _{FS}	-	10.6	-	S	V _{DS} =10V, I _D =10A
I _{GSS}	-	-	±100	nA	V _{GS} =±20V, V _{DS} =0V
I _{DSS}	-	-	1	μA	V _{DS} =48V, V _{GS} =0V
R _{DS(on)}	-	7	10	mΩ	V _{GS} =10V, I _D =10A
Dynamic					
C _{iss}	-	1520	-	pF	V _{DS} =30V, V _{GS} =0V, f=1MHz
C _{oss}	-	326	-		
C _{rss}	-	33	-		
R _g	-	2.8	-	Ω	f=1MHz
Q _g *1, 2	-	22	-	nC	V _{DS} =30V, I _D =10A, V _{GS} =10V
Q _{gs} *1, 2	-	8	-		
Q _{gd} *1, 2	-	4.5	-		
t _{d(ON)} *1, 2	-	14	-	ns	V _{DS} =30V, I _D =10A, V _{GS} =10V, R _{GS} =1Ω
t _r *1, 2	-	14	-		
t _{d(OFF)} *1, 2	-	28	-		
t _f *1, 2	-	8.3	-		
Source-Drain Diode					
V _{SD} *1	-	0.81	1.2	V	I _S =10A, V _{GS} =0V
t _{rr}	-	22	-	ns	I _F =10A, dI _F /dt=100A/μs
Q _{rr}	-	14	-	nC	

Note:

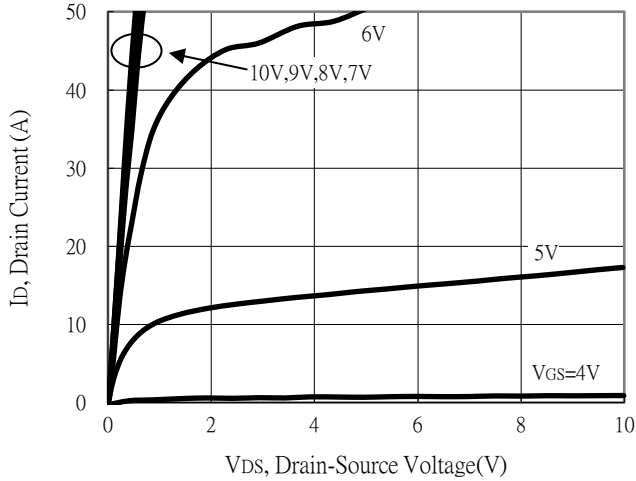
*1. Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

*2. Independent of operating temperature

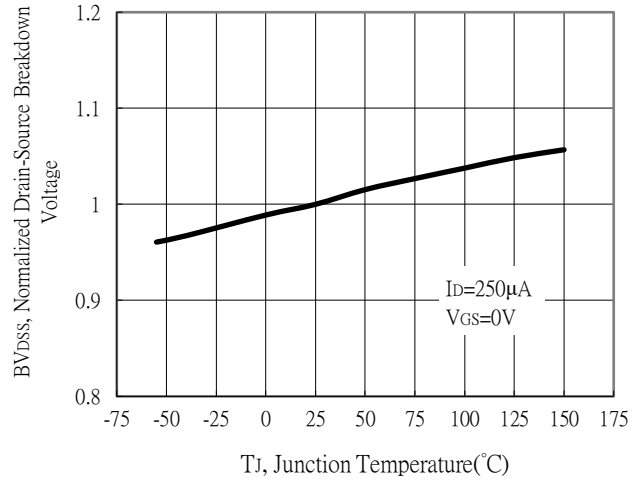


Typical Characteristics

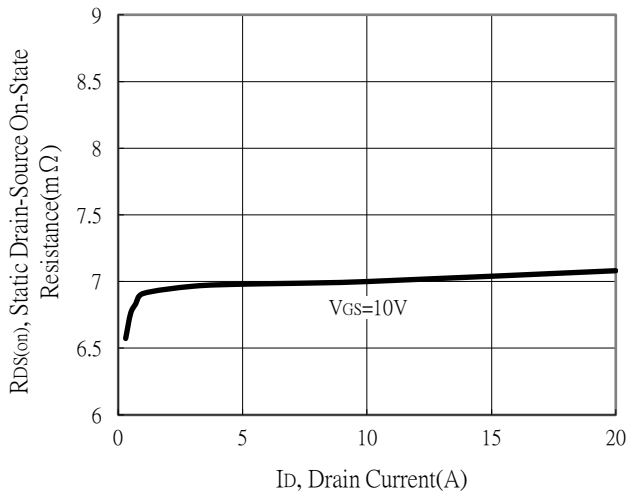
Typical Output Characteristics



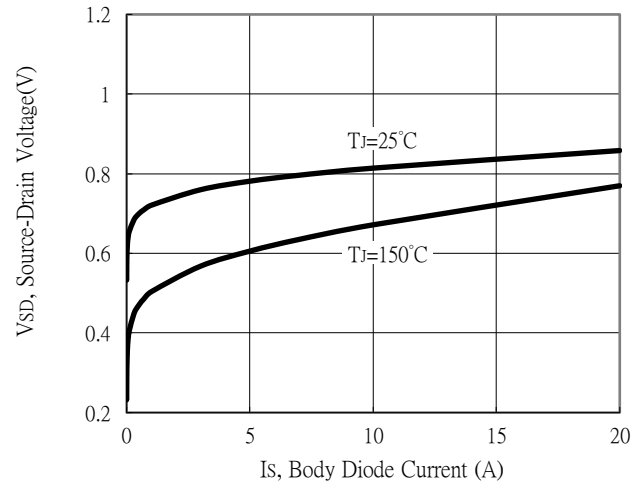
Breakdown Voltage vs Ambient Temperature



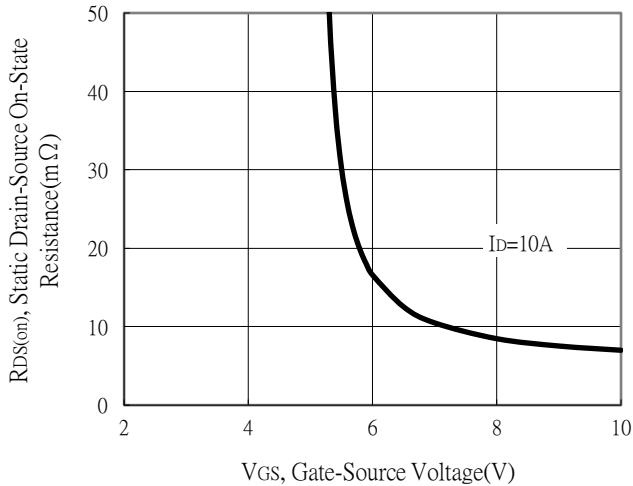
Static Drain-Source On-State resistance vs Drain Current



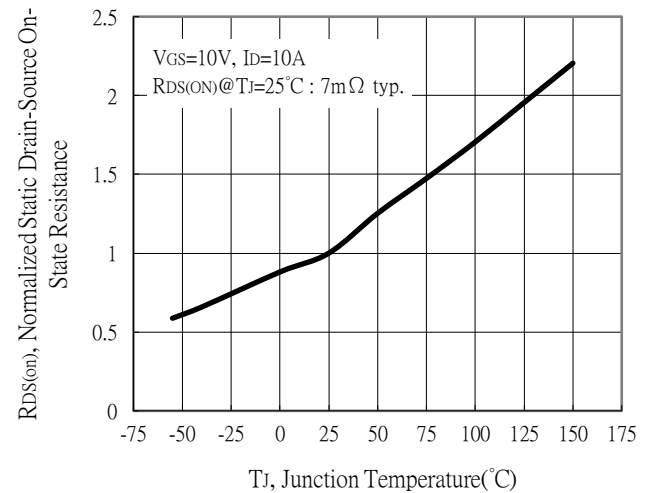
Body Diode Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

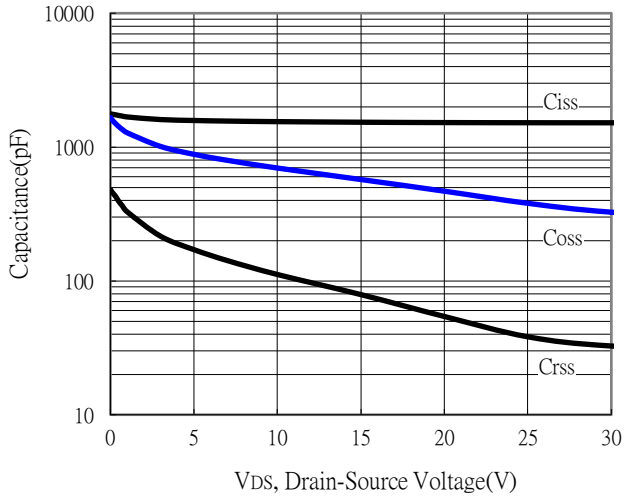


Drain-Source On-State Resistance vs Junction Temperature

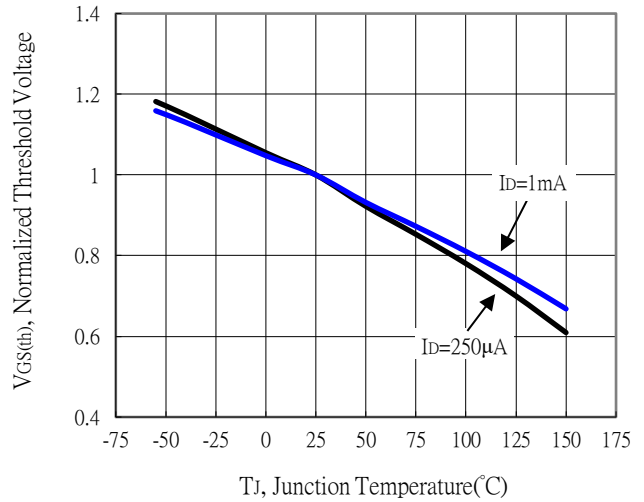


Typical Characteristics (Cont.)

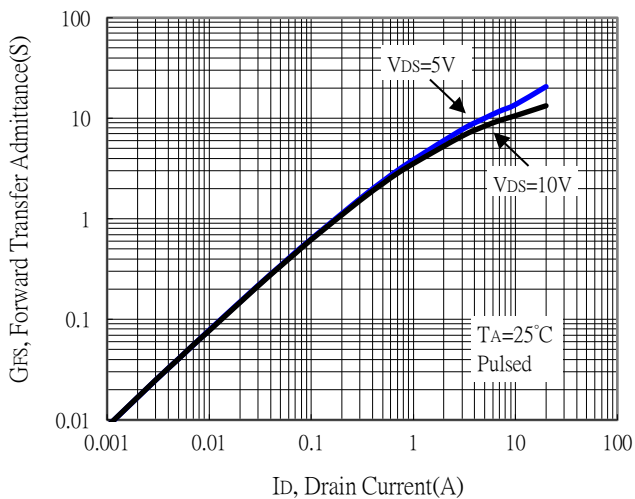
Capacitance vs Drain-to-Source Voltage



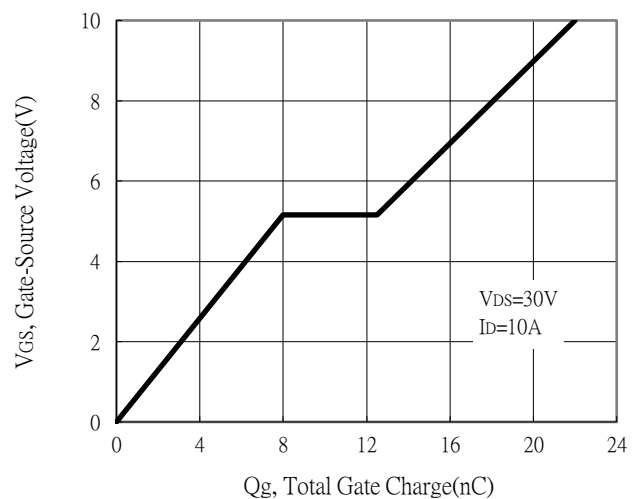
Threshold Voltage vs Junction Temperature



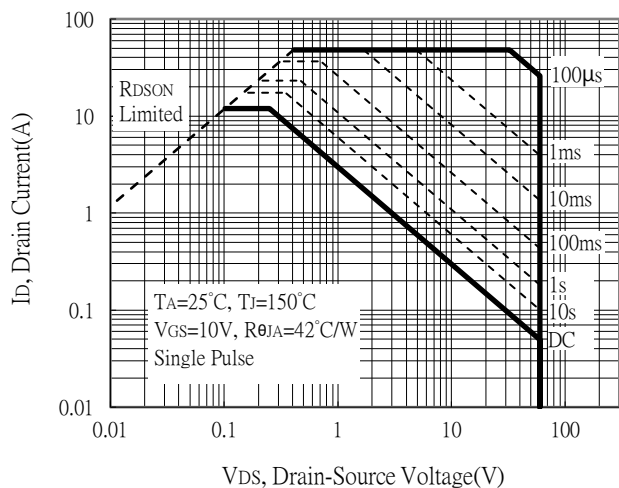
Forward Transfer Admittance vs Drain Current



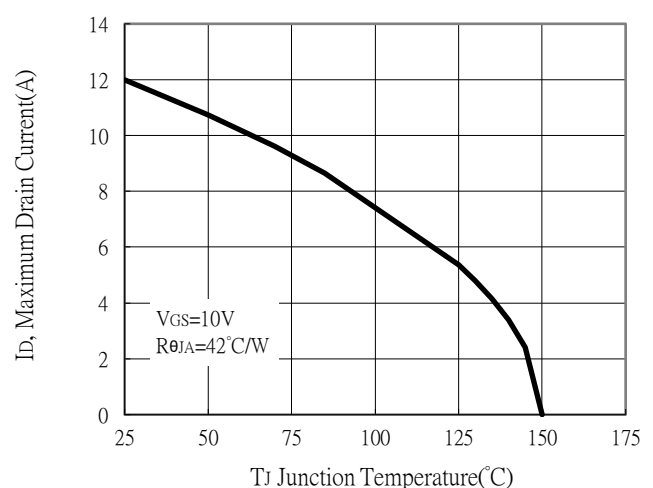
Gate Charge Characteristics



Maximum Safe Operating Area

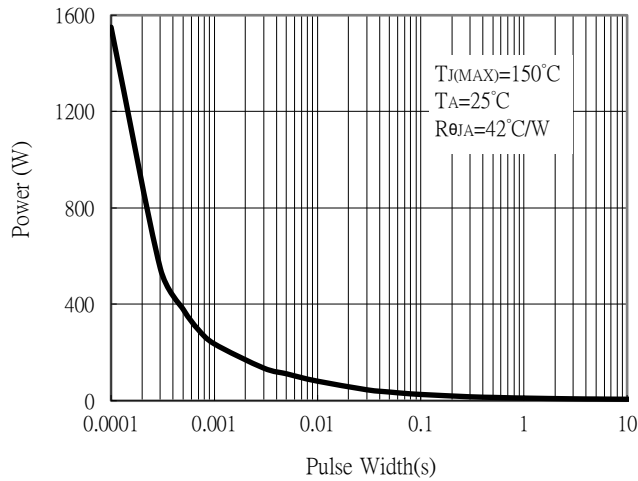


Maximum Drain Current vs Junction Temperature

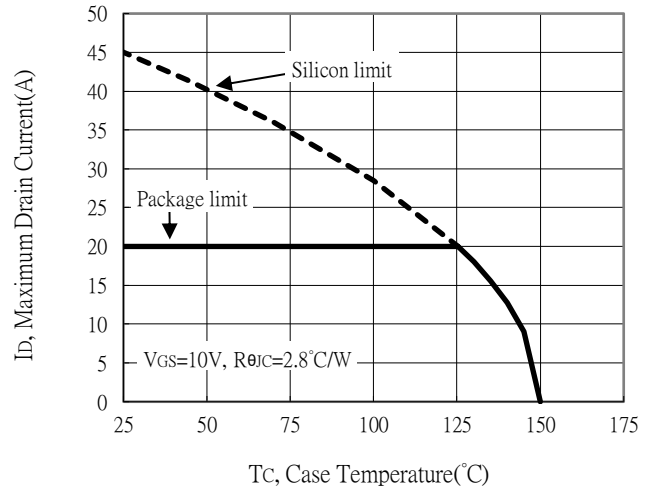


Typical Characteristics (Cont.)

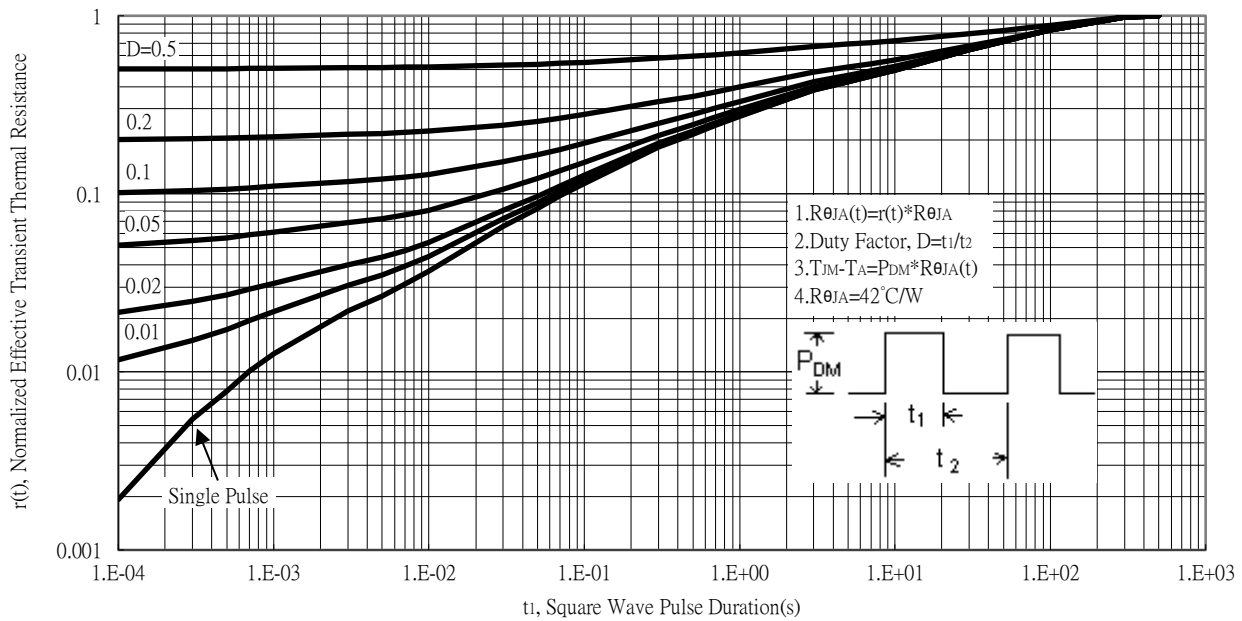
Single Pulse Power Rating, Junction to Ambient



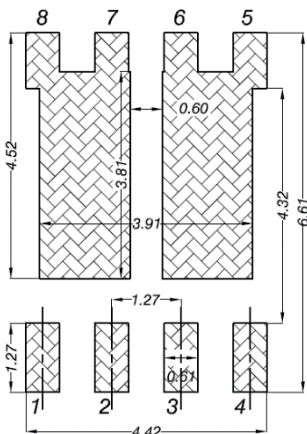
Maximum Drain Current vs Case Temperature



Transient Thermal Response Curves

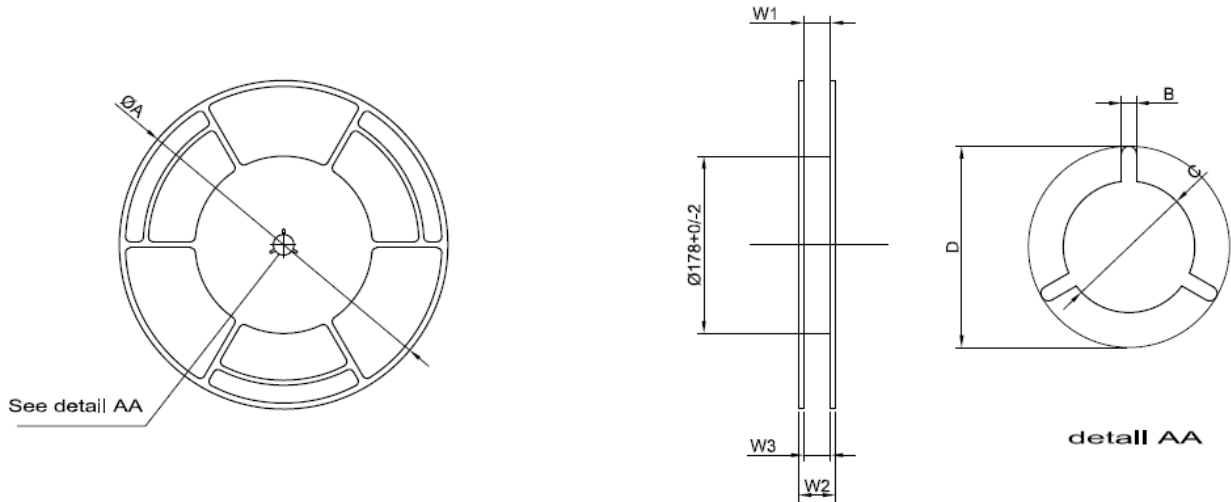


Recommended Soldering Footprint



Unit : mm

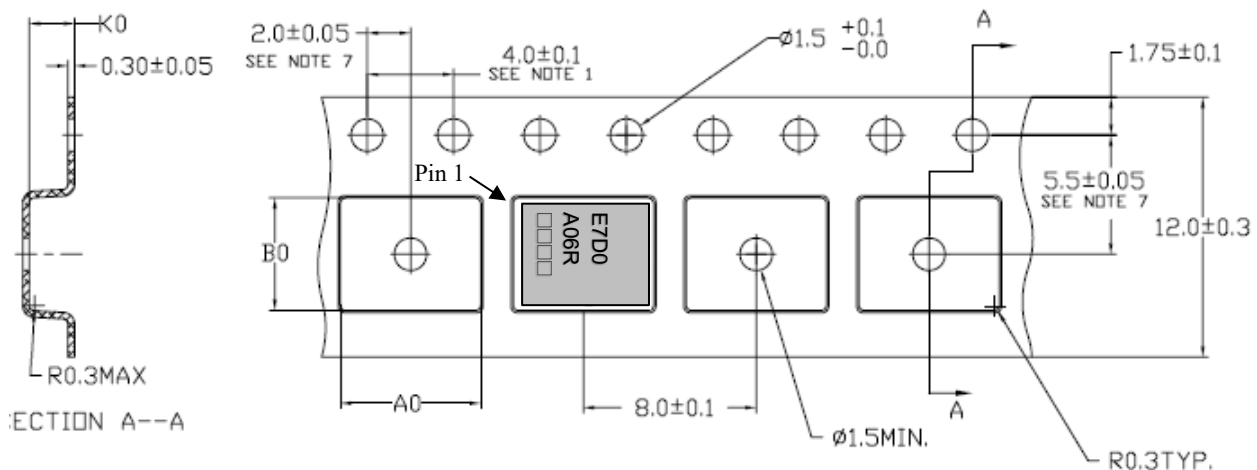
Reel Dimension



TAPE SIZE	A	B	C	D	W1	W2	W3
12mm	330 ± 2.0	2.9 ± 0.5	$13.0 \pm 0.5 / -0$	23 ± 1.0	$12.4 \pm 2 / -0$	18.4 ± 0.5	12~15

Unit : mm

Carrier Tape Dimension



- NOTE:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.2
 2. CAMBER NOT TO EXCEED 1mm IN 100mm, NONCUMULATIVE OVER 250mm.
 3. MATERIAL: BLACK STATIC DISSIPATIVE PS.(POLYSTYRENE)
 4. ALL DIMENSIONS ARE IN MILLIMETERS (UNLESS OTHERWISE SPECIFIED)
 5. $A0$ AND $B0$ MEASURED ON A PLANE 0.3mm ABOVE THE BOTTOM OF THE POCKET
 6. $K0$ MEASURED FROM A PLANE ON THE INSIDE BOTTOM OF THE POCKET TO THE TOP SURFACE OF THE CARRIER
 7. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE
 8. SURFACE RESISTIVITY
 $1 \times 10^4 \sim 1 \times 10^6 \Omega \text{ SQ.}$

Direction of unreeling

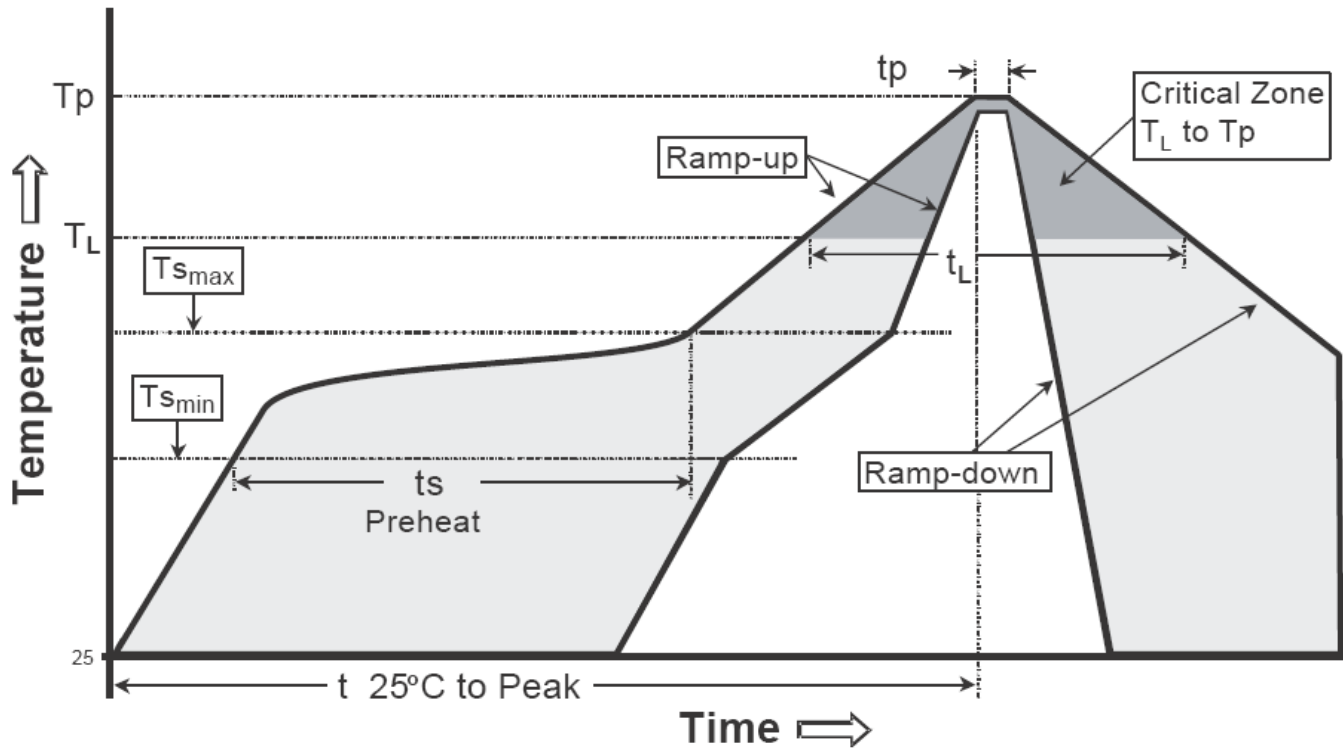
$A0 = 6.5 \pm 0.1$
 $B0 = 5.3 \pm 0.1$
 $K0 = 1.4 \pm 0.1$

Unit : mm

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

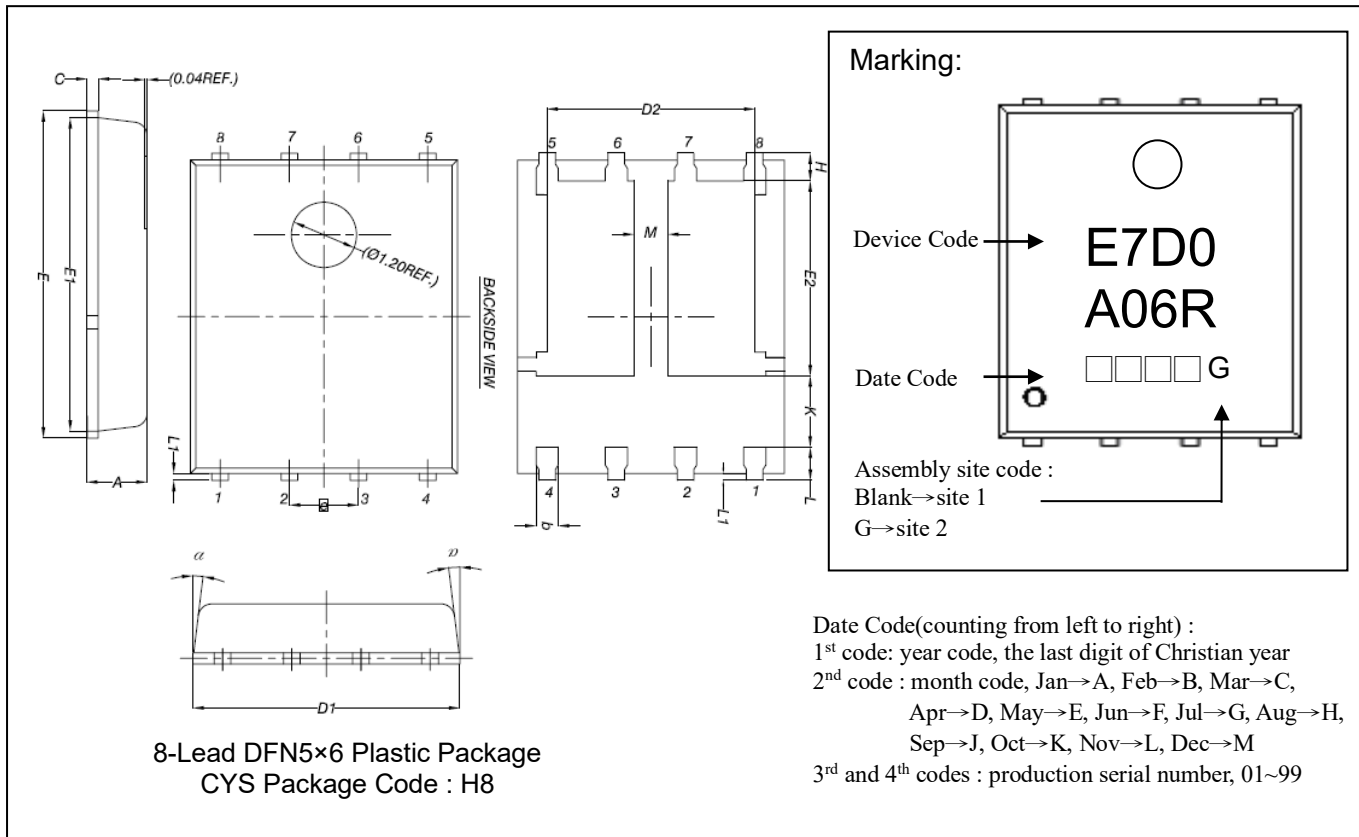
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note :1. All temperatures refer to topside of the package, measured on the package body surface.
 2. For devices mounted on FR-4 PCB of 1.6mm or equivalent grade PCB. If other grade PCB is used, care should be taken to match the coefficients of thermal expansion between components and PCB. If they are not matched well, the solder joints may crack or the bodies of the parts may crack or shatter as the assembly cools.

DFN5x6 Dimension



8-Lead DFN5x6 Plastic Package
 CYS Package Code : H8

Marking:

Device Code → **E7D0**
 Date Code → **A06R**
 Assembly site code :
 Blank → site 1
 G → site 2

Date Code(counting from left to right) :
 1st code: year code, the last digit of Christian year
 2nd code : month code, Jan→A, Feb→B, Mar→C,
 Apr→D, May→E, Jun→F, Jul→G, Aug→H,
 Sep→J, Oct→K, Nov→L, Dec→M
 3rd and 4th codes : production serial number, 01~99

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.90	1.10	0.035	0.043	e	1.27 BSC		0.05 BSC	
b	0.33	0.51	0.012	0.020	H	0.41	0.61	0.016	0.024
C	0.20	0.30	0.007	0.011	K	1.10	-	0.043	-
D1	4.80	5.00	0.188	0.196	L	0.51	0.71	0.020	0.027
D2	3.61	3.96	0.142	0.155	L1	0.06	0.20	0.002	0.007
E	5.90	6.10	0.232	0.240	M	0.50	-	0.019	-
E1	5.70	5.80	0.224	0.228	α	0°	12°	0°	12°
E2	3.38	3.78	0.133	0.148					

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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