

N-Channel Enhancement Mode Power MOSFET

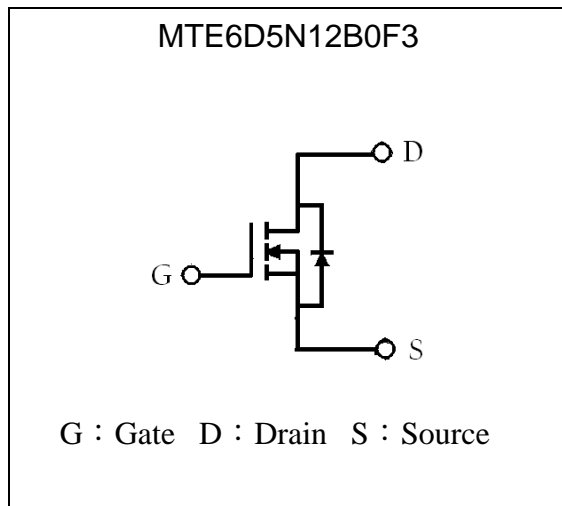
MTE6D5N12B0F3

BV_{DSS}	120V
I_D@V_{GS}=10V, T_C=25°C	112A
I_D@V_{GS}=10V, T_A=25°C	9.3A
R_{DS(ON)}@V_{GS}=10V, I_D=50A	8.1mΩ (typ)

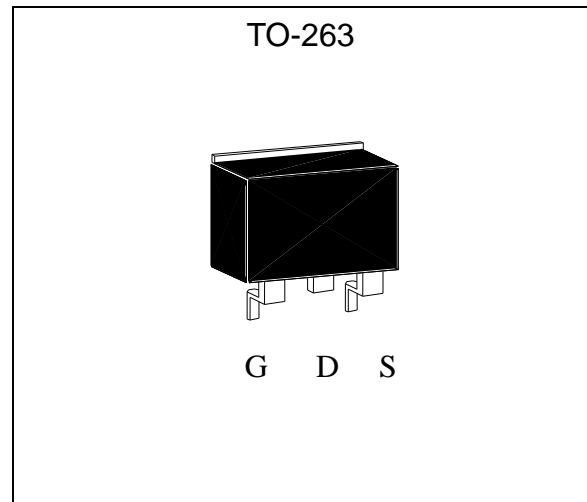
Features

- Low On Resistance
- Simple Drive Requirement
- Low Gate Charge
- Fast Switching Characteristic
- RoHS compliant package

Symbol

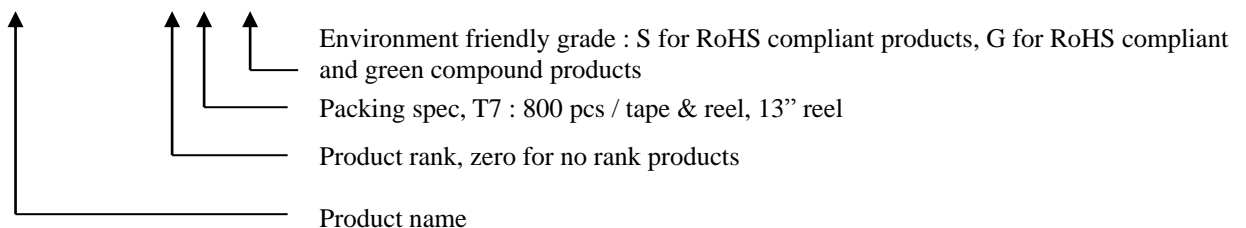


Outline



Ordering Information

Device	Package	Shipping
MTE6D5N12B0F3-0-T7-X	TO-263 (Pb-free lead plating and RoHS compliant package)	800 pcs / Tape & Reel



**Absolute Maximum Ratings** ($T_C=25^{\circ}\text{C}$)

Parameter	Symbol	Limits	Unit	
Drain-Source Voltage (Note 1)	V_{DS}	120	V	
Gate-Source Voltage	V_{GS}	± 30		
Continuous Drain Current @ $T_C=25^{\circ}\text{C}$, $V_{GS}=10\text{V}$ (Note 1)	I_D	112	A	
Continuous Drain Current @ $T_C=100^{\circ}\text{C}$, $V_{GS}=10\text{V}$ (Note 1)		79.2		
Continuous Drain Current @ $T_A=25^{\circ}\text{C}$, $V_{GS}=10\text{V}$ (Note 2)	I_{DSM}	9.3		
Continuous Drain Current @ $T_A=70^{\circ}\text{C}$, $V_{GS}=10\text{V}$ (Note 2)		7.4		
Pulsed Drain Current @ $V_{GS}=10\text{V}$	I_{DM}	380		
Avalanche Current @ $L=0.1\text{mH}$	I_{AS}	25		
Single Pulse Avalanche Energy @ $L=1\text{mH}$, $I_D=20\text{Amps}$, $V_{DD}=25\text{V}$ (Note 4)	E_{AS}	200	mJ	
Repetitive Avalanche Energy (Note 3)	E_{AR}	33		
Power Dissipation	P_D	$T_C=25^{\circ}\text{C}$ (Note 1)	333	W
		$T_C=100^{\circ}\text{C}$ (Note 1)	167	
	P_{DSM}	$T_A=25^{\circ}\text{C}$ (Note 2)	2	
		$T_A=70^{\circ}\text{C}$ (Note 2)	1.3	
Maximum Temperature for Soldering @ Lead at 0.063 in(1.6mm) from case for 10 seconds	T_L	300	$^{\circ}\text{C}$	
Maximum Temperature for Soldering @ Package Body for 10 seconds	T_{PKG}	260		
Operating Junction and Storage Temperature	T_j, T_{stg}	-55~+175		

*Drain current limited by maximum junction temperature

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{\theta JC}$	0.45	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-ambient, max (Note 2)	$R_{\theta JA}$	62.5	

Note : 1. The power dissipation P_D is based on $T_{J(MAX)}=175^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

2. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2 oz. copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

3. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=175^{\circ}\text{C}$. Ratings are based on low frequency and low duty cycles to keep initial $T_J=25^{\circ}\text{C}$.

4. 100% tested by condition of $V_{DD}=25\text{V}$, $I_D=10\text{A}$, $L=2\text{mH}$, $V_{GS}=10\text{V}$.

5. The static characteristics are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% maximum.

6. The $R_{\theta JA}$ is the sum of thermal resistance from junction to case $R_{\theta JC}$ and case to ambient



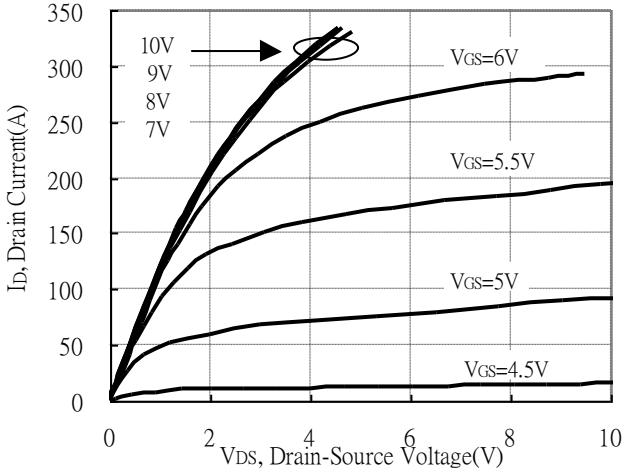
Characteristics (Tj=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	120	-	-	V	V _{GS} =0V, I _D =250μA
ΔBV _{DSS} /ΔT _j	-	130	-	mV/°C	Reference to 25°C, I _D =250μA
V _{GS(th)}	2	-	4	V	V _{DS} = V _{GS} , I _D =250μA
*G _{FS}	-	50	-	S	V _{DS} =5V, I _D =20A
I _{GSS}	-	-	±100	nA	V _{GS} =±30V, V _{DS} =0V
I _{DSS}	-	-	1	μA	V _{DS} =100V, V _{GS} =0V
	-	-	25		V _{DS} =100V, V _{GS} =0V, T _j =125°C
*R _{DS(ON)}	-	8.1	10.6	mΩ	V _{GS} =10V, I _D =50A
Dynamic					
*Q _g	-	143.4	-	nC	V _{DD} =100V, I _D =60A, V _{GS} =10V
*Q _{gs}	-	21.7	-		
*Q _{gd}	-	38.6	-		
*t _{d(ON)}	-	35	-	ns	V _{DD} =60V, I _D =20A, V _{GS} =10V, R _G =3Ω
*t _r	-	39	-		
*t _{d(OFF)}	-	95	-		
*t _f	-	61	-		
C _{iss}	-	5570	-	pF	V _{GS} =0V, V _{DS} =30V, f=1MHz
C _{oss}	-	554	-		
C _{rss}	-	162	-		
R _g	-	1.9	-	Ω	f=1MHz
Source-Drain Diode					
*I _S	-	-	112	A	
*I _{SM}	-	-	380		
*V _{SD}	-	0.83	1.2	V	I _S =50A, V _{GS} =0V
*t _{rr}	-	36	-	ns	V _{GS} =0V, I _F =20A, dI _F /dt=100A/μs
*Q _{rr}	-	142	-	nC	

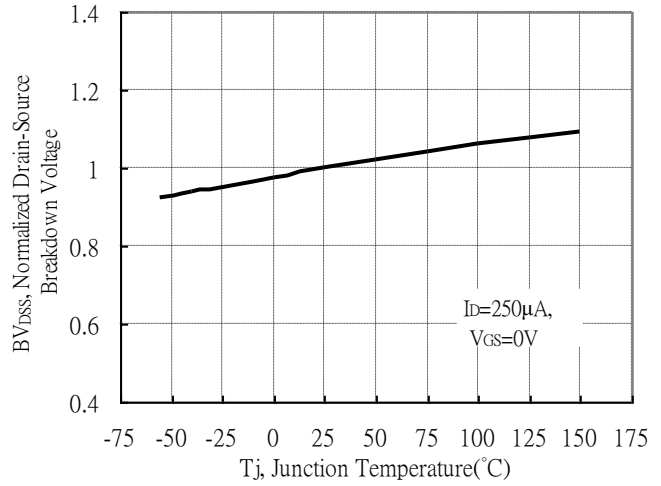
*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Typical Characteristics

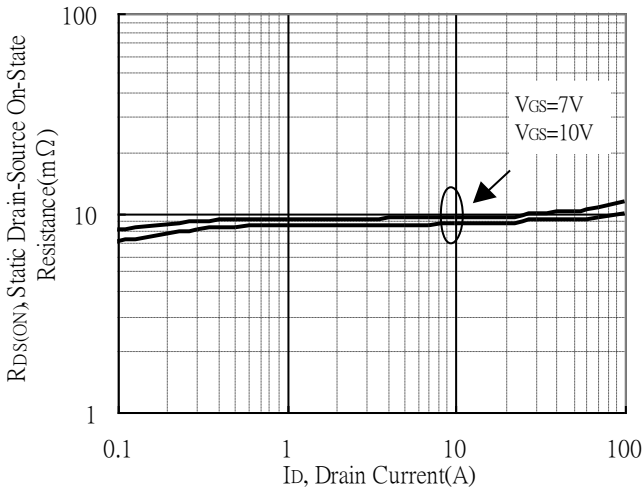
Typical Output Characteristics



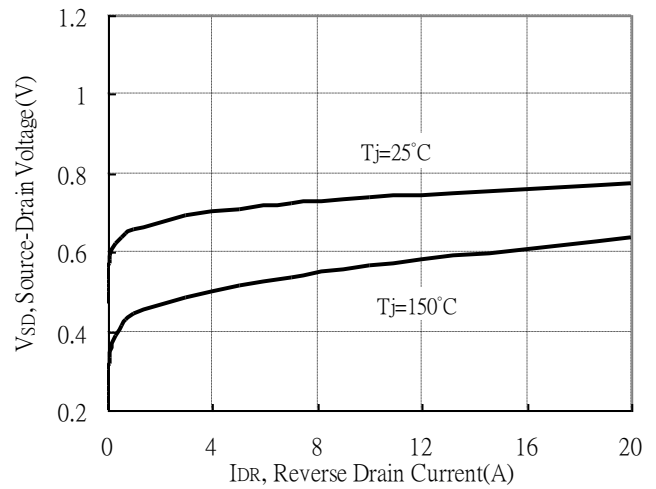
Brekdown Voltage vs Junction Temperature



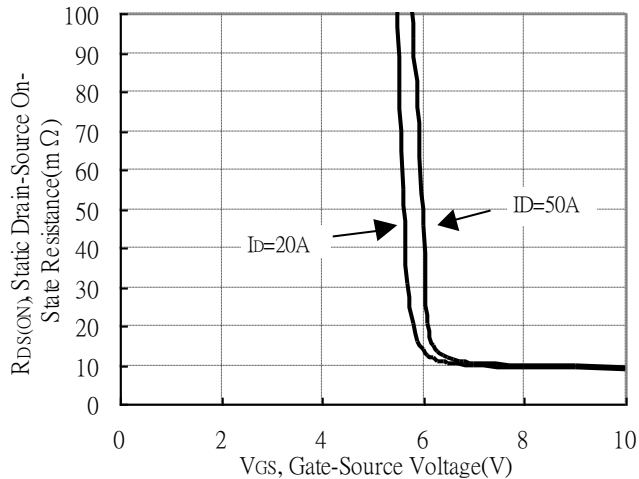
Static Drain-Source On-State resistance vs Drain Current



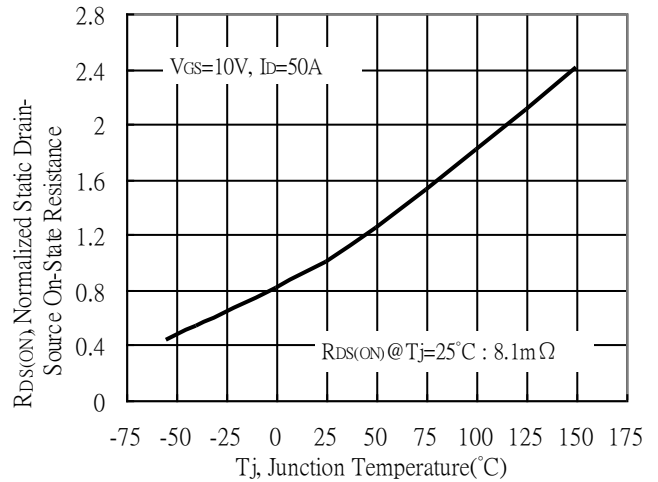
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

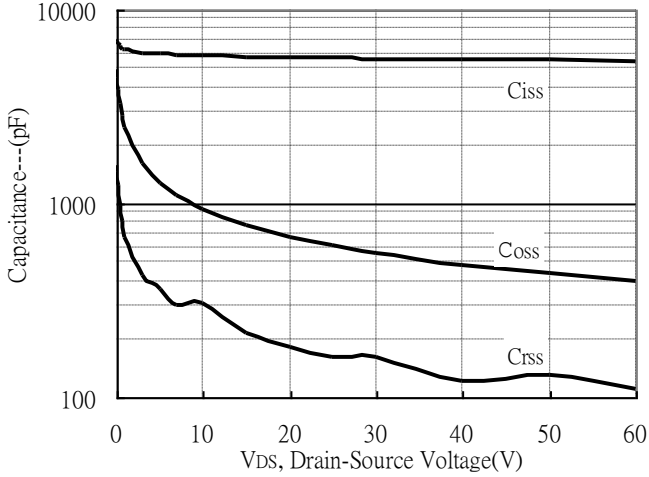


Drain-Source On-State Resistance vs Junction Temperature

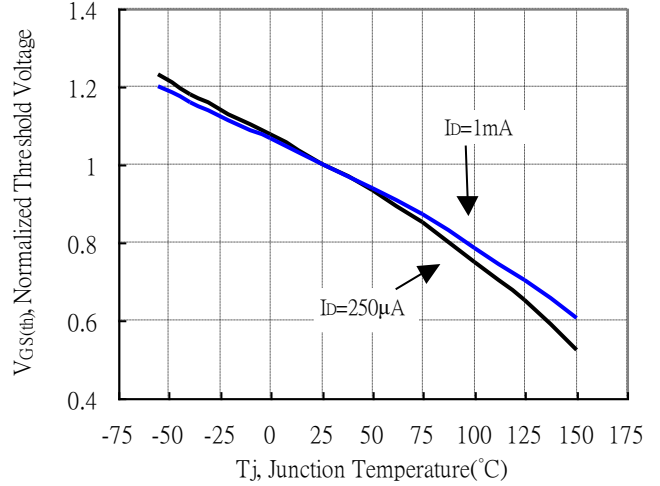


Typical Characteristics(Cont.)

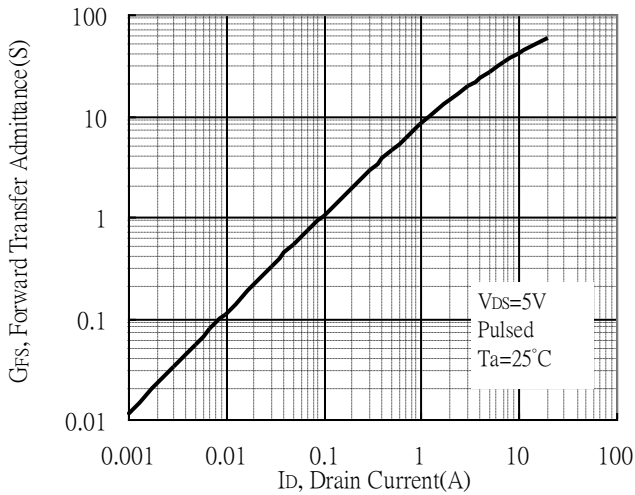
Capacitance vs Drain-to-Source Voltage



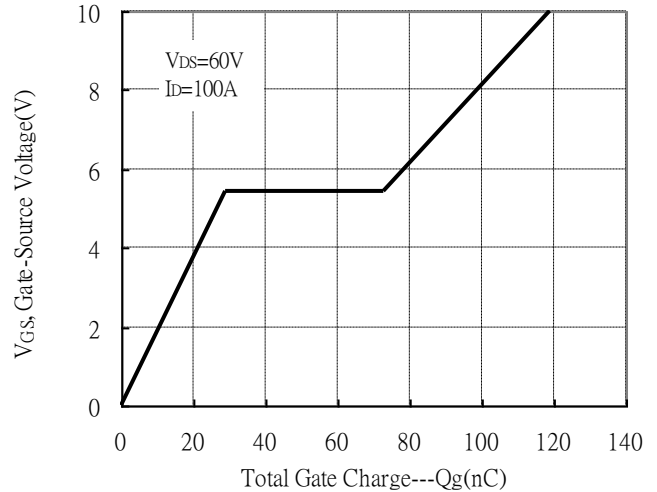
Threshold Voltage vs Junction Temperature



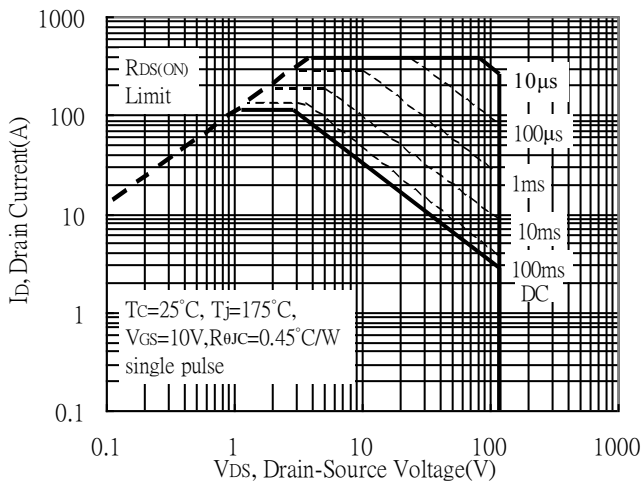
Forward Transfer Admittance vs Drain Current



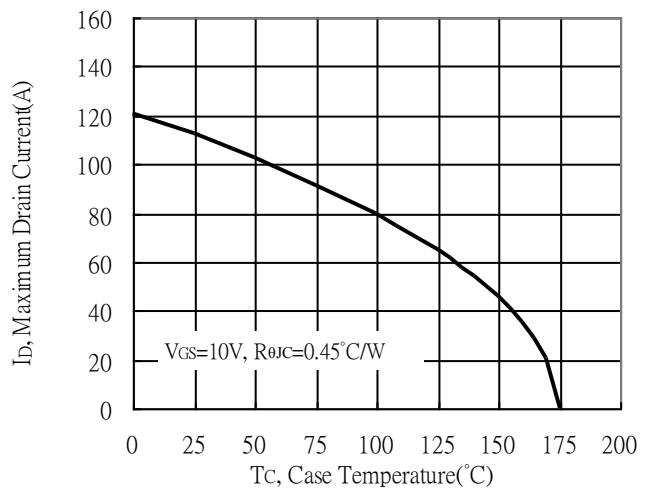
Gate Charge Characteristics



Maximum Safe Operating Area



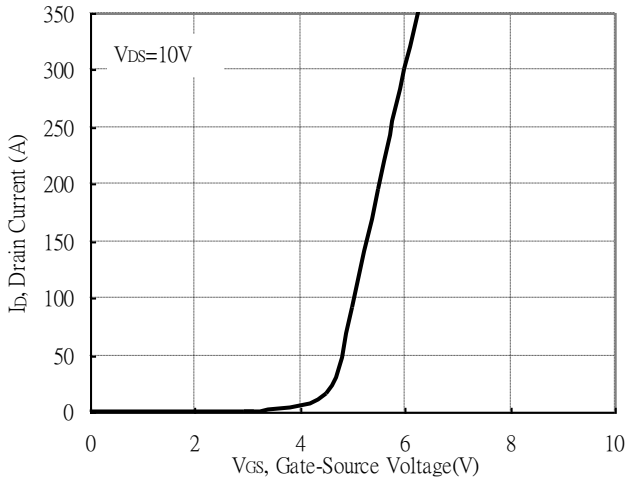
Maximum Drain Current vs Case Temperature



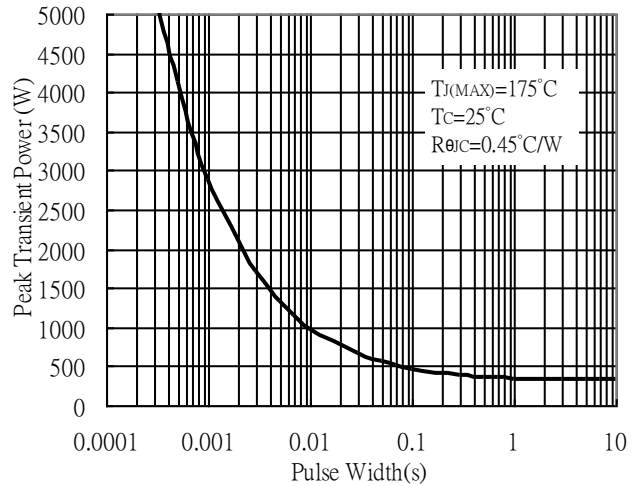


Typical Characteristics(Cont.)

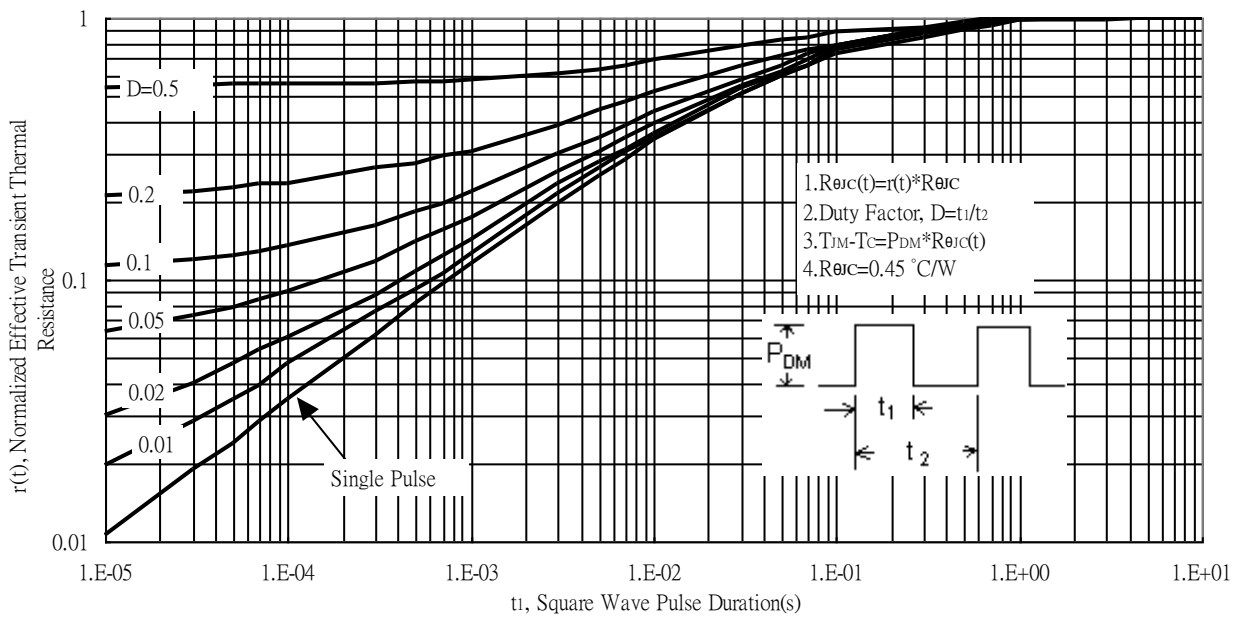
Typical Transfer Characteristics



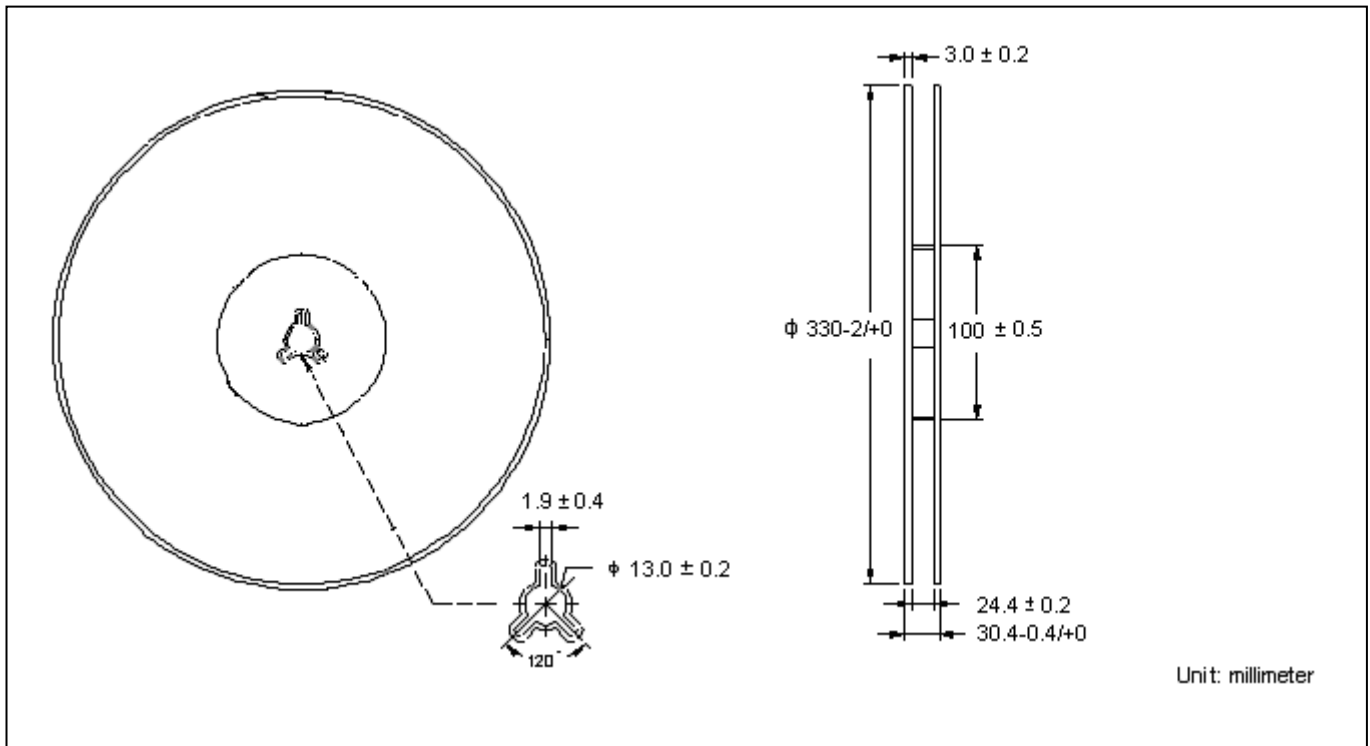
Single Pulse Maximum Power Dissipation



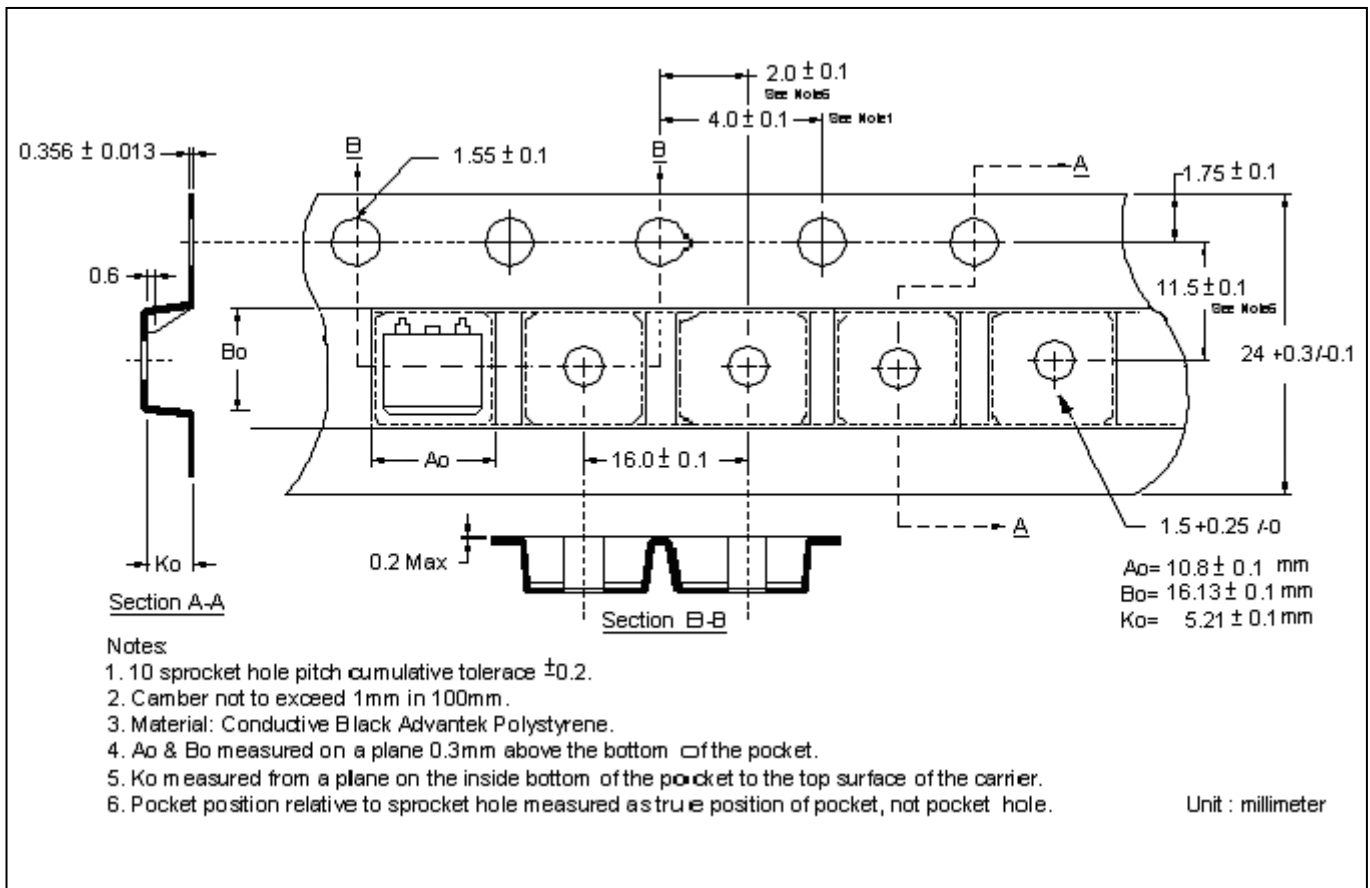
Transient Thermal Response Curves



Reel Dimension



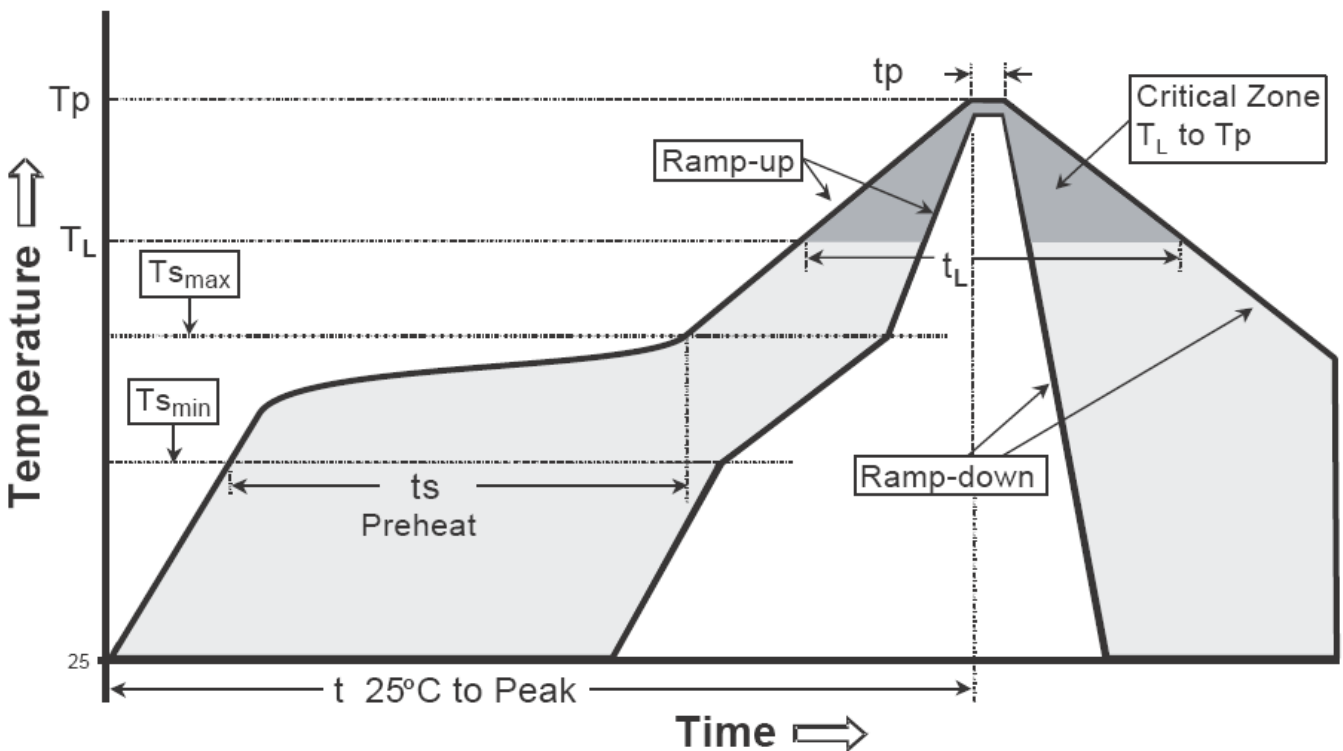
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

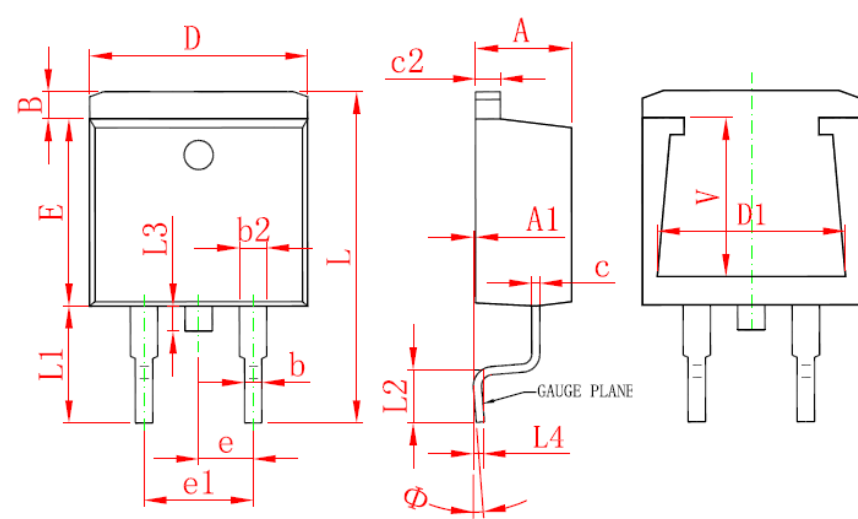
Recommended temperature profile for IR reflow



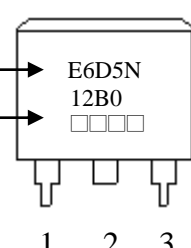
Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-263 Dimension



Marking :



Device Code → E6D5N
 Date Code → 12B0
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1 2 3

Style : Pin 1.Gate 2.Drain
 3.Source

3-Lead Plastic Surface Mounted Package
CYStek Package Code : F3

Date Code : (From left to right)
 First Code : Year code, the last digit of Christian year. For example, 2014→4, 2015→, 2016→6, ..., etc.
 Second Code : Month code, Jan→A, Feb→B, Mar→C, Apr→D, May→E, Jun→F, Jul→G, Aug→H, Sep→J,
 Oct→K, Nov→L, Dec→M
 Third and fourth codes : production serial number, 01~99

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	4.470	4.670	0.176	0.184	e	2.540	TYP	0.100	TYP
A1	0.000	0.150	0.000	0.006	e1	4.980	5.180	0.196	0.204
B	1.120	1.420	0.044	0.056	L	14.940	15.500	0.588	0.610
b	0.710	0.910	0.028	0.036	L1	4.950	5.450	0.195	0.215
b1	1.170	1.370	0.046	0.054	L2	2.340	2.740	0.092	0.108
c	0.381	0.530	0.015	0.021	L3	1.300	1.700	0.051	0.067
c1	1.170	1.370	0.046	0.054	L4	0.250 BSC		0.010 BSC	
D	10.010	10.310	0.394	0.406	Φ	0°	8°	0°	8°
D1	7.562	8.562	0.245	0.337	V	5.880	6.880	0.231	0.271
E	8.500	8.900	0.335	0.350					

Notes : 1.Controlling dimension : millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

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