

N -Channel Enhancement Mode Power MOSFET

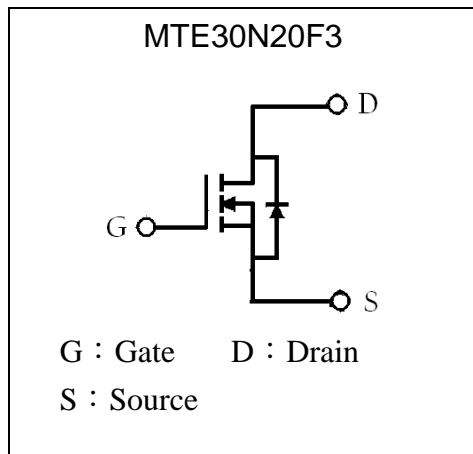
MTE30N20F3

BV_{DSS}	200V
$I_D@V_{GS}=10V, T_C=25^\circ C$	50A
$I_D@V_{GS}=10V, T_A=25^\circ C$	4.8A
$R_{DS(on)(TYP)}$ $V_{GS}=10V, I_D=17A$	28.6mΩ

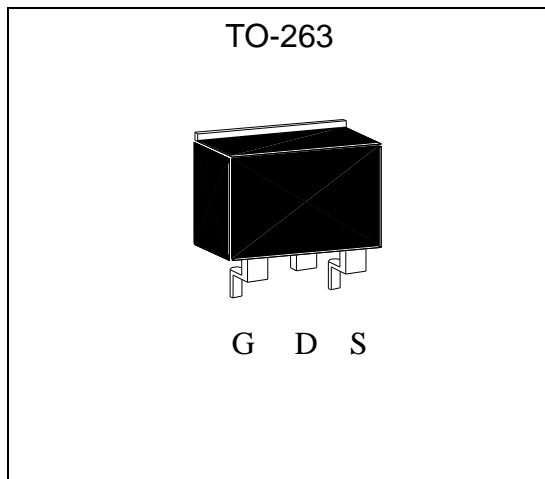
Features

- Low Gate Charge
- Simple Drive Requirement
- Pb-free lead plating package

Symbol

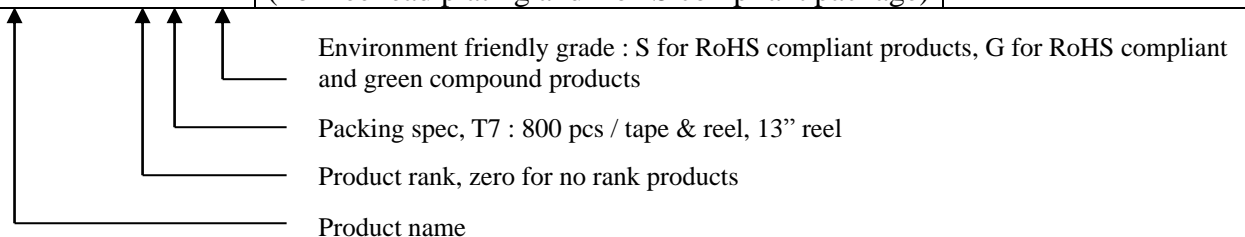


Outline



Ordering Information

Device	Package	Shipping
MTE30N20F3-0-T7-S	TO-263 (Pb-free lead plating and RoHS compliant package)	800 pcs / Tape & Reel



**Absolute Maximum Ratings** ($T_C=25^{\circ}\text{C}$, unless otherwise noted)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current @ $T_C=25^{\circ}\text{C}$, $V_{GS}=10\text{V}$	I_D	50	A
Continuous Drain Current @ $T_C=100^{\circ}\text{C}$, $V_{GS}=10\text{V}$		35	
Continuous Drain Current @ $T_A=25^{\circ}\text{C}$, $V_{GS}=10\text{V}$ (Note 2)	I_{DSM}	4.8	
Continuous Drain Current @ $T_A=70^{\circ}\text{C}$, $V_{GS}=10\text{V}$ (Note 2)		3.8	
Pulsed Drain Current (Note 3)	I_{DM}	200	
Avalanche Current (Note 3)	I_{AS}	14	
Avalanche Energy @ $L=2\text{mH}$, $I_D=14\text{A}$, $V_{DD}=50\text{V}$ (Note 2)	E_{AS}	196	mJ
Repetitive Avalanche Energy @ $L=0.1\text{mH}$ (Note 3)	E_{AR}	25	
Power Dissipation @ $T_C=25^{\circ}\text{C}$ (Note 1)	P_D	250	W
Power Dissipation @ $T_C=100^{\circ}\text{C}$ (Note 1)		125	
Power Dissipation @ $T_A=25^{\circ}\text{C}$ (Note 2)	P_{DSM}	2	
Power Dissipation @ $T_A=70^{\circ}\text{C}$ (Note 2)		1.3	
Operating Junction and Storage Temperature Range	T_j, T_{stg}	$-55\sim+175$	$^{\circ}\text{C}$

*100% UIS tested at condition of $L=2\text{mH}$, $I_{AS}=8\text{A}$, $V_{DD}=50\text{V}$.**Thermal Data**

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{th,j-c}$	0.6	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-ambient, max (Note 2)	$R_{th,j-a}$	62	

- Note : 1. The power dissipation P_D is based on $T_{J(MAX)}=175^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
2. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2 oz. copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.
3. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=175^{\circ}\text{C}$. Ratings are based on low frequency and low duty cycles to keep initial $T_j=25^{\circ}\text{C}$.
4. 100% tested by conditions of $L=2\text{mH}$, $I_{AS}=8\text{A}$, $V_{GS}=10\text{V}$, $V_{DD}=50\text{V}$
5. The static characteristics are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% maximum.
6. The $R_{\theta JA}$ is the sum of thermal resistance from junction to case $R_{\theta JC}$ and case to ambient.



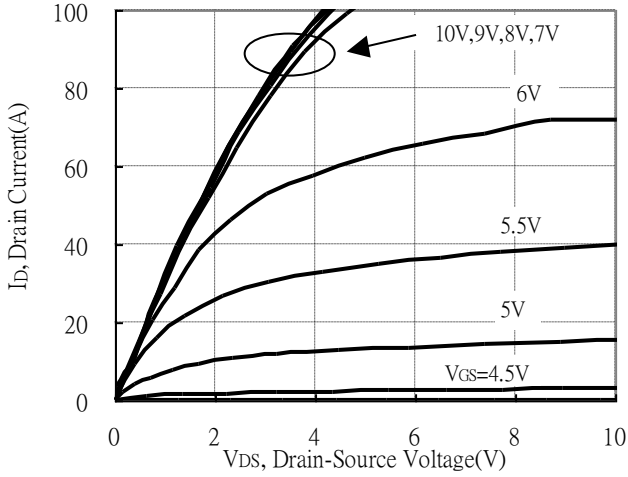
Characteristics (Tc=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	200	-	-	V	V _{GS} =0V, I _D =250μA
ΔBV _{DSS} /ΔT _j	-	0.18	-	V/°C	Reference to I _D =250μA
V _{GS(th)}	2	-	4	V	V _{DS} =V _{GS} , I _D =250μA
I _{GSS}	-	-	±100	nA	V _{GS} =±20V, V _{DS} =0V
I _{DSS}	-	-	1	μA	V _{DS} =160V, V _{GS} =0V
	-	-	25		V _{DS} =160V, V _{GS} =0V, T _J =125°C
R _{DS(ON)} *1	-	28.6	36	mΩ	V _{GS} =10V, I _D =17A
G _{FS} *1	-	24.5	-	S	V _{DS} =15V, I _D =10A
Dynamic					
Q _g *1, 2	-	71.1	-	nC	V _{DS} =160V, I _D =39A, V _{GS} =10V
Q _{gs} *1, 2	-	12.4	-		
Q _{gd} *1, 2	-	31.2	-		
t _{d(ON)} *1, 2	-	28.4	-	ns	V _{DS} =100V, I _D =37A, V _{GS} =10V, R _G =5.6Ω
t _r *1, 2	-	60	-		
t _{d(OFF)} *1, 2	-	74	-		
t _f *1, 2	-	100	-		
C _{iss}	-	3197	-	pF	V _{GS} =0V, V _{DS} =25V, f=1MHz
C _{oss}	-	335	-		
C _{rss}	-	116	-		
R _g	-	1.8	-	Ω	f=1MHz
Source-Drain Diode					
I _S *1	-	-	50	A	
I _{SM} *3	-	-	200		
V _{SD} *1	-	0.8	1.2	V	I _F =25A, V _{GS} =0V
t _{rr}	-	78	-	ns	I _F =20A, dI _F /dt=100A/μs
Q _{rr}	-	300	-	nC	

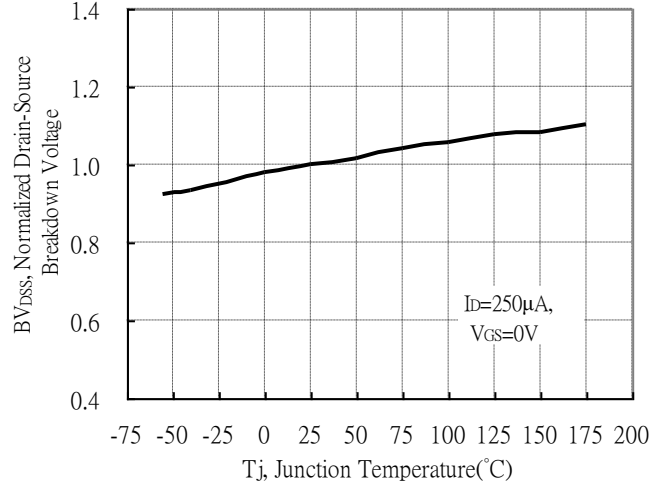
Note : *1.Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%
 *2.Independent of operating temperature
 *3.Pulse width limited by maximum junction temperature.

Typical Characteristics

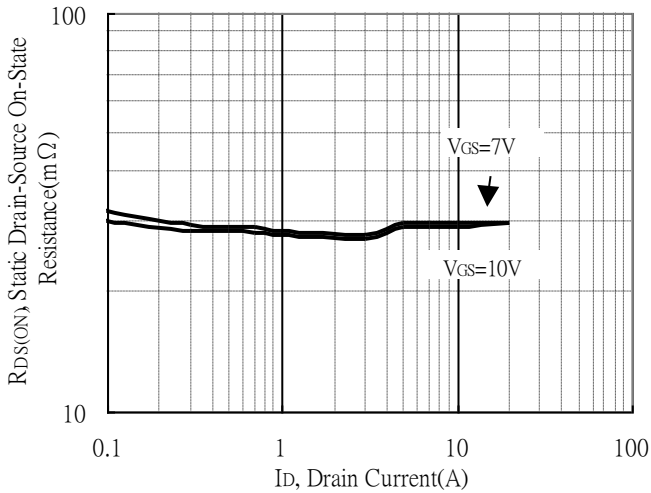
Typical Output Characteristics



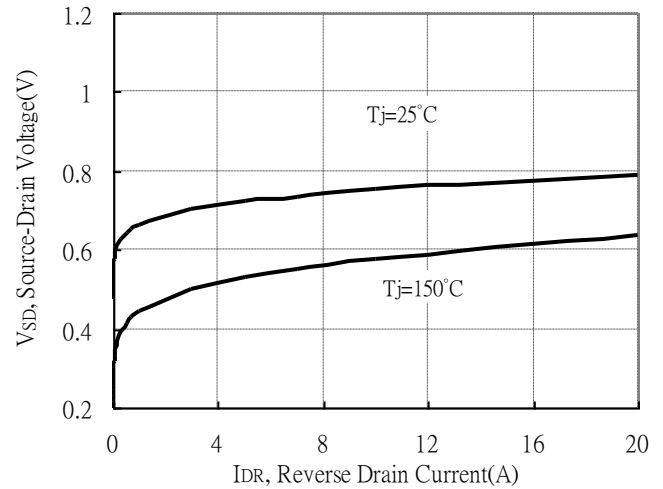
Brekdown Voltage vs Junction Temperature



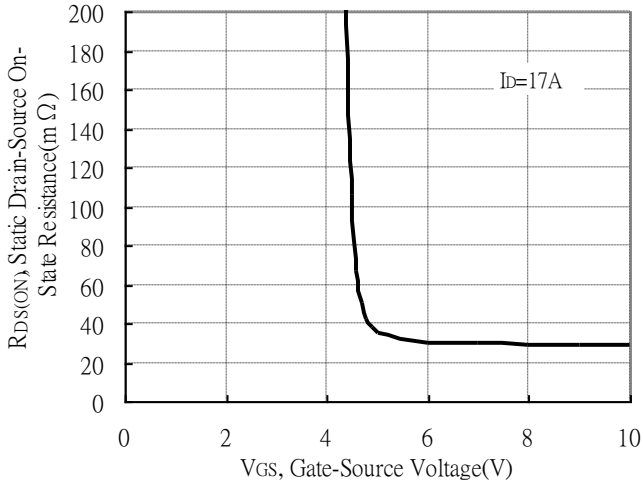
Static Drain-Source On-State resistance vs Drain Current



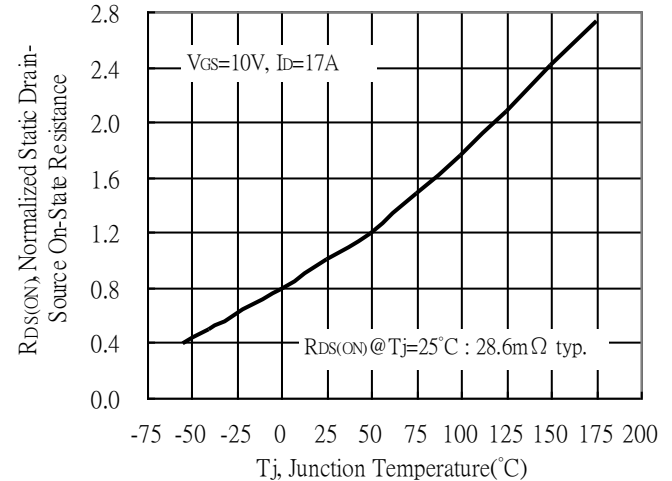
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

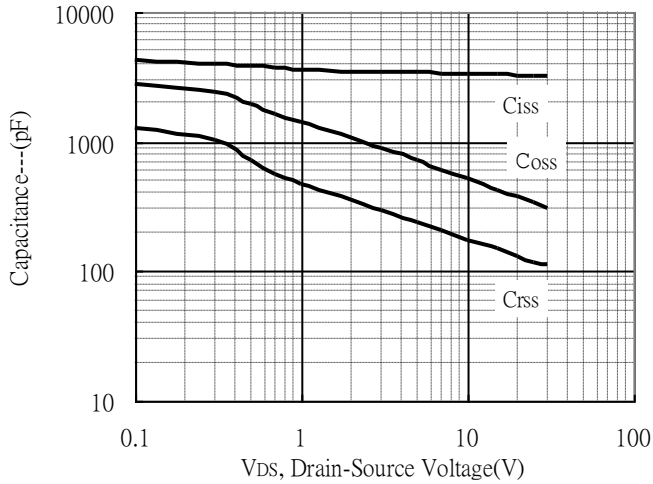


Drain-Source On-State Resistance vs Junction Temperature

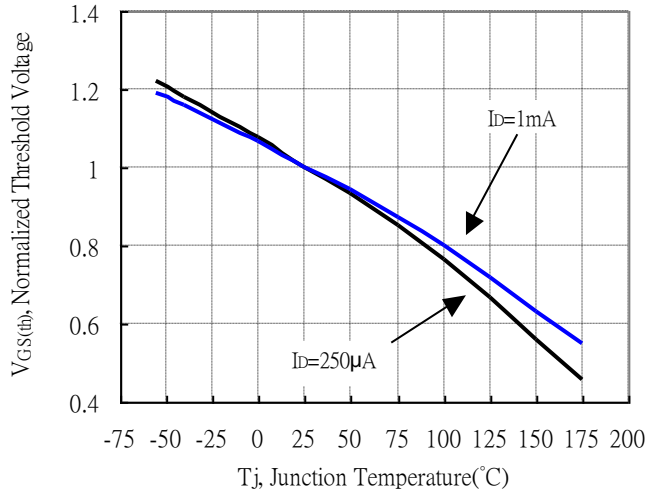


Typical Characteristics(Cont.)

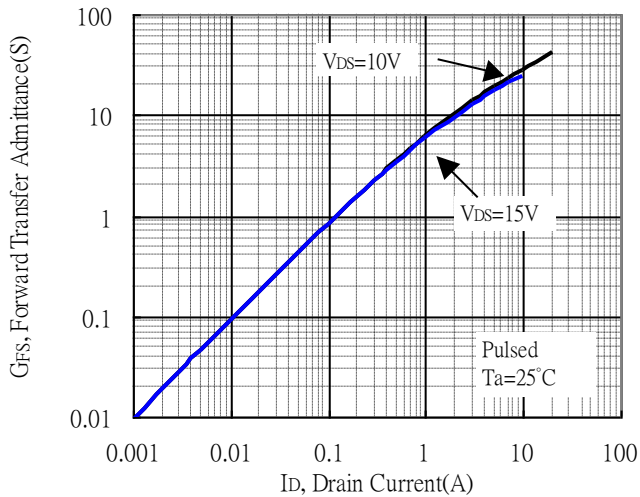
Capacitance vs Drain-to-Source Voltage



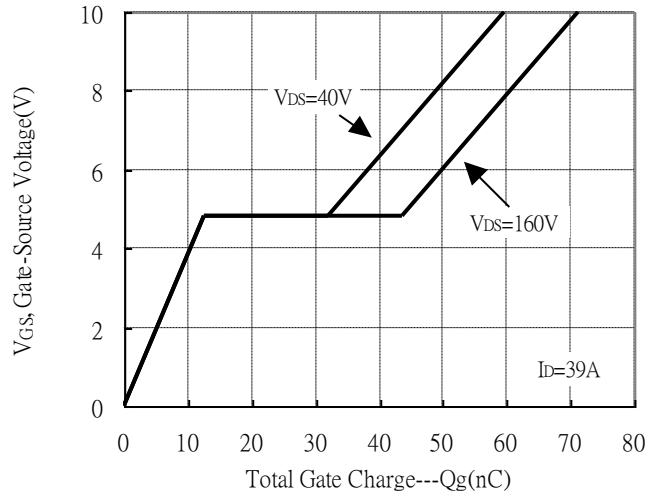
Threshold Voltage vs Junction Temperature



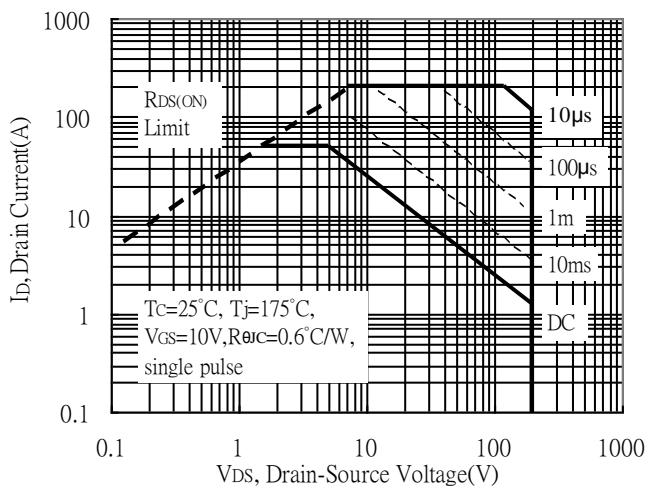
Forward Transfer Admittance vs Drain Current



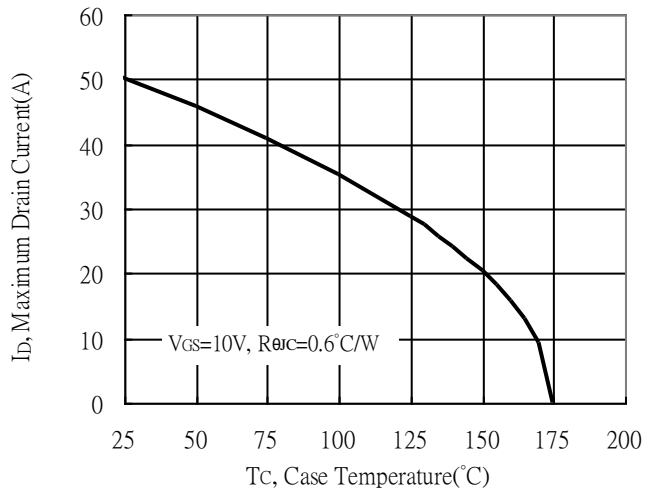
Gate Charge Characteristics



Maximum Safe Operating Area

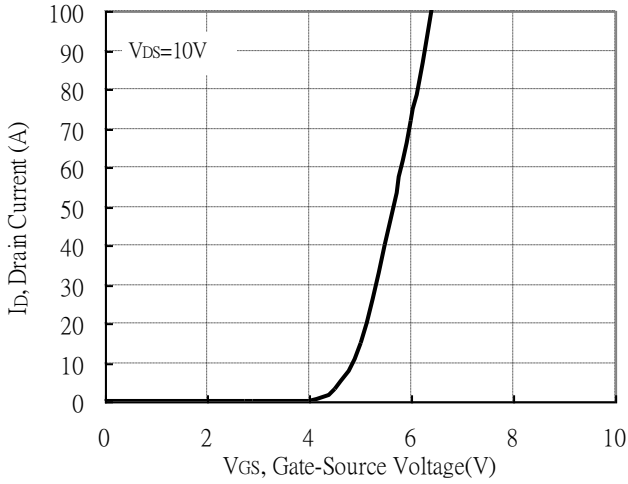


Maximum Drain Current vs Case Temperature

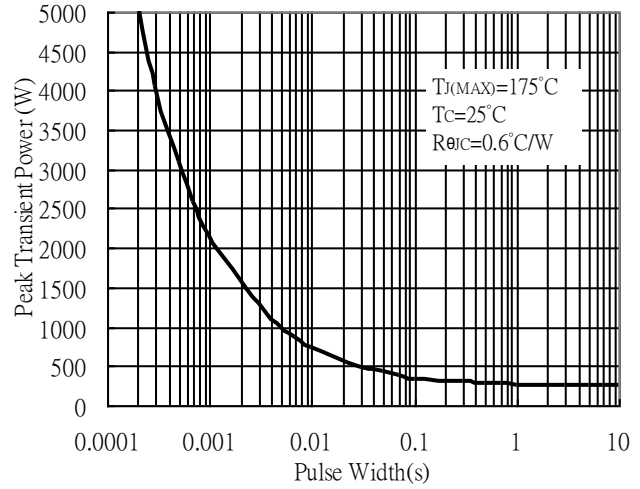


Typical Characteristics(Cont.)

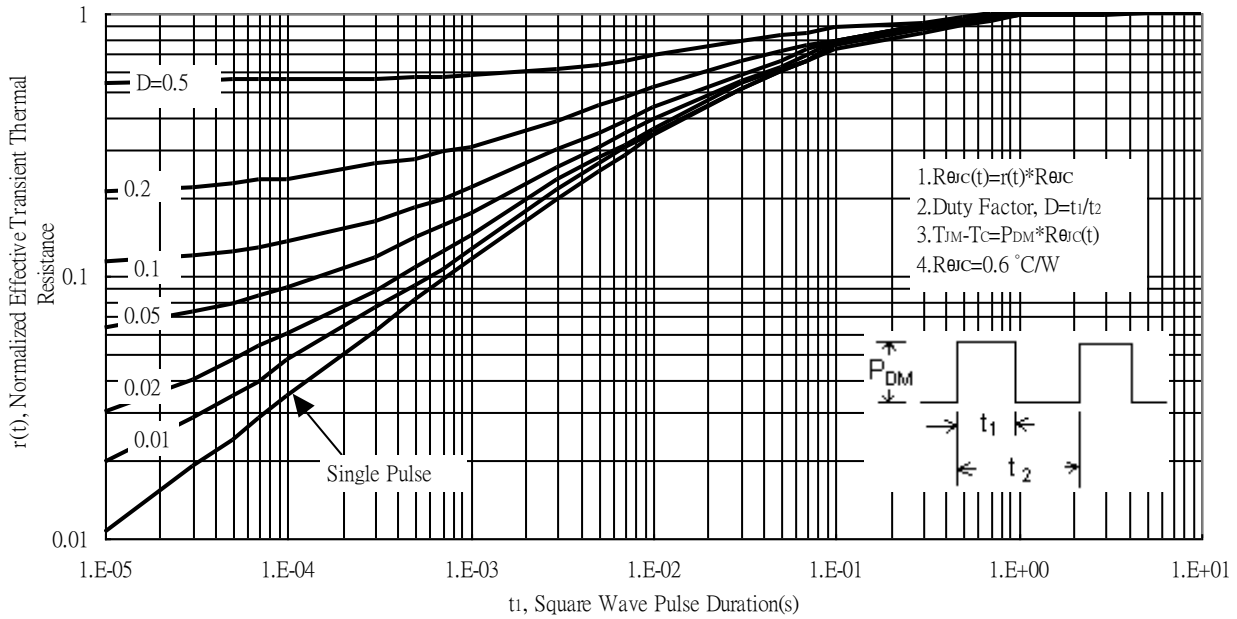
Typical Transfer Characteristics



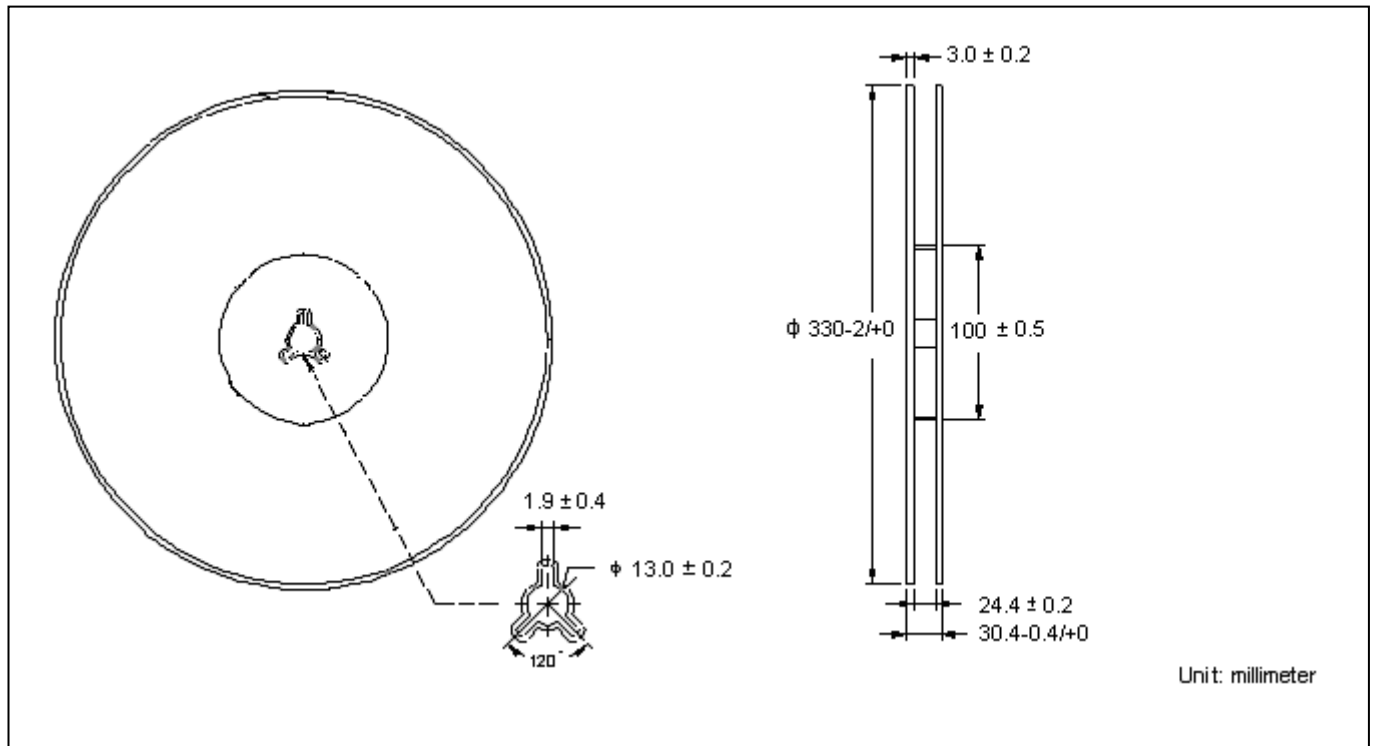
Single Pulse Maximum Power Dissipation



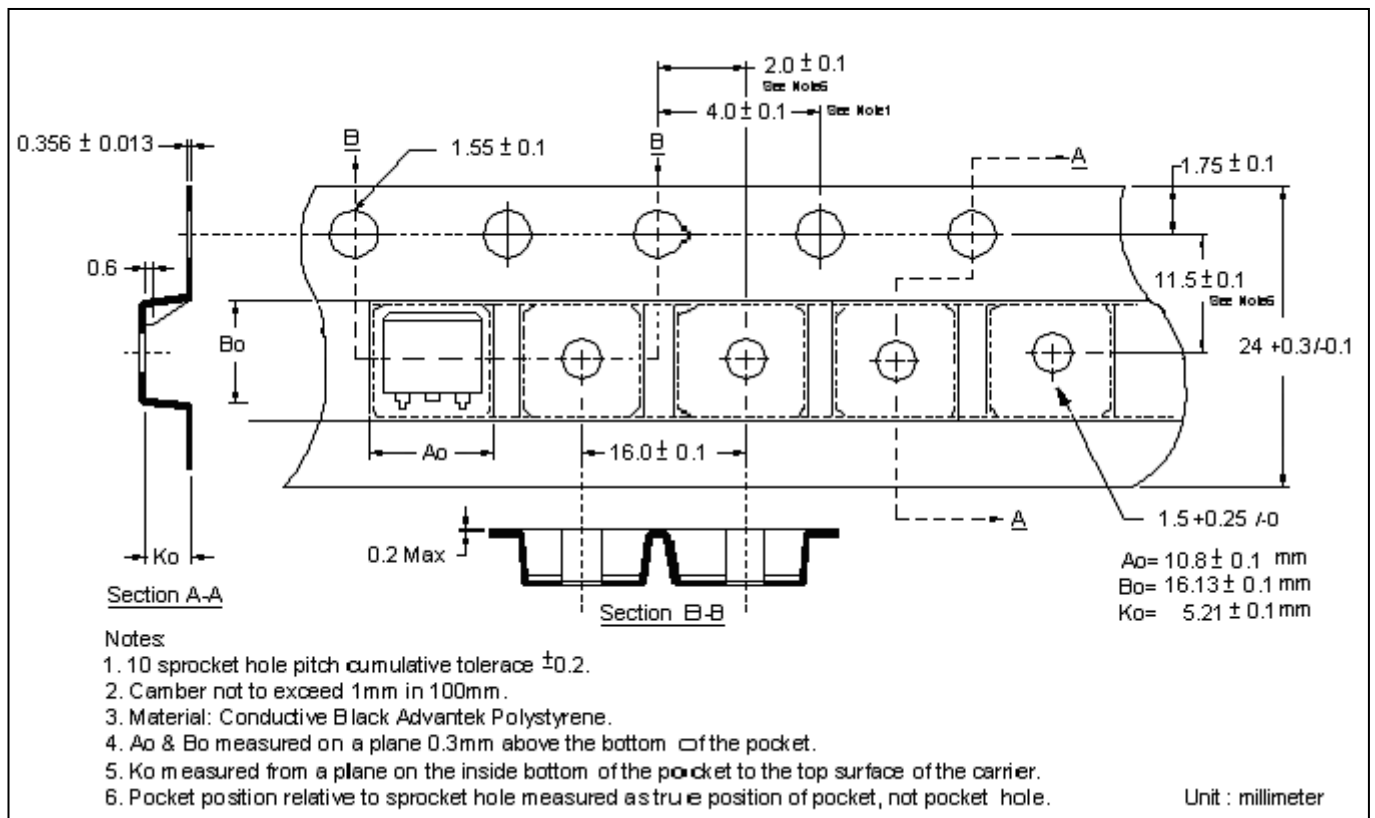
Transient Thermal Response Curves



Reel Dimension



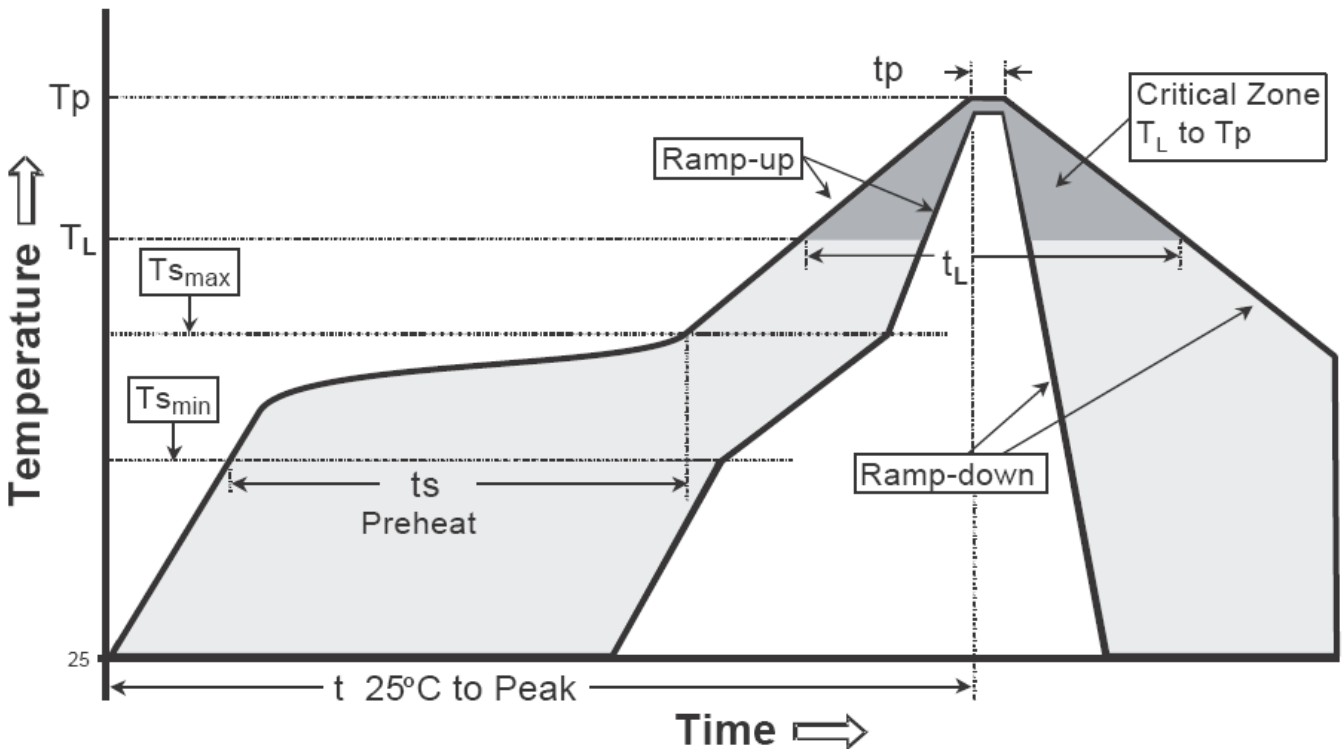
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

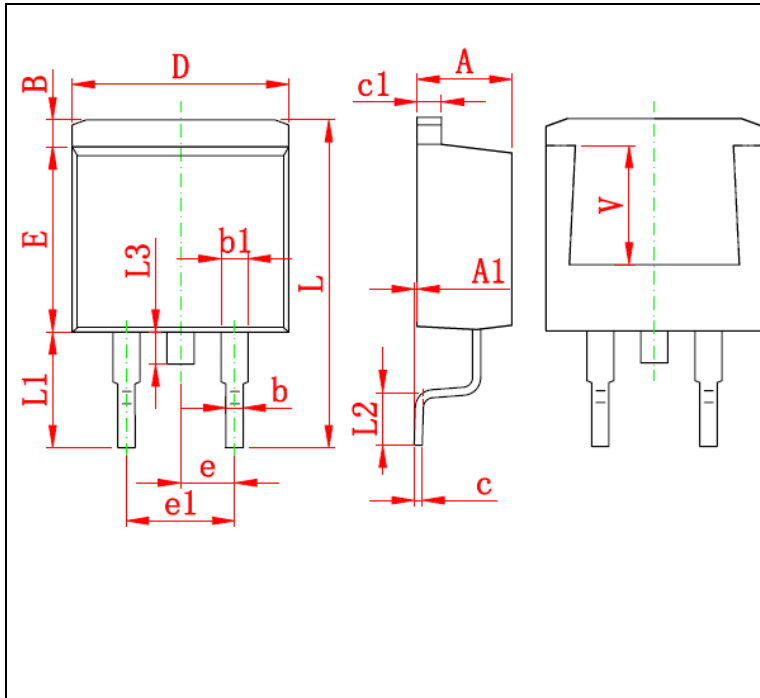
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{Smax} to T _P)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{S min})	100°C	150°C
-Temperature Max(T _{S max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(t _p)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

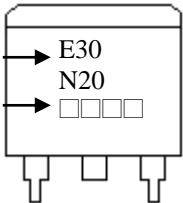
Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-263 Dimension



The diagram shows three views of the TO-263 package: a top view, a side view, and a bottom view. Dimensions are labeled with letters and numbers: A, A1, B, C, C1, D, E, E1, L, L1, L2, L3, b, b1, c, e, e1, and V. The top view shows a rectangular package with three leads extending from the bottom. The side view shows the profile of the package and the leads. The bottom view shows the leads from a different perspective.

Marking :



Device Name → E30
 N20
 Date Code → □□□□

Style : Pin 1.Gate 2.Drain 3.Source

3-Lead Plastic Surface Mounted Package
 CYStek Package Code : F3

*:Typical

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	4.470	4.670	0.176	0.184	E	8.500	8.900	0.335	0.350
A1	0.000	0.150	0.000	0.006	e	*2.540		*0.100	
B	1.170	1.370	0.046	0.054	e1	4.980	5.180	0.196	0.204
b	0.710	0.910	0.028	0.036	L	15.050	15.450	0.593	0.608
b1	1.170	1.370	0.046	0.054	L1	5.080	5.480	0.200	0.216
c	0.310	0.530	0.012	0.021	L2	2.340	2.740	0.092	0.108
c1	1.170	1.370	0.046	0.054	L3	1.300	1.700	0.051	0.067
D	10.010	10.310	0.394	0.406	V	5.600	REF	0.220	REF

- Notes :**
- Controlling dimension : millimeters.
 - Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 - If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

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