

**N-Channel Enhancement Mode Power MOSFET**

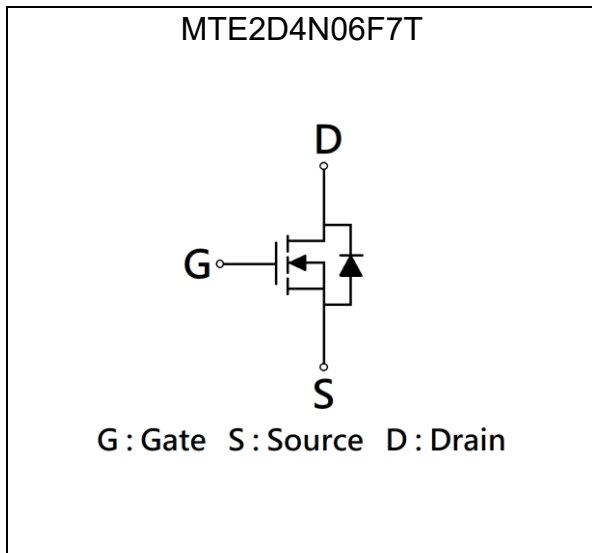
# MTE2D4N06F7T

**Features**

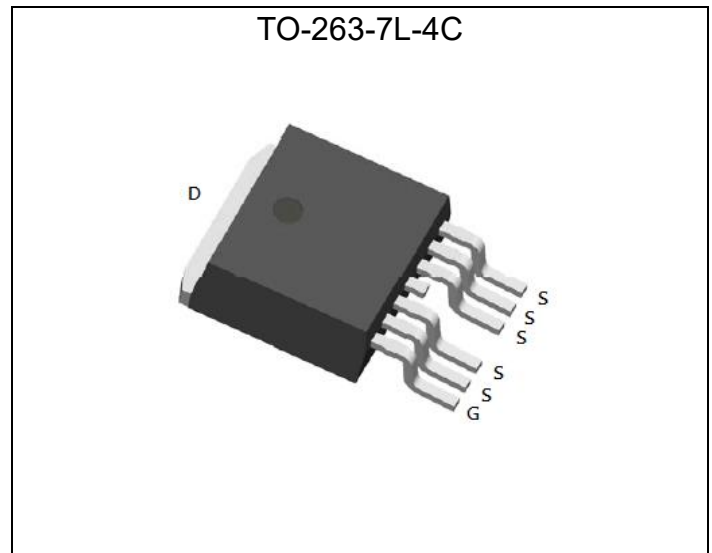
- Low On Resistance
- Low Gate Charge
- Fast Switching Characteristic

$BV_{DSS}$	60V
$I_D@V_{GS}=10V, T_C=25^\circ C$	150A
$I_D@V_{GS}=10V, T_A=25^\circ C$	27A
$R_{DS(ON) typ. @ V_{GS}=10V, I_D=20A}$	2mΩ

**Equivalent Circuit**

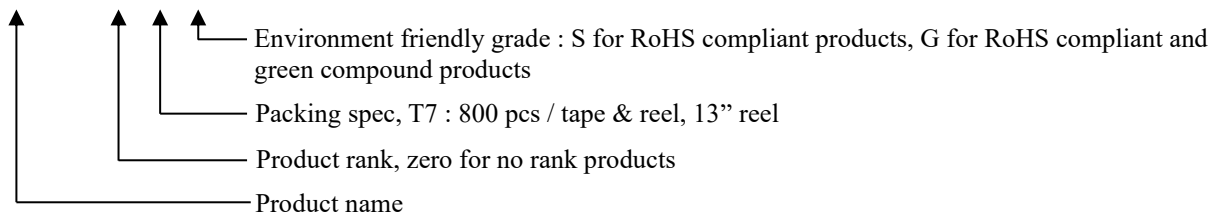


**Outline**



**Ordering Information**

Device	Package	Shipping
MTE2D4N06F7T-0-T7-G	TO-263-7L-4C (Pb-free lead plating and RoHS compliant package)	800 pcs / Tape & Reel



**Absolute Maximum Ratings (T<sub>A</sub>=25°C)**

Parameter	Symbol	Limits	Unit	
Drain-Source Voltage	V <sub>DS</sub>	60	V	
Gate-Source Voltage	V <sub>GS</sub>	±30		
Continuous Drain Current @ V <sub>GS</sub> =10V, T <sub>C</sub> =25°C	I <sub>D</sub>	150	A	
Continuous Drain Current @ V <sub>GS</sub> =10V, T <sub>C</sub> =100°C		95		
Continuous Drain Current @ V <sub>GS</sub> =10V, T <sub>A</sub> =25°C		27		
Continuous Drain Current @ V <sub>GS</sub> =10V, T <sub>A</sub> =70°C		22		
Pulsed Drain Current	I <sub>DM</sub>	600		
Continuous Body Diode Forward Current @ T <sub>C</sub> =25°C	I <sub>S</sub>	115		
Pulsed Body Diode Forward Current @ T <sub>C</sub> =25°C	I <sub>SM</sub>	460		
Avalanche Current @ L=0.1mH	I <sub>AS</sub>	80		
Avalanche Energy @ L=0.5mH	E <sub>AS</sub>	305	mJ	
Total Power Dissipation	P <sub>D</sub>	T <sub>C</sub> =25°C	139	W
		T <sub>C</sub> =100°C	56	
		T <sub>A</sub> =25°C	4.6	
		T <sub>A</sub> =70°C	2.9	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55~+150	°C	

**Thermal Data**

Parameter	Symbol	Steady State	Unit
Thermal Resistance, Junction-to-case	R <sub>θJC</sub>	0.9	°C/W
Thermal Resistance, Junction-to-ambient	R <sub>θJA</sub>	27	

Note:

- \*a. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- \*b. The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2 oz. copper, in a still air environment with T<sub>A</sub>=25°C. The power dissipation P<sub>D</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
- \*c. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C. Ratings are based on low frequency and low duty cycles to keep initial T<sub>J</sub>=25°C.



**Electrical Characteristics (T<sub>A</sub>=25°C, unless otherwise specified)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
<b>Static</b>					
BV <sub>DSS</sub>	60	-	-	V	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA
V <sub>GS(th)</sub>	2	-	4		V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA
G <sub>FS</sub>	-	42	-	S	V <sub>DS</sub> =10V, I <sub>D</sub> =20A
I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> =±30V, V <sub>DS</sub> =0V
I <sub>DSS</sub>	-	-	1	μA	V <sub>DS</sub> =48V, V <sub>GS</sub> =0V
R <sub>DS(ON)</sub>	-	2	2.6	mΩ	V <sub>GS</sub> =10V, I <sub>D</sub> =20A
<b>Dynamic</b>					
C <sub>iss</sub>	-	6200	-	pF	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, f=1MHz
C <sub>oss</sub>	-	980	-		
C <sub>rss</sub>	-	350	-		
R <sub>g</sub>	-	1.3	-	Ω	f=1MHz
Q <sub>g</sub> *1, 2	-	120	-	nC	V <sub>DS</sub> =30V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V
Q <sub>gs</sub> *1, 2	-	25	-		
Q <sub>gd</sub> *1, 2	-	40	-		
t <sub>d(ON)</sub> *1, 2	-	43	-	ns	V <sub>DS</sub> =30V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V, R <sub>GS</sub> =4.7Ω
t <sub>r</sub> *1, 2	-	39	-		
t <sub>d(OFF)</sub> *1, 2	-	95	-		
t <sub>f</sub> *1, 2	-	33	-		
<b>Source-Drain Diode</b>					
V <sub>SD</sub> *1	-	0.77	1.2	V	I <sub>S</sub> =20A, V <sub>GS</sub> =0V
t <sub>rr</sub>	-	49	-	ns	I <sub>F</sub> =20A, dI <sub>F</sub> /dt=100A/μs
Q <sub>rr</sub>	-	71	-	nC	

Note:

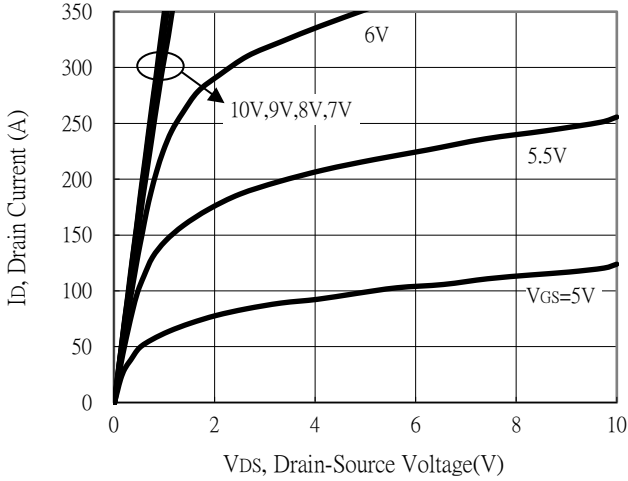
\*1. Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

\*2. Independent of operating temperature

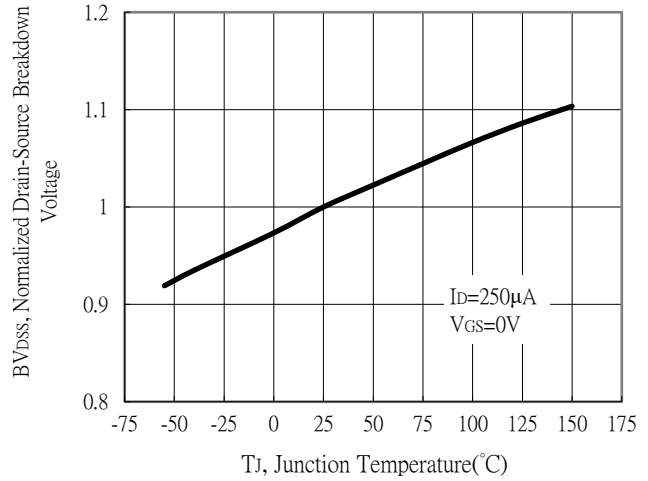


### Typical Characteristics

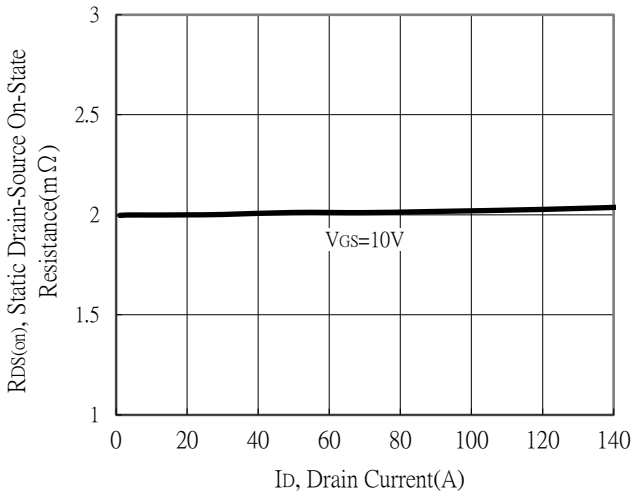
Typical Output Characteristics



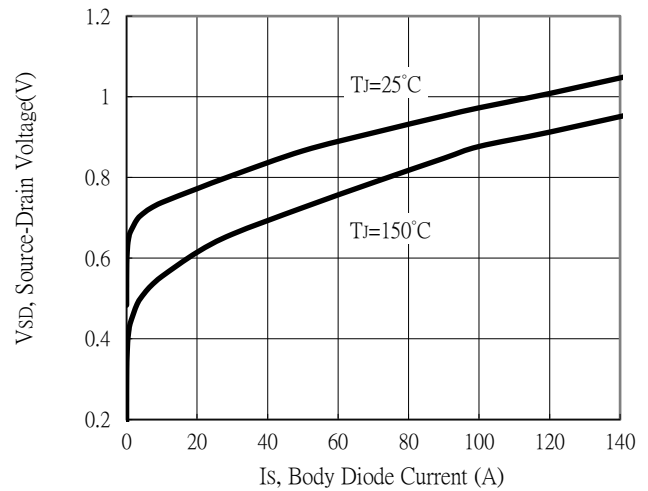
Breakdown Voltage vs Ambient Temperature



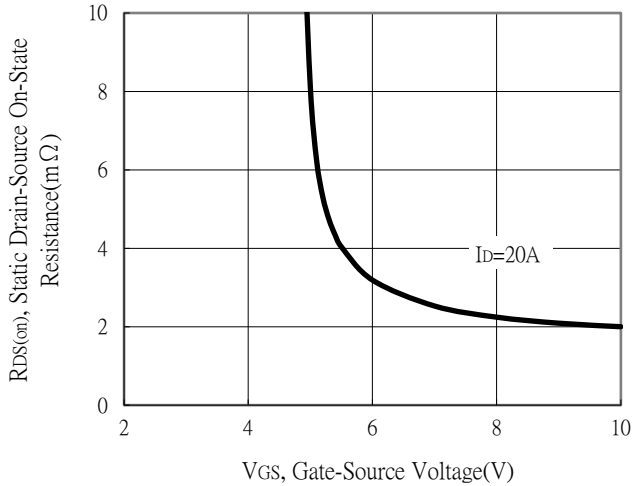
Static Drain-Source On-State resistance vs Drain Current



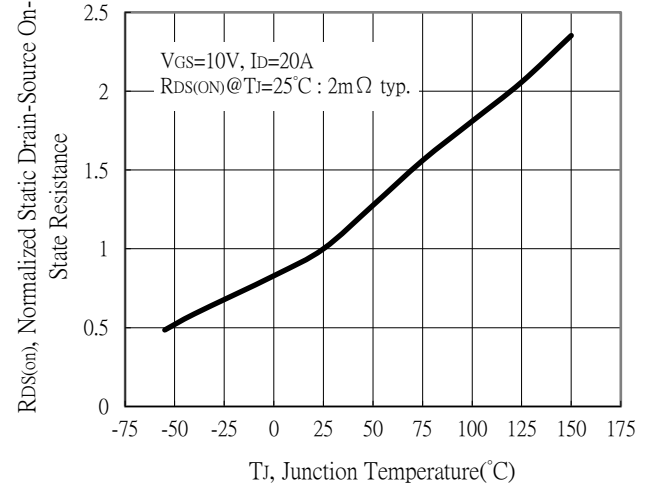
Body Diode Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage



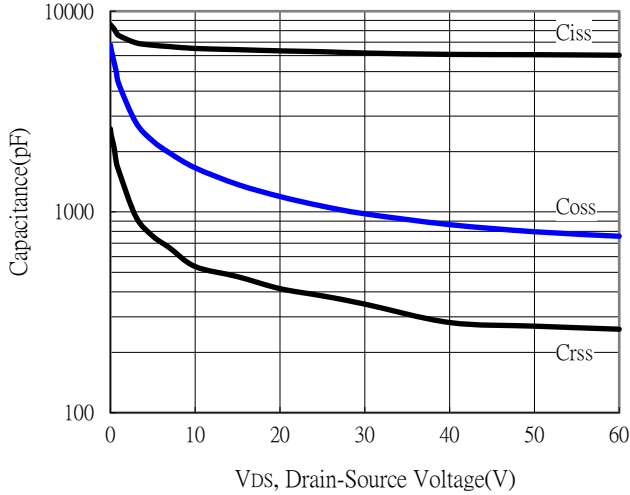
Drain-Source On-State Resistance vs Junction Temperature



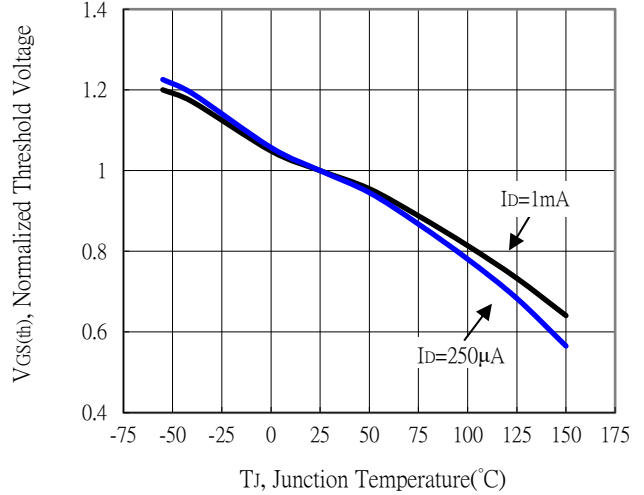


**Typical Characteristics (Cont.)**

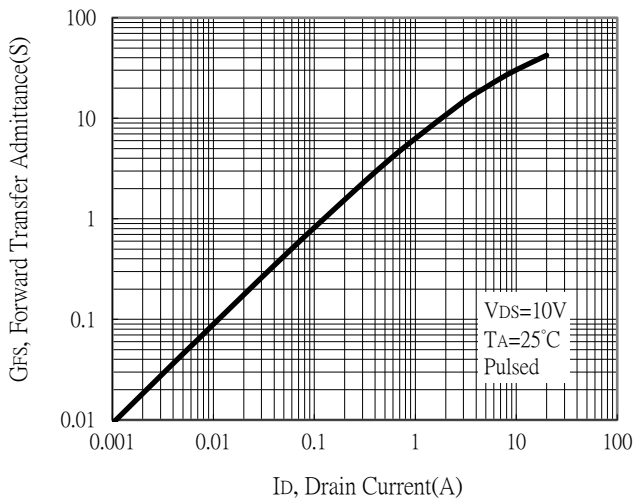
Capacitance vs Drain-to-Source Voltage



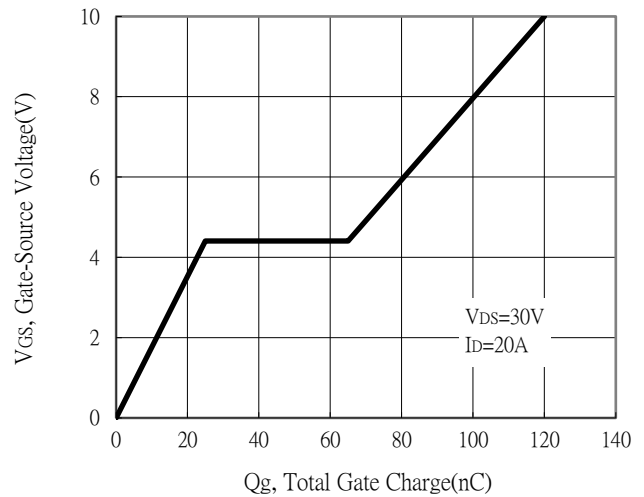
Threshold Voltage vs Junction Temperature



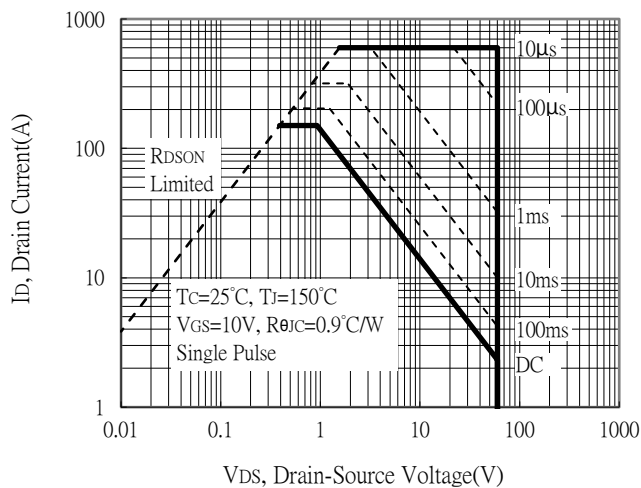
Forward Transfer Admittance vs Drain Current



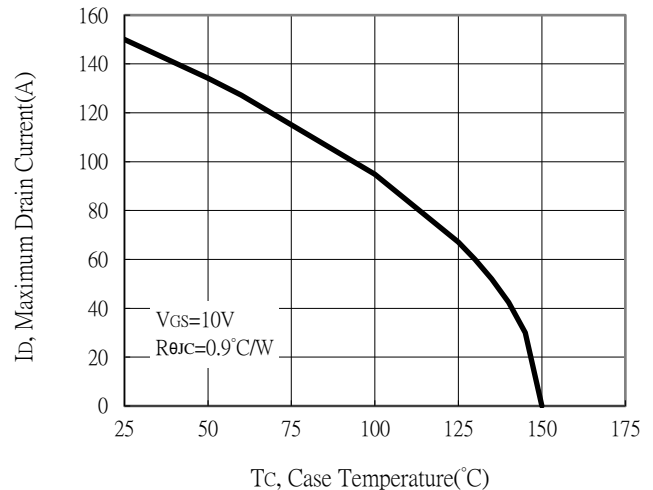
Gate Charge Characteristics



Maximum Safe Operating Area



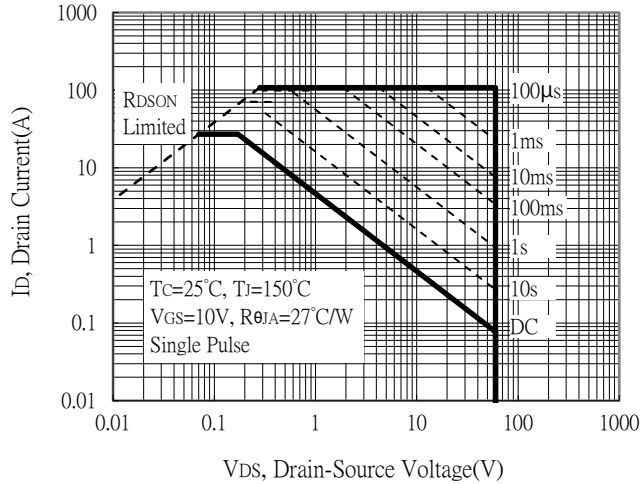
Maximum Drain Current vs Case Temperature



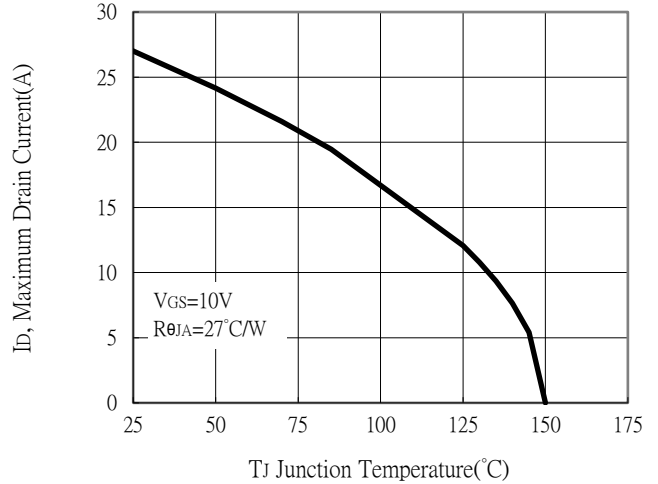


**Typical Characteristics (Cont.)**

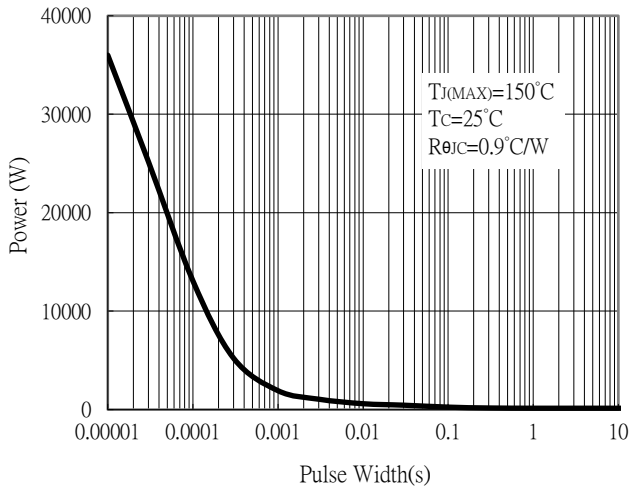
Maximum Safe Operating Area



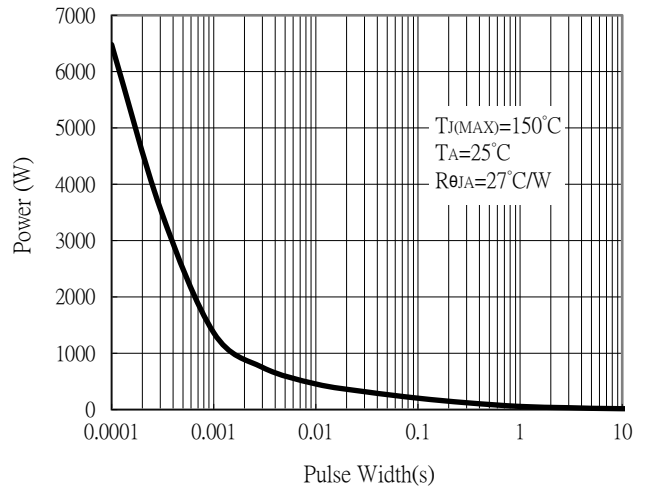
Maximum Drain Current vs Junction Temperature



Single Pulse Power Rating, Junction to Case

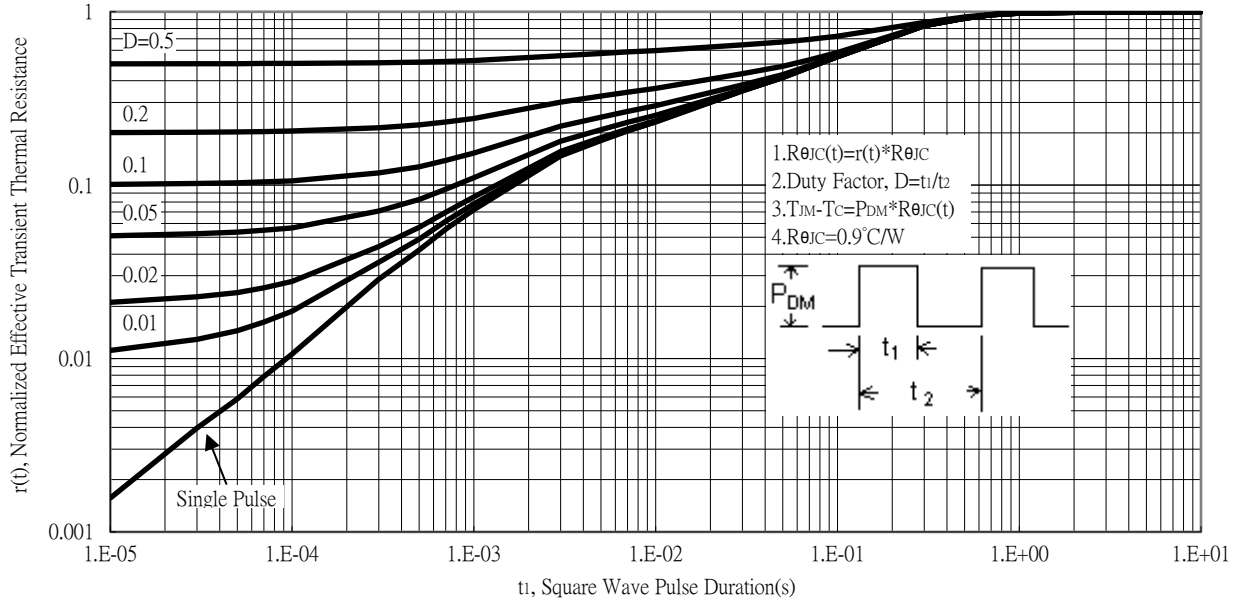


Single Pulse Power Rating, Junction to Ambient

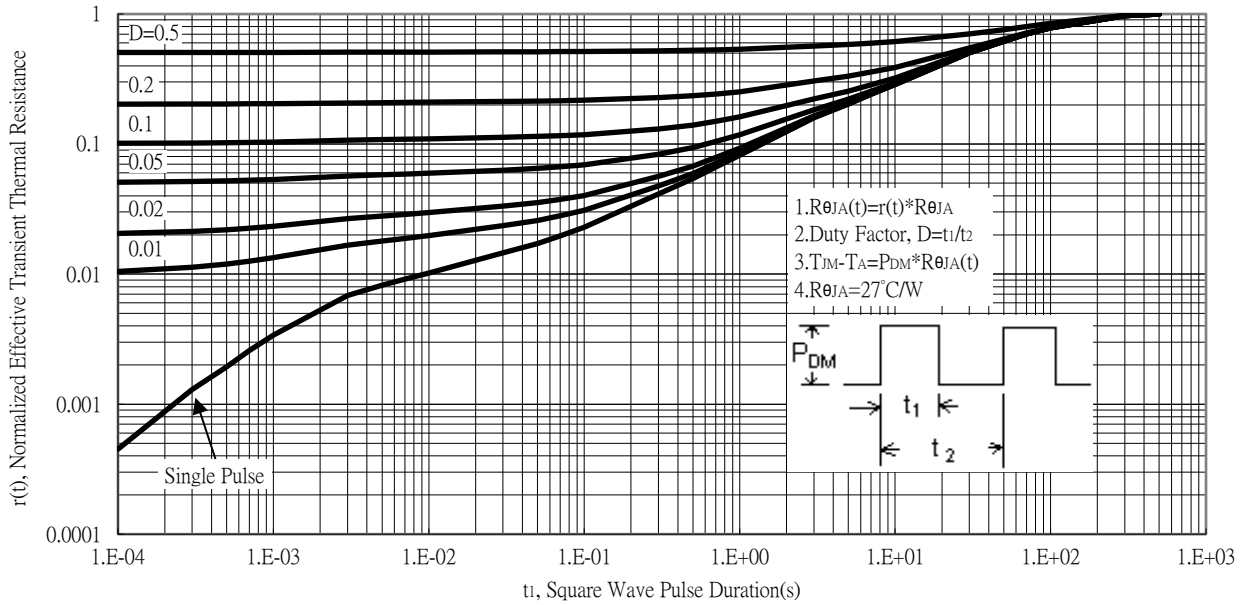


**Typical Characteristics (Cont.)**

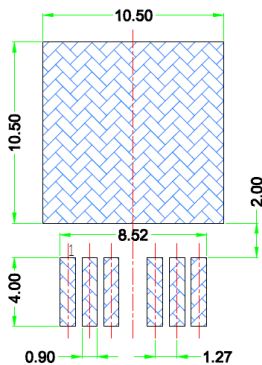
Transient Thermal Response Curves



Transient Thermal Response Curves

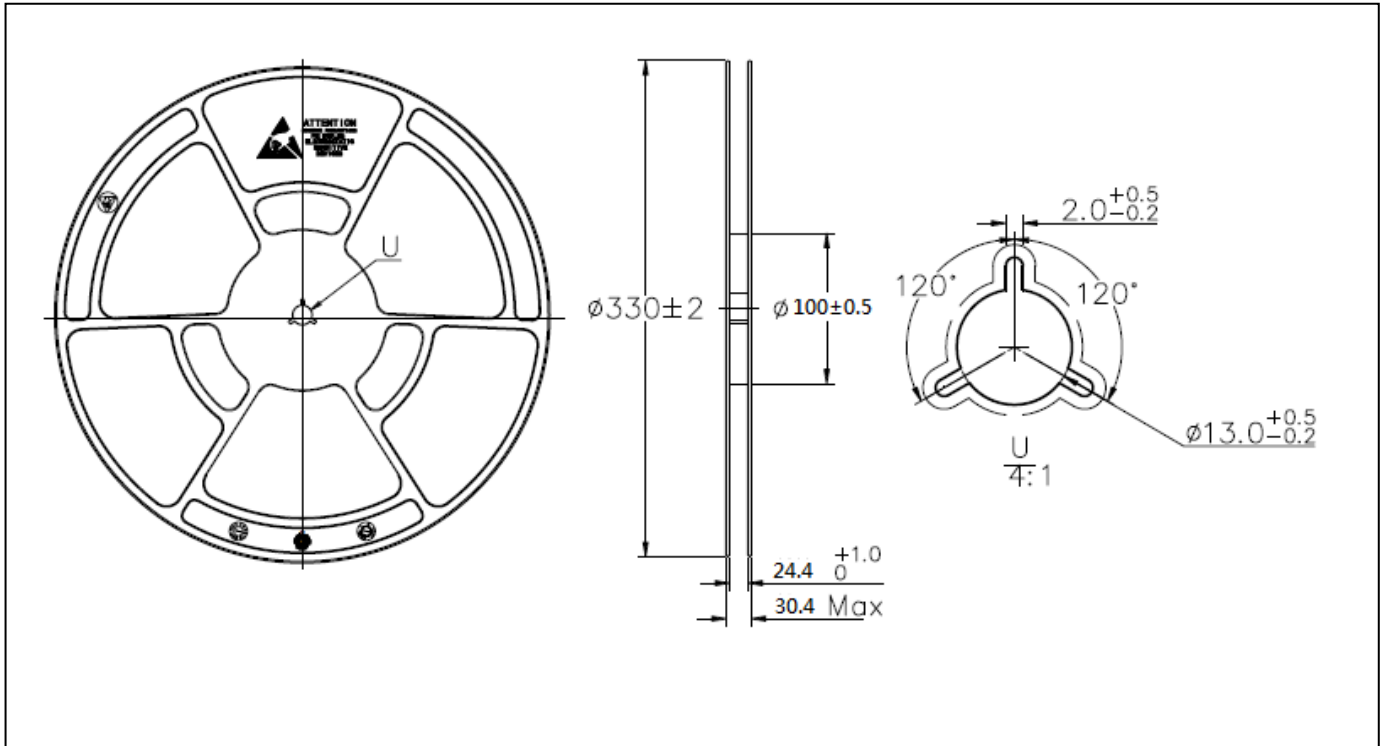


**Recommended Soldering Footprint**

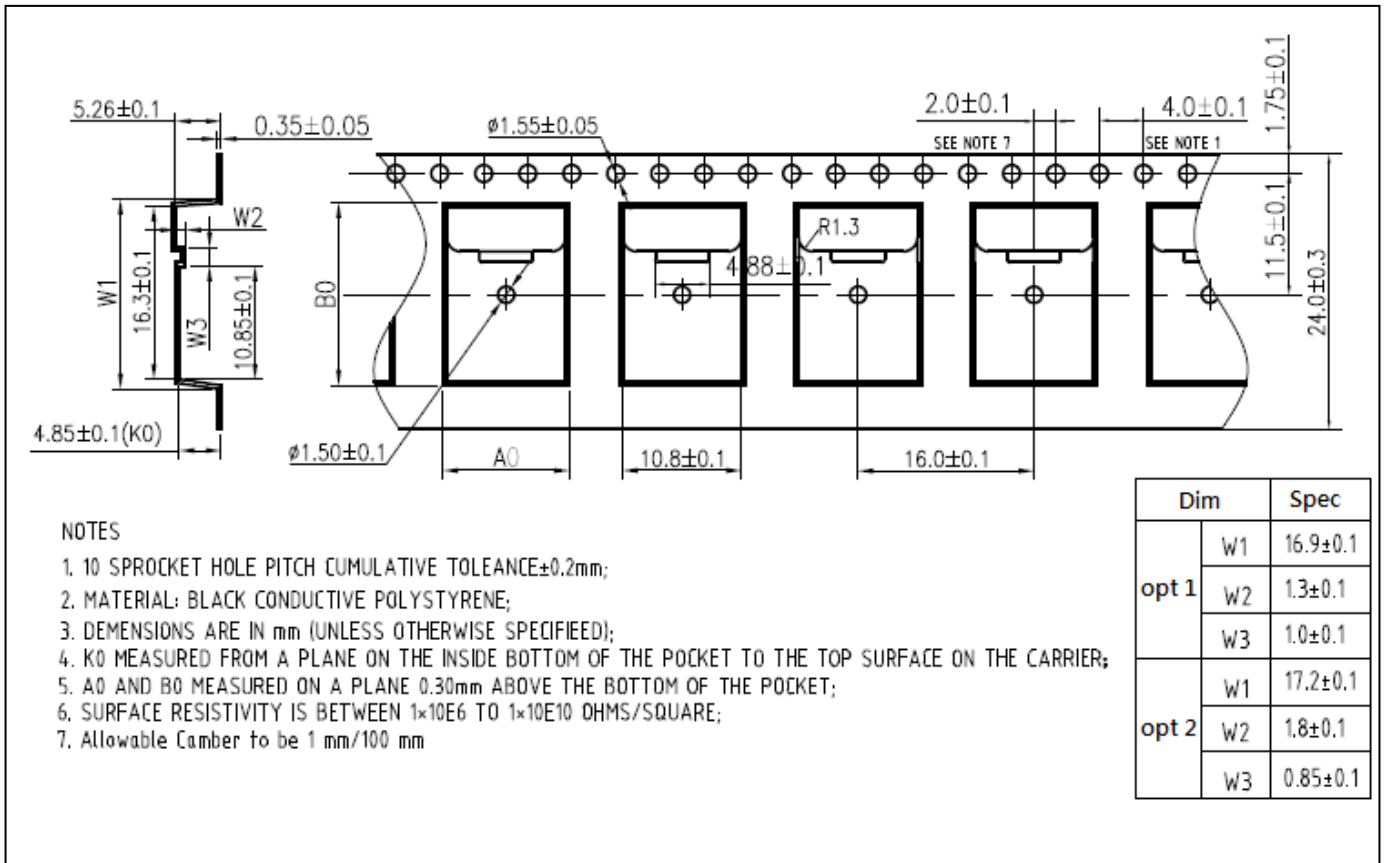


Unit : mm

**Reel Dimension**



**Carrier Tape Dimension**

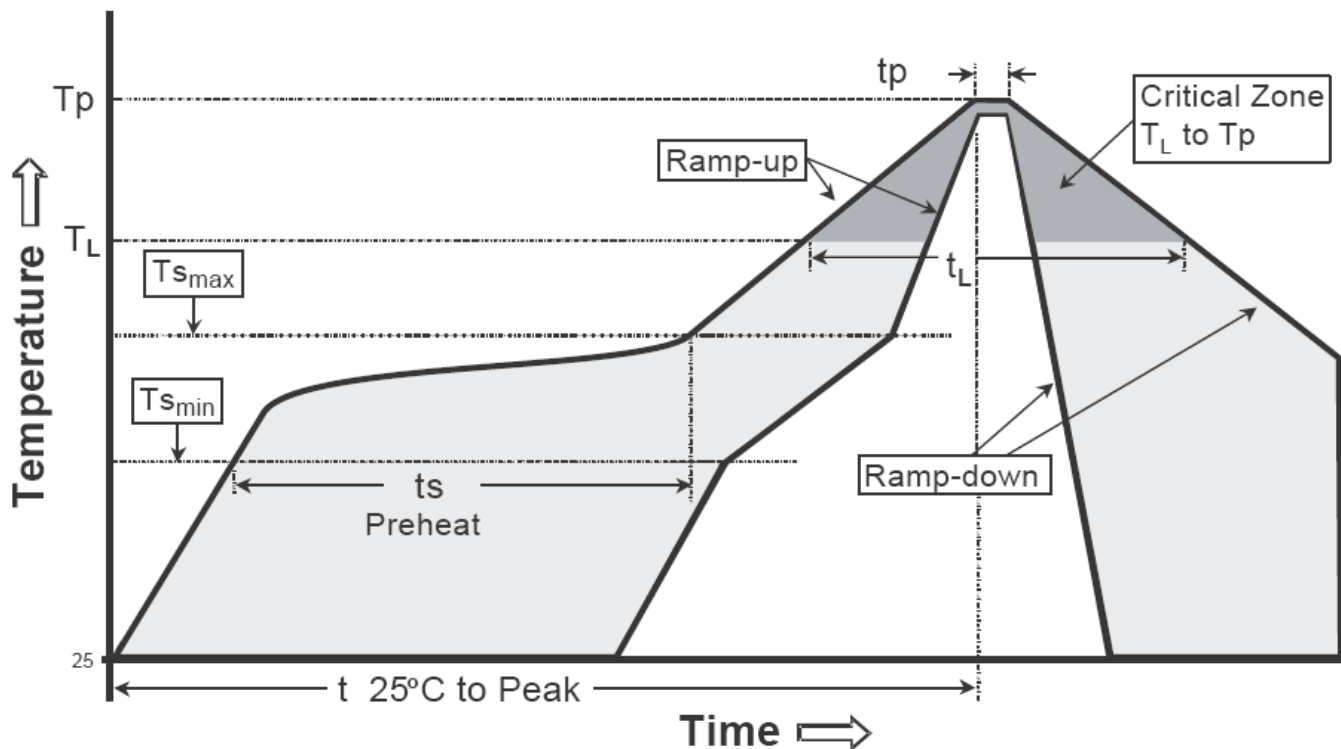




**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

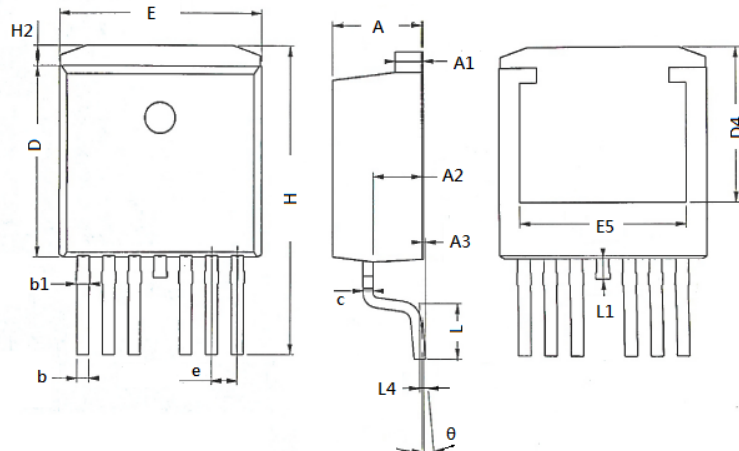
**Recommended temperature profile for IR reflow**



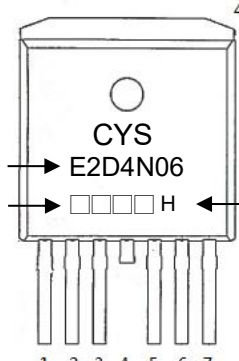
Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

**TO-263-7L-4C Dimension (Site1 forming)**



**Marking :**



Device Name → E2D4N06  
 Date Code → □□□□ H

Assembly site code:  
 H→site 1  
 A→site 2

7-Lead Plastic Surface Mounted TO-263-7L Package  
 CYS Package Code : F7T

Style : Pin 1. Gate  
 Pin 2, 3, 5, 6, 7 : Source  
 Pin 4. Drain

Date Code(counting from left to right) :  
 1<sup>st</sup> code: year code, the last digit of Christian year  
 2<sup>nd</sup> code : month code, Jan→A, Feb→B, Mar→C,  
 Apr→D, May→E, Jun→F, Jul→G, Aug→H,  
 Sep→J, Oct→K, Nov→L, Dec→M  
 3<sup>rd</sup> and 4<sup>th</sup> codes : production serial number, 01~99

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.167	0.179	4.25	4.55	E	0.386	0.402	9.80	10.20
A1	0.047	0.055	1.20	1.40	e	0.050	BSC	1.27	BSC
A2	0.089	0.100	2.25	2.55	E5	0.285	-	7.25	-
A3	0.0004	0.010	0.01	0.25	H	0.577	0.604	14.65	15.35
b	0.020	0.028	0.50	0.70	H2	0.031	0.047	0.80	1.20
b1	0.023	0.033	0.58	0.84	L	0.094	0.118	2.40	3.00
c	0.016	0.024	0.40	0.60	L1	0.033	0.045	0.85	1.15
D	0.356	0.372	9.05	9.45	L4	0.010	BSC	0.25	BSC
D4	0.272	-	6.90	-	θ	2°	8°	2°	8°

Notes : 1.Controlling dimension : millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

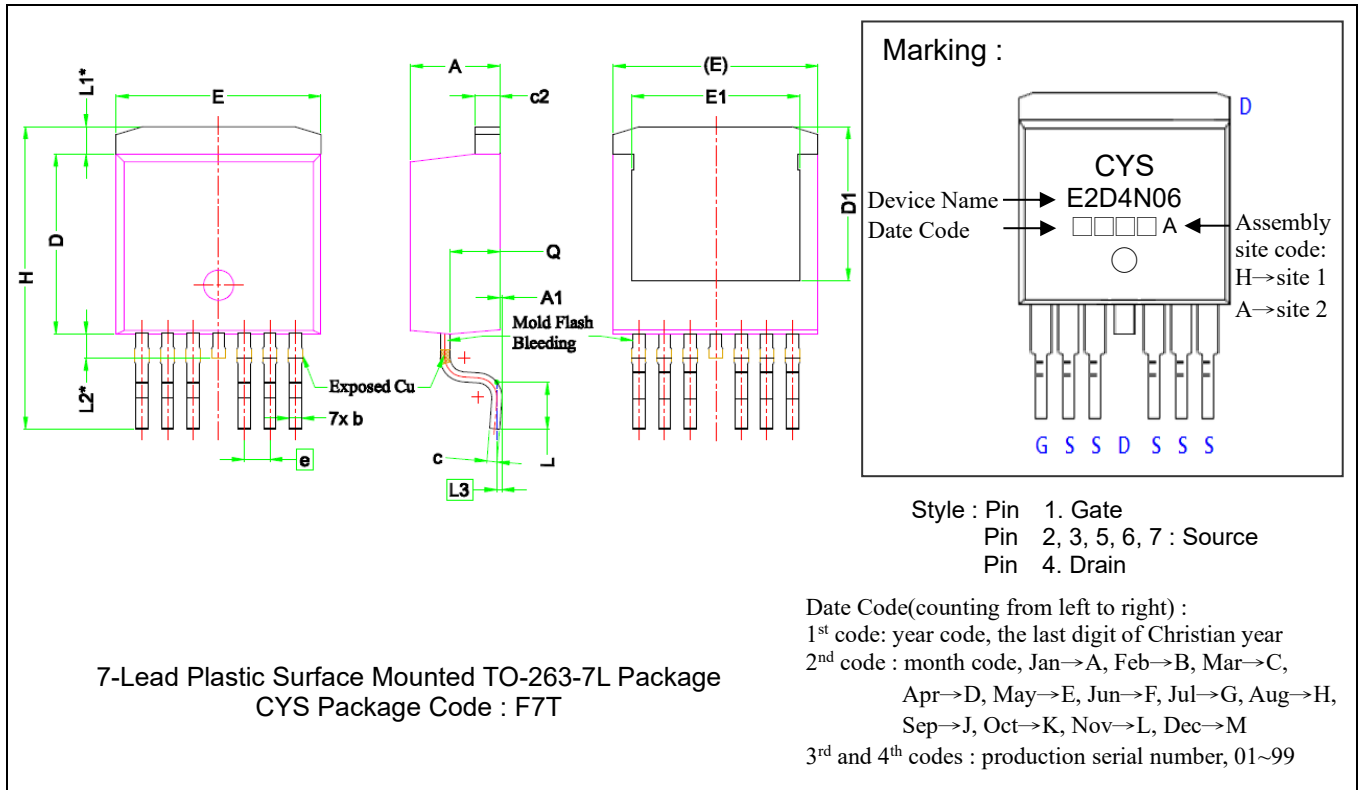
**Material :**

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

**Important Notice:**

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.

**TO-263-7L-4C Dimension (Site2 forming)**



**7-Lead Plastic Surface Mounted TO-263-7L Package**  
 CYS Package Code : F7T

**Marking :**

Device Name → E2D4N06  
 Date Code → □□□□ A

Assembly site code:  
 H → site 1  
 A → site 2

Style : Pin 1. Gate  
 Pin 2, 3, 5, 6, 7 : Source  
 Pin 4. Drain

Date Code(counting from left to right) :  
 1<sup>st</sup> code: year code, the last digit of Christian year  
 2<sup>nd</sup> code : month code, Jan→A, Feb→B, Mar→C,  
 Apr→D, May→E, Jun→F, Jul→G, Aug→H,  
 Sep→J, Oct→K, Nov→L, Dec→M  
 3<sup>rd</sup> and 4<sup>th</sup> codes : production serial number, 01~99

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.167	0.183	4.24	4.64	E1	0.321	0.337	8.15	8.55
A1	0.000	0.010	0.00	0.25	e	0.050 BSC		1.27	BSC
b	0.020	0.028	0.50	0.70	H	0.575	0.625	14.61	15.88
c	0.016	0.024	0.40	0.60	L	0.070	0.110	1.78	2.79
c2	0.045	0.055	1.15	1.40	L1	0.054 REF.		1.36 REF.	
D	0.347	0.355	8.82	9.02	L2	0.047 REF.		1.20 REF.	
D1	0.270	-	6.86	-	L3	0.010 BSC		0.25 BSC	
E	0.392	0.408	9.96	10.36	Q	0.091	0.106	2.30	2.70

**Notes :** 1.Controlling dimension : millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material :**

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

**Important Notice:**

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.