

**P-Channel Enhancement Mode Power MOSFET**

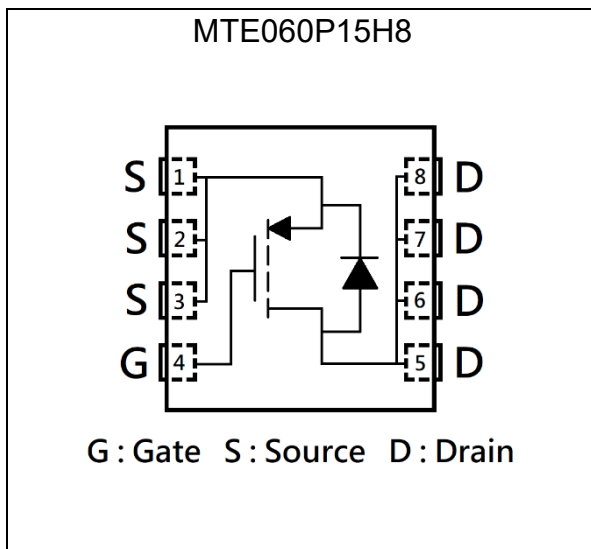
# MTE060P15H8

**Features**

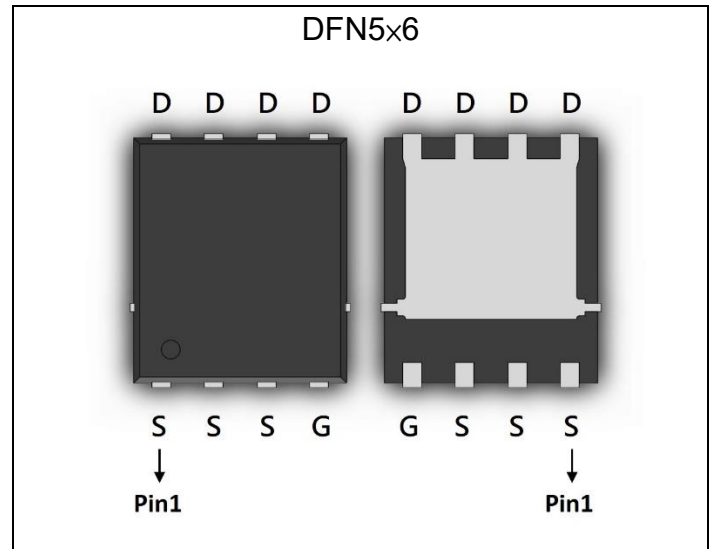
- Low On Resistance
- Low Gate Charge
- Fast Switching Characteristic

$BV_{DSS}$	-150V
$I_D@V_{GS}=-10V, T_C=25^\circ C$	-24A
$I_D@V_{GS}=-10V, T_A=25^\circ C$	-4.4A
$R_{DS(ON) typ.}@V_{GS}=-10V, I_D=-5A$	63mΩ

**Equivalent Circuit**

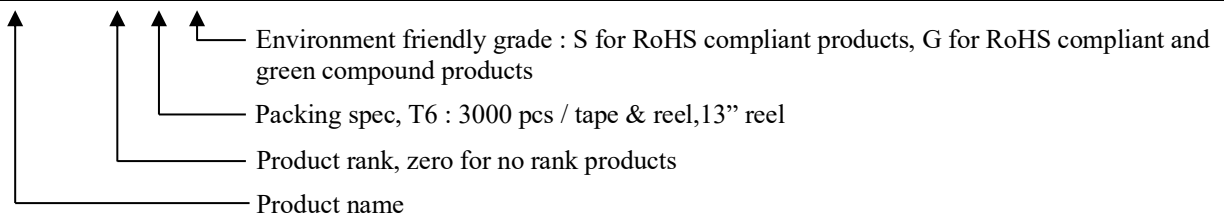


**Outline**



**Ordering Information**

Device	Package	Shipping
MTE060P15H8-0-T6-G	DFN5x6 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel





**Absolute Maximum Ratings (T<sub>A</sub>=25°C)**

Parameter	Symbol	Limits	Unit	
Drain-Source Voltage	V <sub>DS</sub>	-150	V	
Gate-Source Voltage	V <sub>GS</sub>	±20		
Continuous Drain Current @ V <sub>GS</sub> =-10V, T <sub>C</sub> =25°C	I <sub>D</sub>	-24	A	
Continuous Drain Current @ V <sub>GS</sub> =-10V, T <sub>C</sub> =100°C		-15		
Continuous Drain Current @ V <sub>GS</sub> =-10V, T <sub>A</sub> =25°C		-4.4		
Continuous Drain Current @ V <sub>GS</sub> =-10V, T <sub>A</sub> =70°C		-3.5		
Pulsed Drain Current	I <sub>DM</sub>	-96		
Continuous Body Diode Forward Current @ T <sub>C</sub> =25°C	I <sub>S</sub>	-24		
Avalanche Current @ L=0.1mH	I <sub>AS</sub>	-40		
Avalanche Energy @ L=0.5mH	E <sub>AS</sub>	144	mJ	
Total Power Dissipation	P <sub>D</sub>	T <sub>C</sub> =25°C	96	W
		T <sub>C</sub> =100°C	38	
		T <sub>A</sub> =25°C	3	
		T <sub>A</sub> =70°C	2	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55~+150	°C	

**Thermal Data**

Parameter	Symbol	Steady State	Unit
Thermal Resistance, Junction-to-case	R <sub>θJC</sub>	1.3	°C/W
Thermal Resistance, Junction-to-ambient	R <sub>θJA</sub>	41	

Note:

- \*a. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- \*b. The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2 oz. copper, in a still air environment with T<sub>A</sub>=25°C. The power dissipation P<sub>D</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
- \*c. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C. Ratings are based on low frequency and low duty cycles to keep initial T<sub>J</sub>=25°C.



**Electrical Characteristics (T<sub>A</sub>=25°C, unless otherwise specified)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
<b>Static</b>					
BV <sub>DSS</sub>	-150	-	-	V	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA
V <sub>GS(th)</sub>	-2	-	-4		V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA
G <sub>FS</sub>	-	29	-	S	V <sub>DS</sub> =-10V, I <sub>D</sub> =-20A
I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V
I <sub>DSS</sub>	-	-	-1	μA	V <sub>DS</sub> =-120V, V <sub>GS</sub> =0V
R <sub>DS(on)</sub>	-	63	82	mΩ	V <sub>GS</sub> =-10V, I <sub>D</sub> =-5A
<b>Dynamic</b>					
C <sub>iss</sub>	-	4200	-	pF	V <sub>DS</sub> =-75V, V <sub>GS</sub> =0V, f=1MHz
C <sub>oss</sub>	-	190	-		
C <sub>rss</sub>	-	100	-		
R <sub>g</sub>	-	3	-	Ω	f=1MHz
Q <sub>g</sub> *1, 2	-	76	-	nC	V <sub>DS</sub> =-75V, I <sub>D</sub> =-5A, V <sub>GS</sub> =-10V
Q <sub>gs</sub> *1, 2	-	17	-		
Q <sub>gd</sub> *1, 2	-	19	-		
t <sub>d(ON)</sub> *1, 2	-	33	-	ns	V <sub>DS</sub> =-75V, I <sub>D</sub> =-5A, V <sub>GS</sub> =-10V, R <sub>GS</sub> =6Ω
t <sub>r</sub> *1, 2	-	30	-		
t <sub>d(OFF)</sub> *1, 2	-	106	-		
t <sub>f</sub> *1, 2	-	37	-		
<b>Source-Drain Diode</b>					
V <sub>SD</sub> *1	-	-0.8	-1.2	V	I <sub>S</sub> =-5A, V <sub>GS</sub> =0V
t <sub>rr</sub>	-	50	-	ns	I <sub>F</sub> =-5A, dI <sub>F</sub> /dt=100A/μs
Q <sub>rr</sub>	-	118	-	nC	

Note:

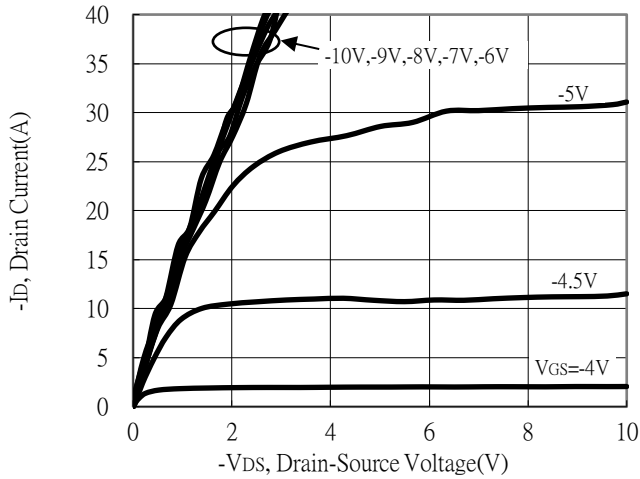
\*1. Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

\*2. Independent of operating temperature

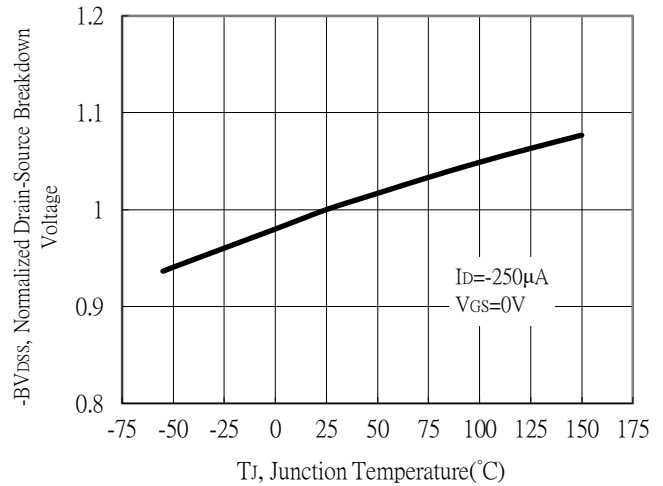


**Typical Characteristics**

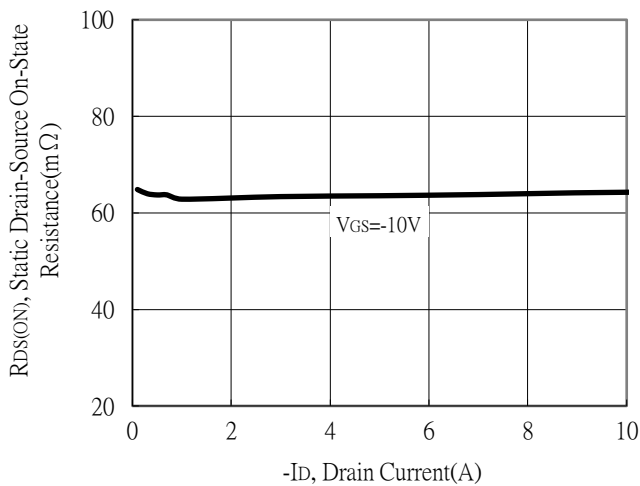
Typical Output Characteristics



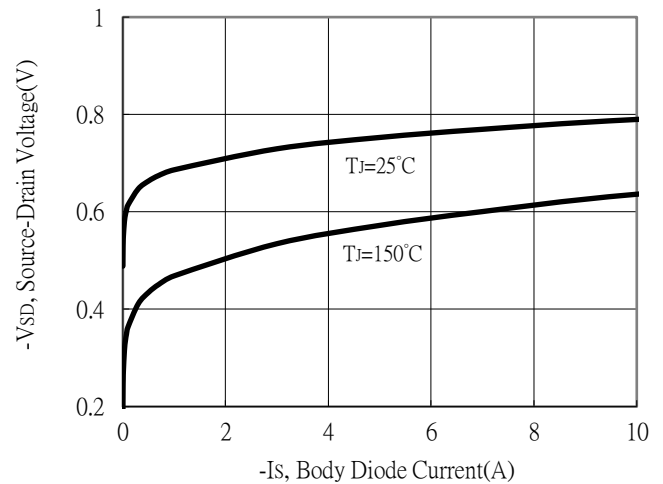
Breakdown Voltage vs Ambient Temperature



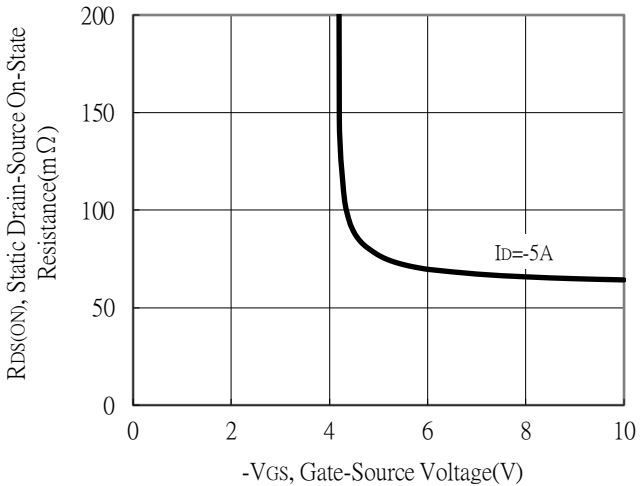
Static Drain-Source On-State resistance vs Drain Current



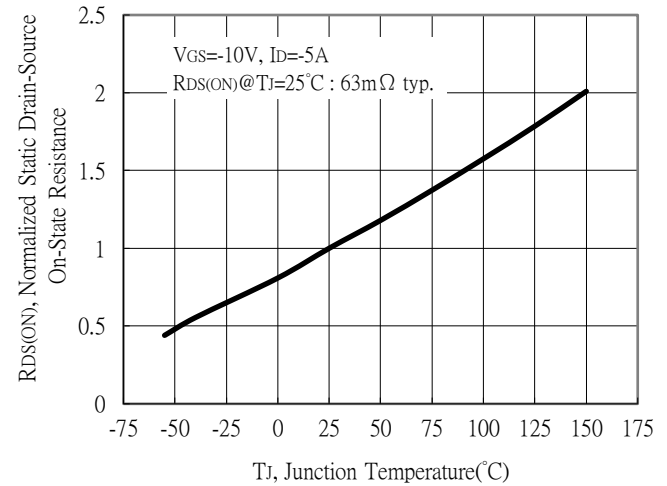
Body Diode Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage



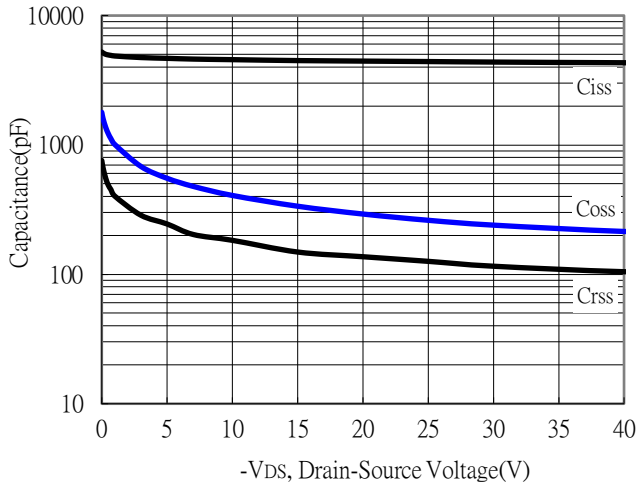
Drain-Source On-State Resistance vs Junction Temperature



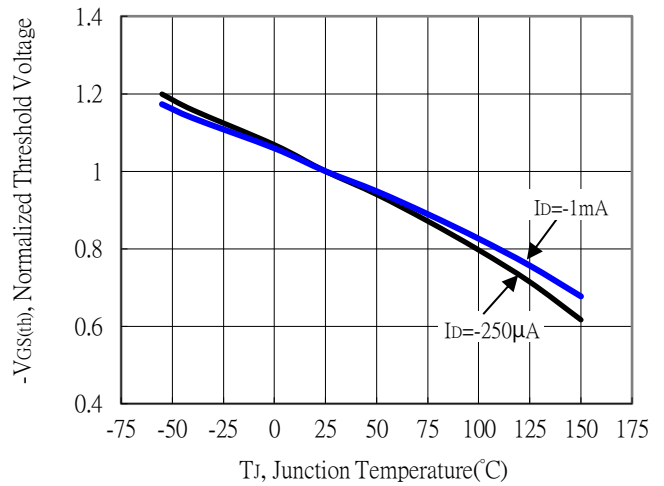


**Typical Characteristics (Cont.)**

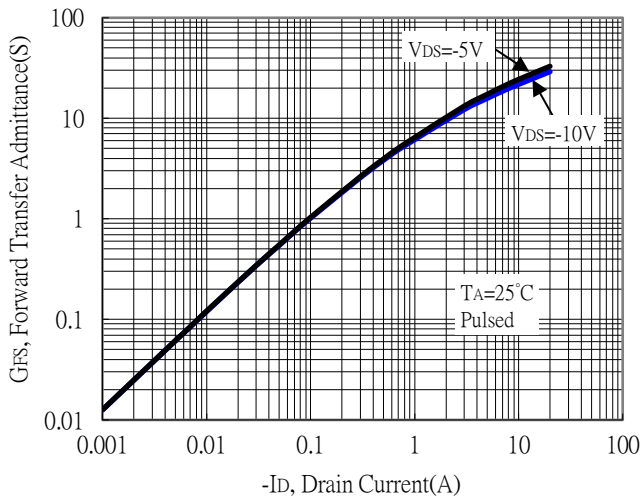
Capacitance vs Drain-to-Source Voltage



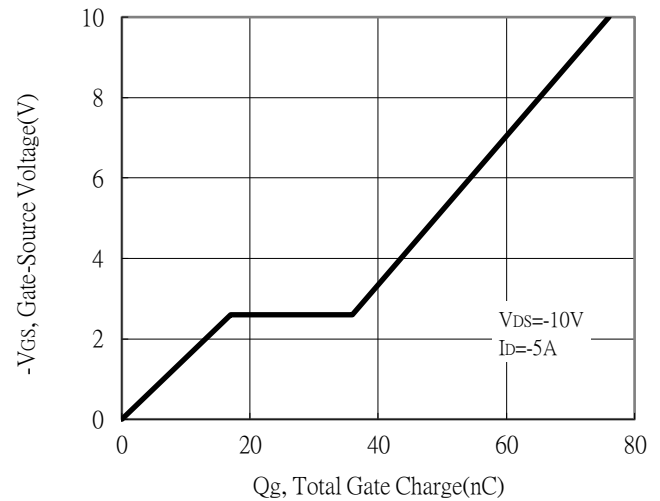
Threshold Voltage vs Junction Temperature



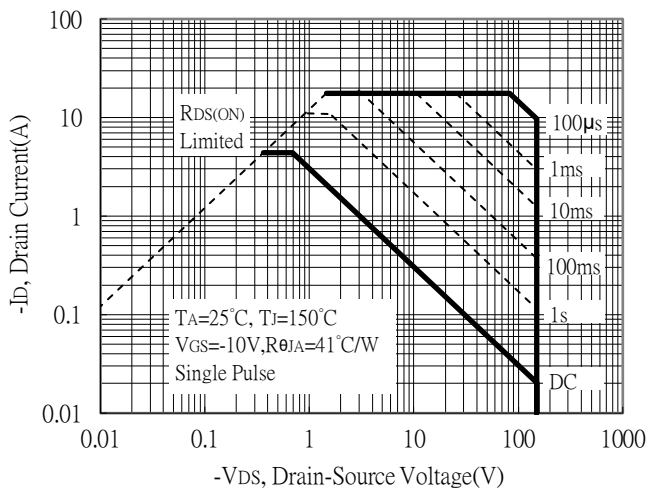
Forward Transfer Admittance vs Drain Current



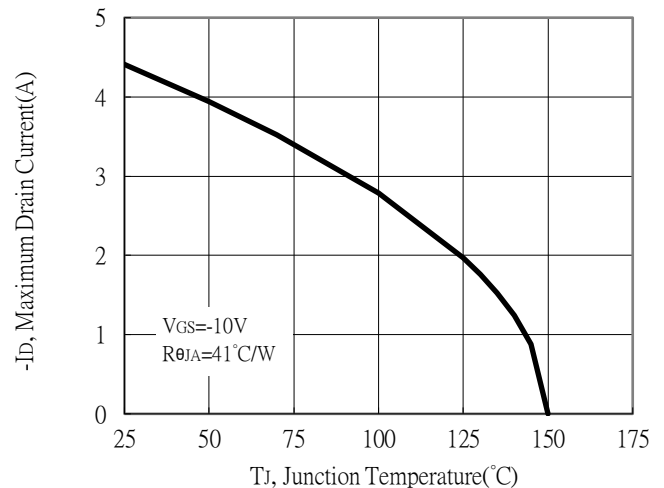
Gate Charge Characteristics



Maximum Safe Operating Area

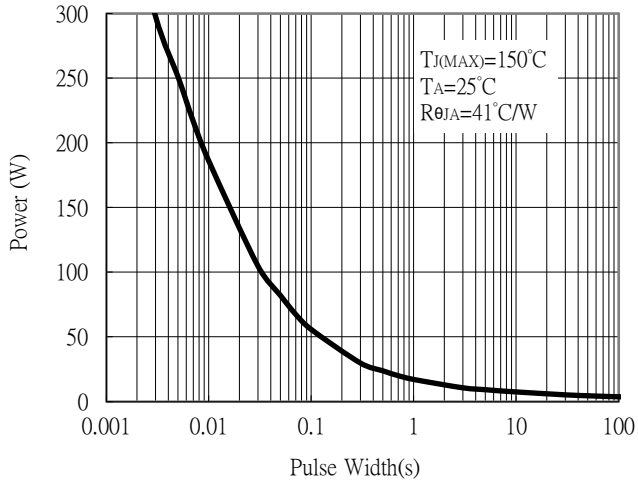


Maximum Drain Current vs Junction Temperature

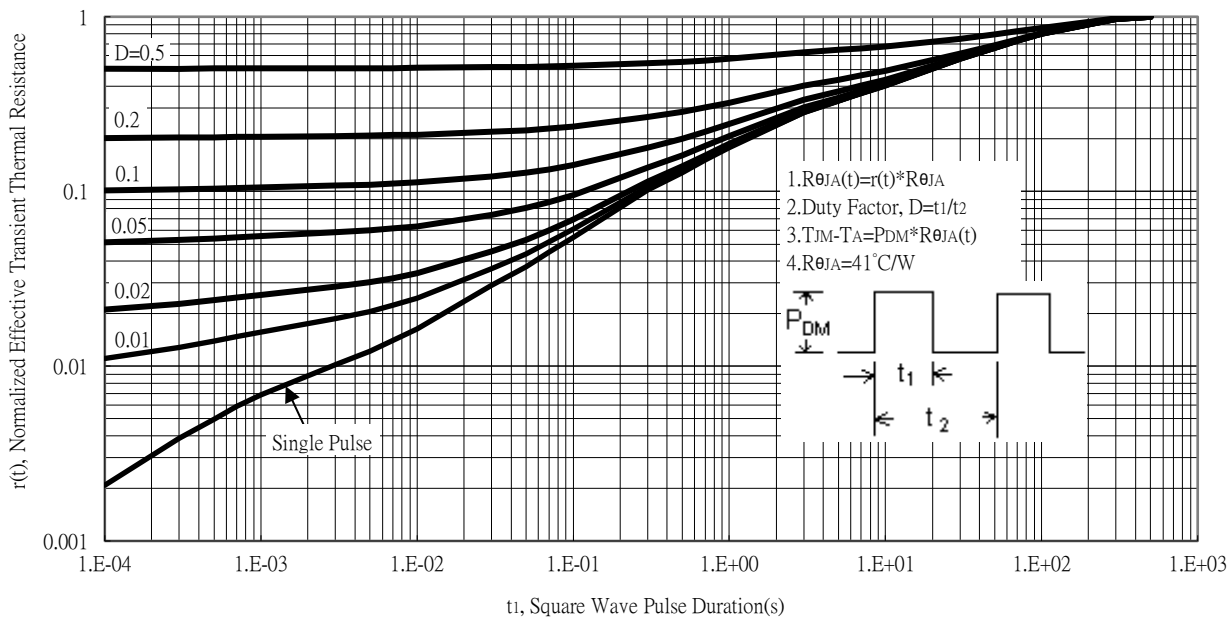


**Typical Characteristics (Cont.)**

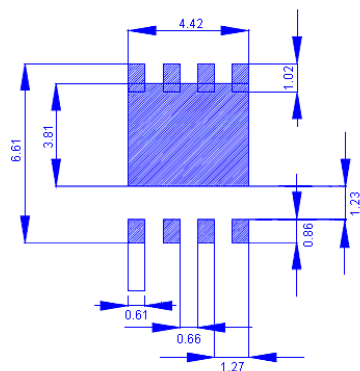
Single Pulse Power Rating, Junction to Ambient



Transient Thermal Response Curves

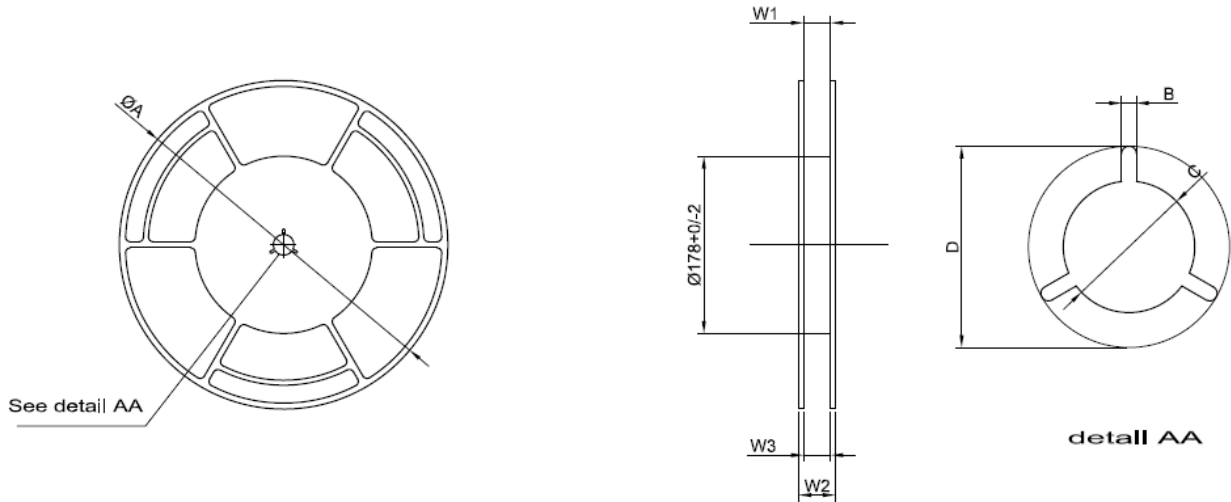


**Recommended Soldering Footprint**



Unit : mm

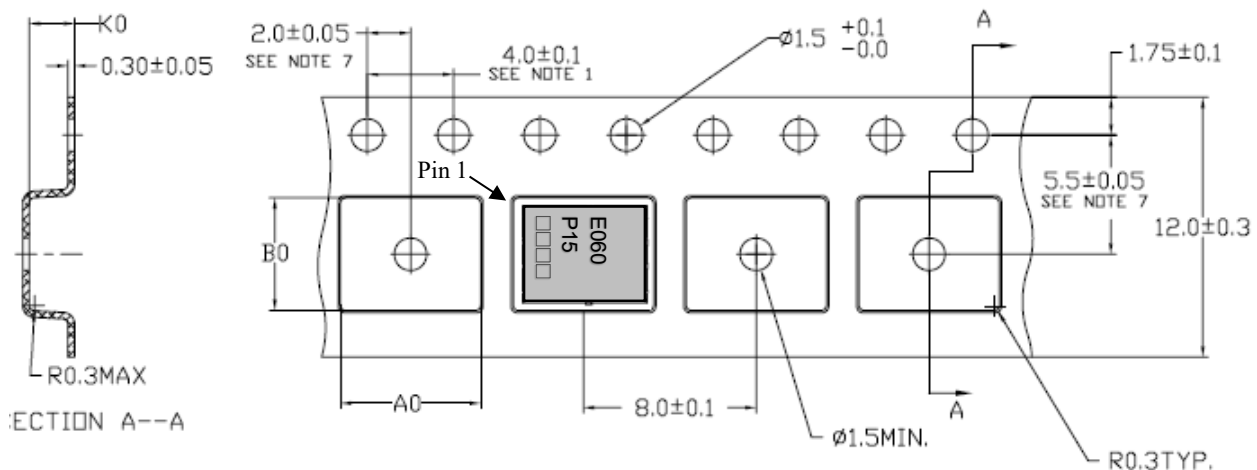
**Reel Dimension**



TAPE SIZE	A	B	C	D	W1	W2	W3
12mm	$330\pm2.0$	$2.9\pm0.5$	$13.0\pm0.5/-0$	$23\pm1.0$	$12.4\ +2/-0$	$18.4\pm0.5$	12~15

Unit : mm

**Carrier Tape Dimension**



- NOTE:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE  $\pm0.2$
  2. CAMBER NOT TO EXCEED 1mm IN 100mm, NONCUMULATIVE OVER 250mm.
  3. MATERIAL: BLACK STATIC DISSIPATIVE PS.(POLYSTYRENE)
  4. ALL DIMENSIONS ARE IN MILLIMETERS (UNLESS OTHERWISE SPECIFIED)
  5. A0 AND B0 MEASURED ON A PLANE 0.3mm ABOVE THE BOTTOM OF THE POCKET
  6. K0 MEASURED FROM A PLANE ON THE INSIDE BOTTOM OF THE POCKET TO THE TOP SURFACE OF THE CARRIER
  7. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE
  8. SURFACE RESISTIVITY  
 $1\times10^4\sim1\times10^11\ \text{OHMS}/\text{SQ.}$

Direction of unreeling →

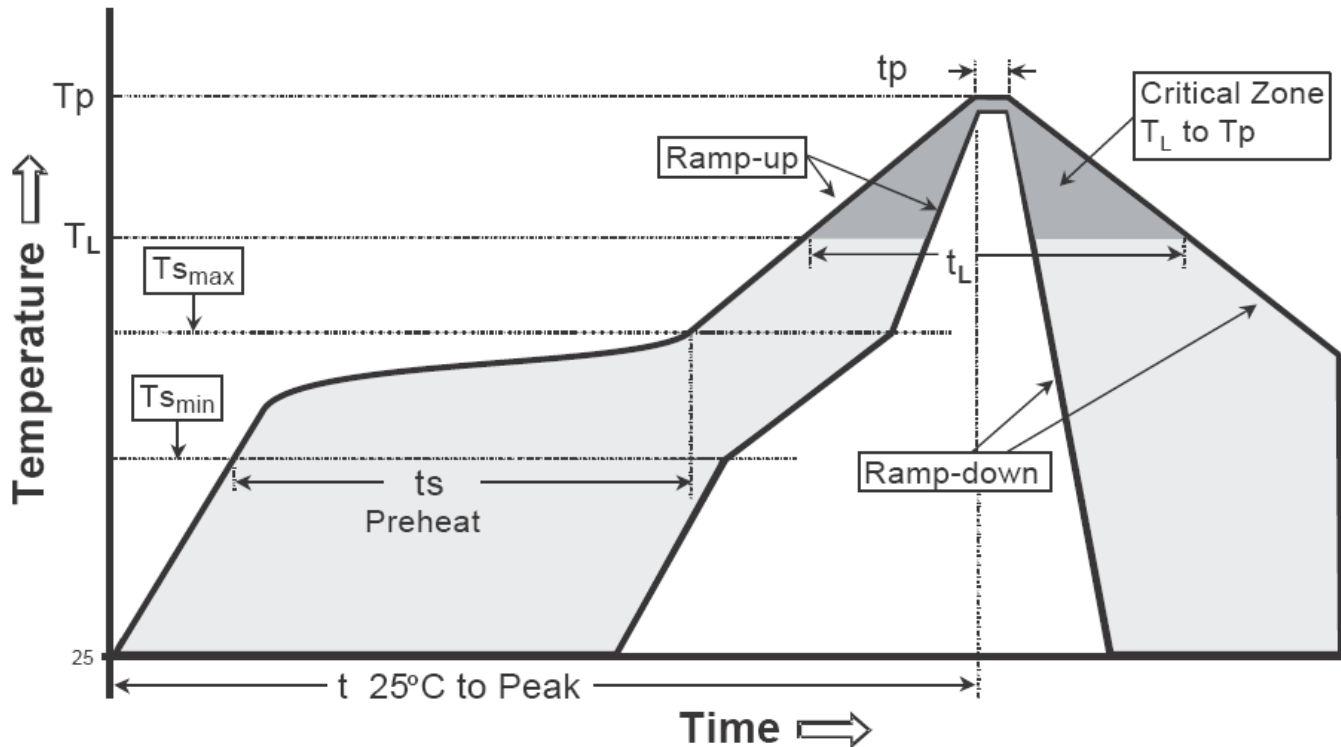
A0= $6.5\pm0.1$   
 B0= $5.3\pm0.1$   
 K0= $1.4\pm0.1$

Unit : mm

**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

**Recommended temperature profile for IR reflow**

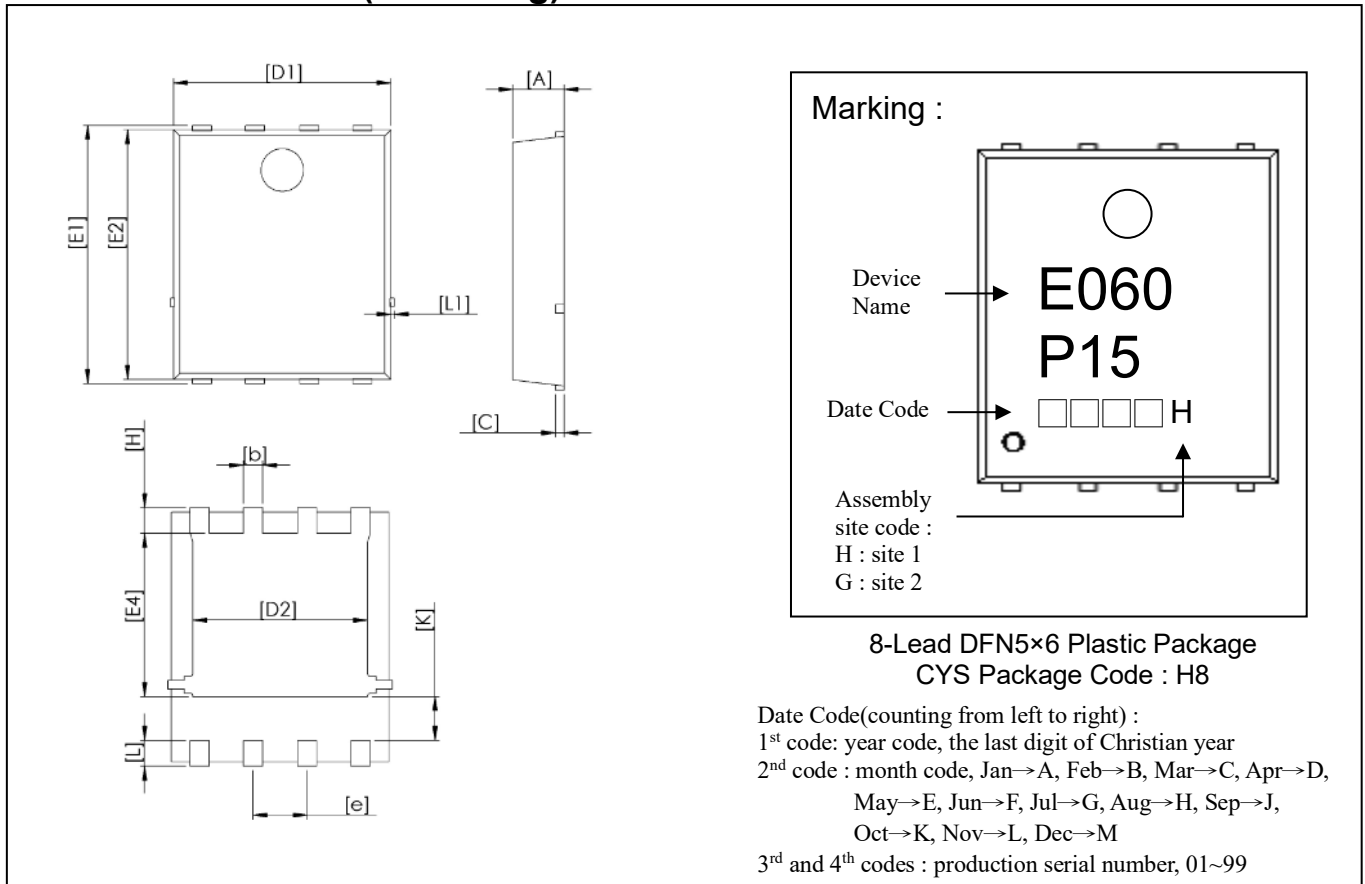


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T <sub>s min</sub> )	100°C	150°C
-Temperature Max(T <sub>s max</sub> )	150°C	200°C
-Time(t <sub>s min</sub> to t <sub>s max</sub> )	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T <sub>L</sub> )	183°C	217°C
- Time (t <sub>L</sub> )	60-150 seconds	60-150 seconds
Peak Temperature(T <sub>P</sub> )	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.



**DFN5x6 Dimension (H forming)**



**Marking :**

Device Name → E060  
 P15

Date Code → □ □ □ □ H

Assembly site code :  
 H : site 1  
 G : site 2

**8-Lead DFN5x6 Plastic Package**  
 CYS Package Code : H8

Date Code(counting from left to right) :  
 1<sup>st</sup> code: year code, the last digit of Christian year  
 2<sup>nd</sup> code : month code, Jan→A, Feb→B, Mar→C, Apr→D,  
 May→E, Jun→F, Jul→G, Aug→H, Sep→J,  
 Oct→K, Nov→L, Dec→M  
 3<sup>rd</sup> and 4<sup>th</sup> codes : production serial number, 01~99

DIM	Millimeters		Inches		DIM	Millimeters		DIM	
	Min.	Max.	Min.	Min.		Min.	Max.	Min.	Max.
A	1.000	1.200	0.0394	0.0472	E2	5.660	6.060	0.2228	0.2386
b	0.300	0.500	0.0118	0.0197	E4	3.520	3.920	0.1386	0.1543
C	0.154	0.354	0.0061	0.0139	H	0.400	0.600	0.0157	0.0236
D1	5.050	5.450	0.1988	0.2145	K	1.34 REF		0.0527 REF	
D2	3.800	4.250	0.1496	0.1673	L	0.300	0.700	0.0118	0.0276
e	1.170	1.370	0.0461	0.0539	L1	0.000	0.120	0.0000	0.0047
E1	5.950	6.350	0.2343	0.2500					

**Notes:** 1.Controlling dimension: millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

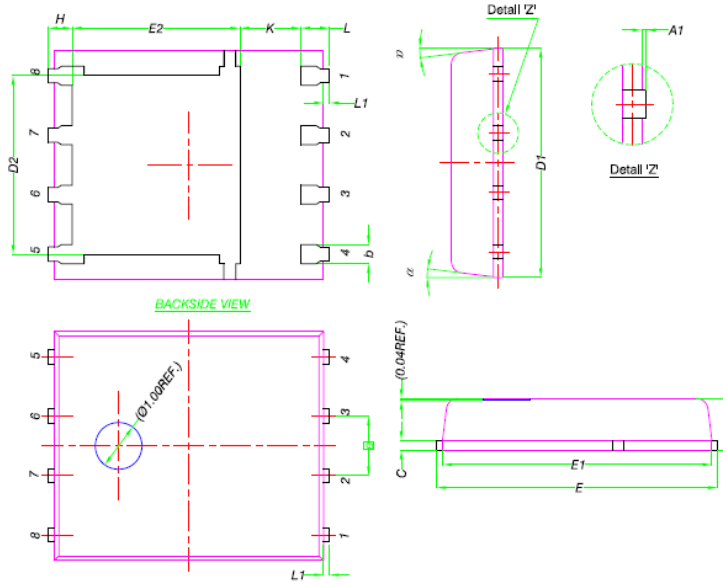
**Material:**

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

**Important Notice:**

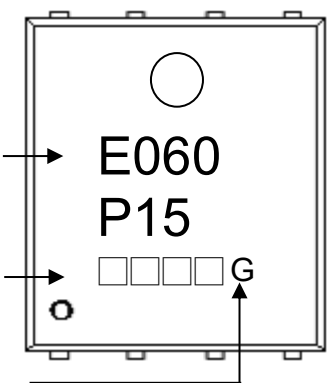
- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.

## DFN5x6 Dimension (G forming)



**8-Lead DFN5x6 Plastic Package**  
 CYS Package Code : H8

**Marking:**



Device Code → **E060**  
**P15**

Date Code →     **G**

Assembly site code :  
 H : site 1  
 G : site 2

Date Code(counting from left to right) :

1<sup>st</sup> code: year code, the last digit of Christian year

2<sup>nd</sup> code : month code, Jan→A, Feb→B, Mar→C, Apr→D, May→E, Jun→F, Jul→G, Aug→H, Sep→J, Oct→K, Nov→L, Dec→M

3<sup>rd</sup> and 4<sup>th</sup> codes : production serial number, 01~99

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.90	1.10	0.035	0.043	E2	3.38	3.78	0.133	0.149
A1	0.00	0.05	0.000	0.002	e	1.27	BSC	0.050	BSC
b	0.33	0.51	0.013	0.020	H	0.41	0.61	0.016	0.024
C	0.20	0.30	0.008	0.012	K	1.10	-	0.043	-
D1	4.80	5.00	0.189	0.197	L	0.51	0.71	0.020	0.028
D2	3.61	3.96	0.142	0.156	L1	0.06	0.20	0.002	0.008
E	5.90	6.10	0.232	0.240	α	0°	12°	0°	12°
E1	5.70	5.80	0.224	0.228					

**Notes:** 1.Controlling dimension: millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

**Important Notice:**

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.