

**P-Channel Enhancement Mode Power MOSFET**

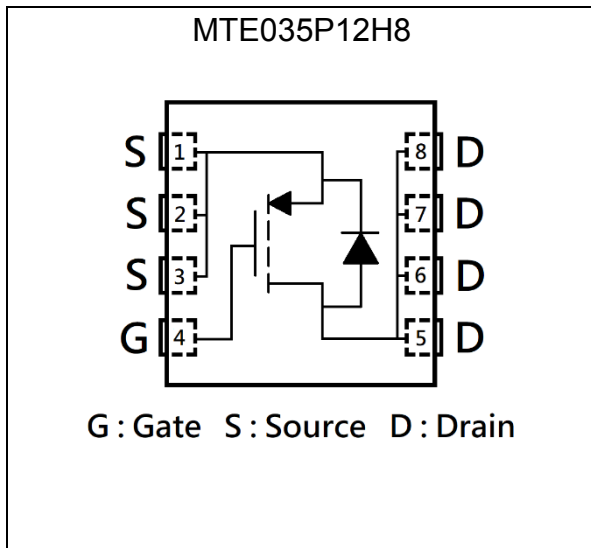
# MTE035P12H8

**Features**

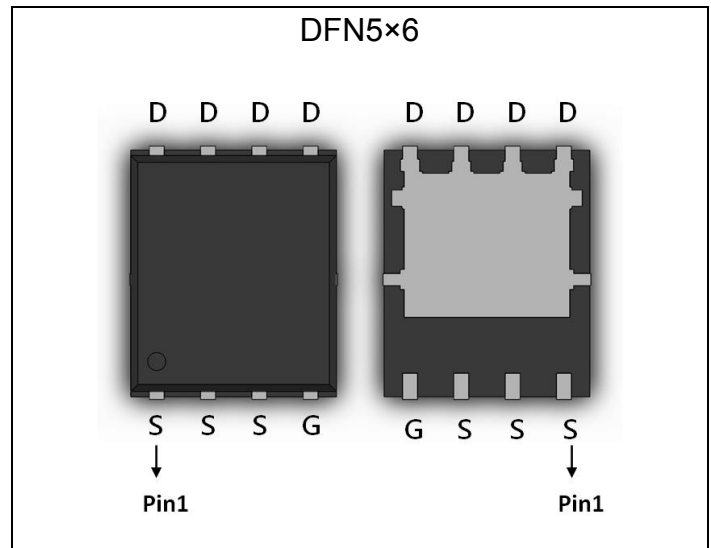
- Low On Resistance
- Low Gate Charge
- Fast Switching Characteristic

$BV_{DSS}$	-120V
$I_D@V_{GS}=-10V, T_C=25^{\circ}C$	-27A
$I_D@V_{GS}=-10V, T_A=25^{\circ}C$	-6A
$R_{DS(ON) typ. @V_{GS}=-10V, I_D=-5A}$	36mΩ

**Equivalent Circuit**

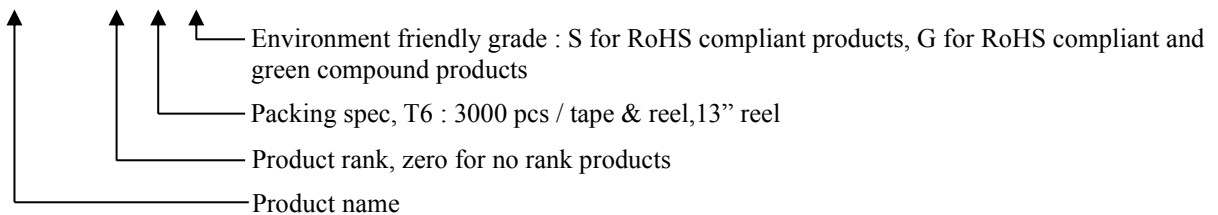


**Outline**



**Ordering Information**

Device	Package	Shipping
MTE035P12H8-0-T6-G	DFN5×6 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel





**Absolute Maximum Ratings (TA=25°C)**

Parameter	Symbol	Limits	Unit	
Drain-Source Voltage	V <sub>DS</sub>	-120	V	
Gate-Source Voltage	V <sub>GS</sub>	±20		
Continuous Drain Current @ V <sub>GS</sub> =-10V, T <sub>C</sub> =25°C	I <sub>D</sub>	-27	A	
Continuous Drain Current @ V <sub>GS</sub> =-10V, T <sub>C</sub> =100°C		-17		
Continuous Drain Current @ V <sub>GS</sub> =-10V, T <sub>A</sub> =25°C		-6		
Continuous Drain Current @ V <sub>GS</sub> =-10V, T <sub>A</sub> =70°C		-4.8		
Pulsed Drain Current		I <sub>DM</sub>		-108
Continuous Body Diode Forward Current @ T <sub>C</sub> =25°C	I <sub>S</sub>	-27		
Avalanche Current @ L=0.1mH	I <sub>AS</sub>	-45		
Avalanche Energy @ L=0.5mH	E <sub>AS</sub>	156	mJ	
Total Power Dissipation	P <sub>D</sub>	T <sub>C</sub> =25°C	70	W
		T <sub>C</sub> =100°C	28	
		T <sub>A</sub> =25°C	3.3	
		T <sub>A</sub> =70°C	2.1	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55~+150	°C	

**Thermal Data**

Parameter	Symbol	Steady State	Unit
Thermal Resistance, Junction-to-case	R <sub>θJC</sub>	1.5	°C/W
Thermal Resistance, Junction-to-ambient	R <sub>θJA</sub>	38	

Note:

- \*a. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- \*b. The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2 oz. copper, in a still air environment with T<sub>A</sub>=25°C. The power dissipation P<sub>D</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
- \*c. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C. Ratings are based on low frequency and low duty cycles to keep initial T<sub>J</sub>=25°C.



**Electrical Characteristics (T<sub>A</sub>=25°C, unless otherwise specified)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
<b>Static</b>					
BV <sub>DSS</sub>	-120	-	-	V	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA
V <sub>GS(th)</sub>	-2	-	-4		V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA
G <sub>FS</sub>	-	16	-	S	V <sub>DS</sub> =-5V, I <sub>D</sub> =-5A
I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V
I <sub>DSS</sub>	-	-	-1	μA	V <sub>DS</sub> =-96V, V <sub>GS</sub> =0V
R <sub>DS(ON)</sub>	-	36	48	mΩ	V <sub>GS</sub> =-10V, I <sub>D</sub> =-5A
<b>Dynamic</b>					
C <sub>iSS</sub>	-	4600	-	pF	V <sub>DS</sub> =-60V, V <sub>GS</sub> =0V, f=1MHz
C <sub>oSS</sub>	-	206	-		
C <sub>rSS</sub>	-	128	-		
R <sub>g</sub>	-	6	-	Ω	f=1MHz
Q <sub>g</sub> *1, 2	-	80	-	nC	V <sub>DS</sub> =-60V, I <sub>D</sub> =-5A, V <sub>GS</sub> =-10V
Q <sub>gs</sub> *1, 2	-	19	-		
Q <sub>gd</sub> *1, 2	-	22	-		
t <sub>d(ON)</sub> *1, 2	-	28	-	ns	V <sub>DS</sub> =-60V, I <sub>D</sub> =-5A, V <sub>GS</sub> =-10V, R <sub>GS</sub> =6Ω
t <sub>r</sub> *1, 2	-	35	-		
t <sub>d(OFF)</sub> *1, 2	-	141	-		
t <sub>f</sub> *1, 2	-	58	-		
<b>Source-Drain Diode</b>					
V <sub>SD</sub> *1	-	-0.77	-1.2	V	I <sub>S</sub> =-5A, V <sub>GS</sub> =0V
t <sub>rr</sub>	-	41	-	ns	I <sub>F</sub> =-5A, dI <sub>F</sub> /dt=100A/μs
Q <sub>rr</sub>	-	79	-	nC	

Note:

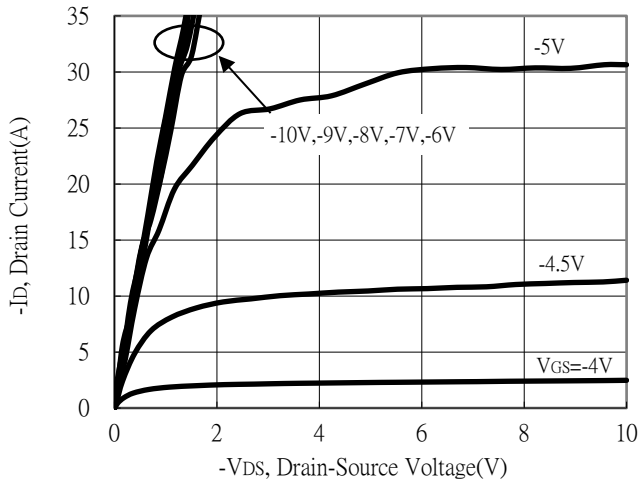
\*1. Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

\*2. Independent of operating temperature

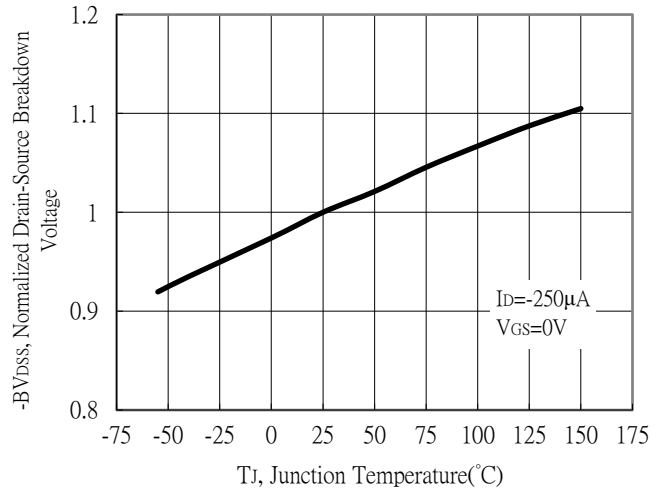


**Typical Characteristics**

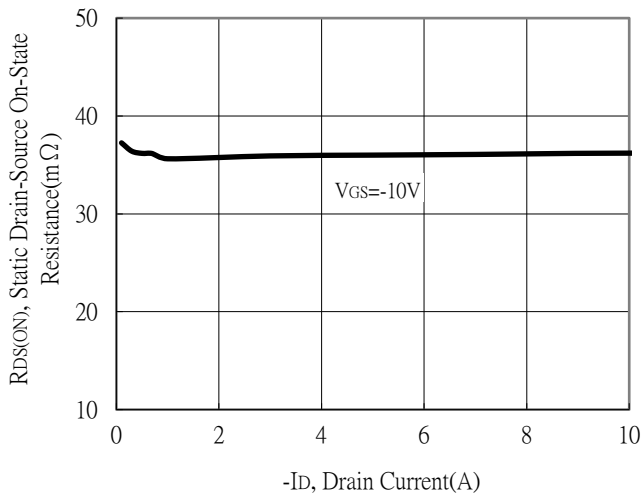
Typical Output Characteristics



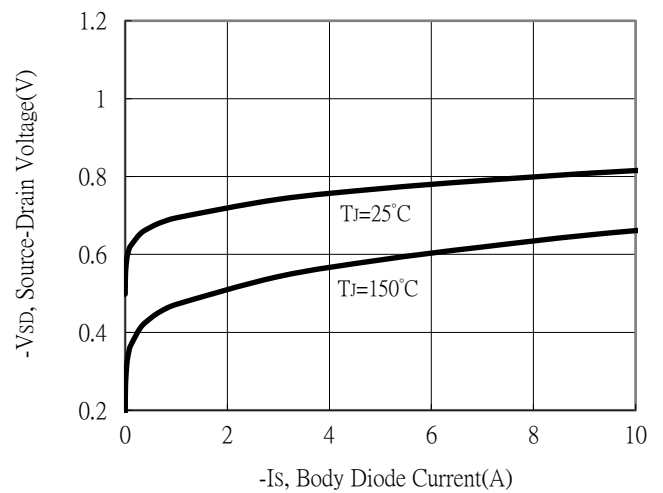
Breakdown Voltage vs Ambient Temperature



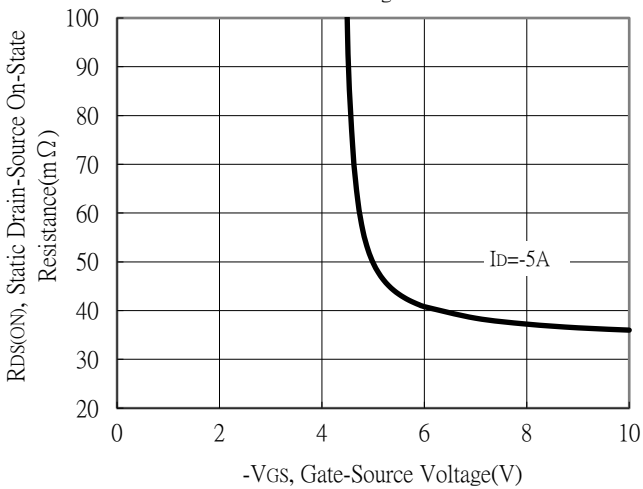
Static Drain-Source On-State resistance vs Drain Current



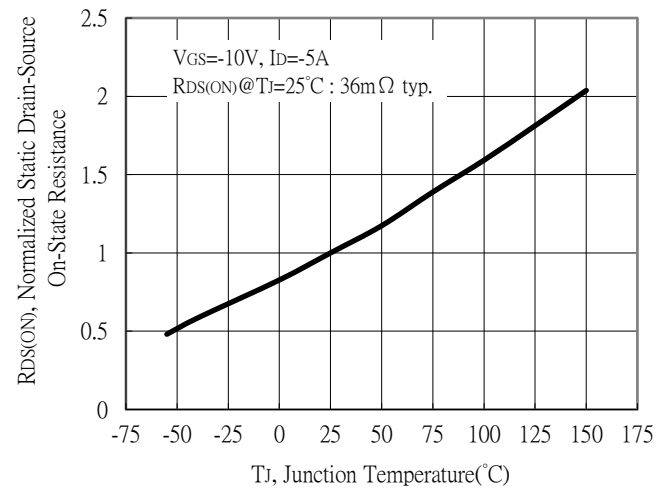
Body Diode Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage



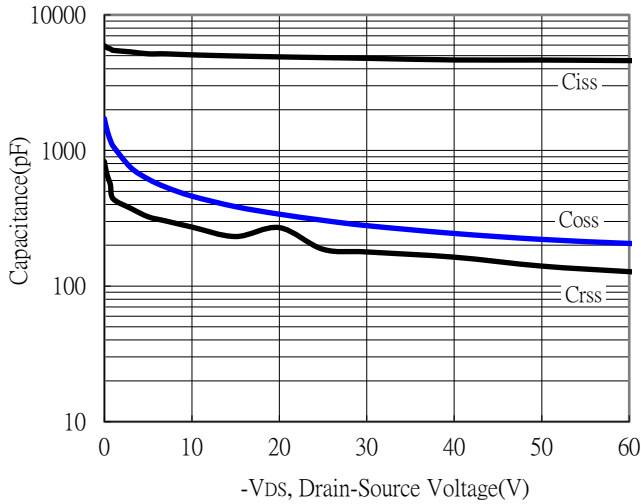
Drain-Source On-State Resistance vs Junction Temperature



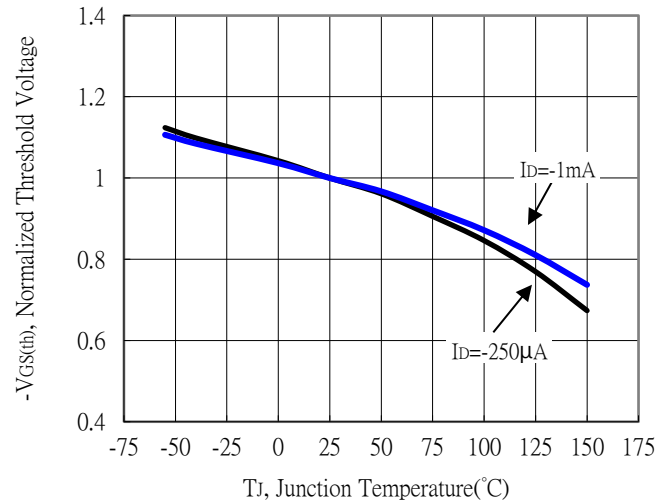


**Typical Characteristics (Cont.)**

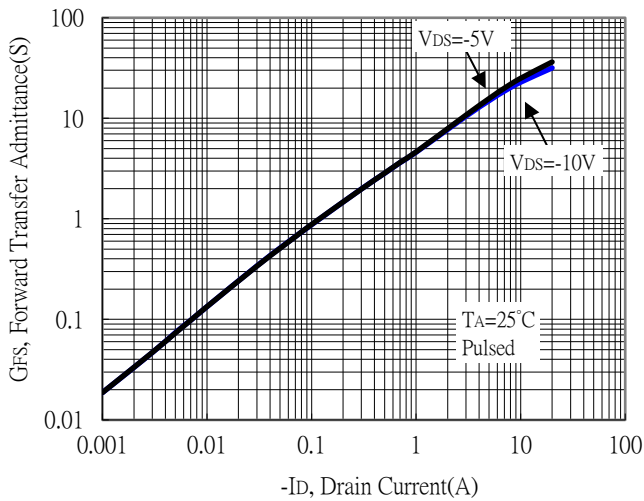
Capacitance vs Drain-to-Source Voltage



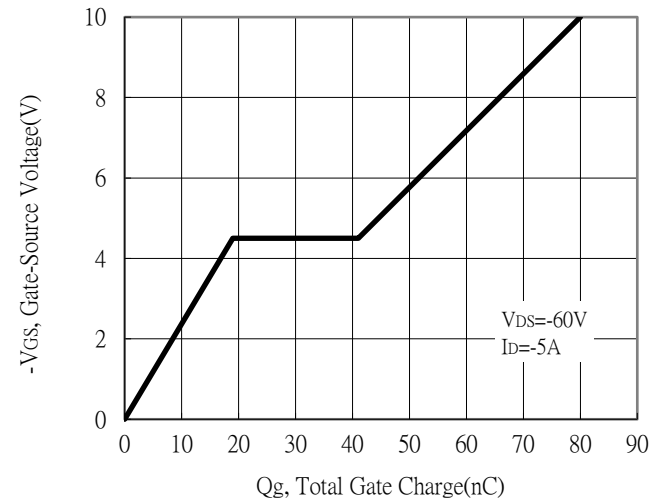
Threshold Voltage vs Junction Temperature



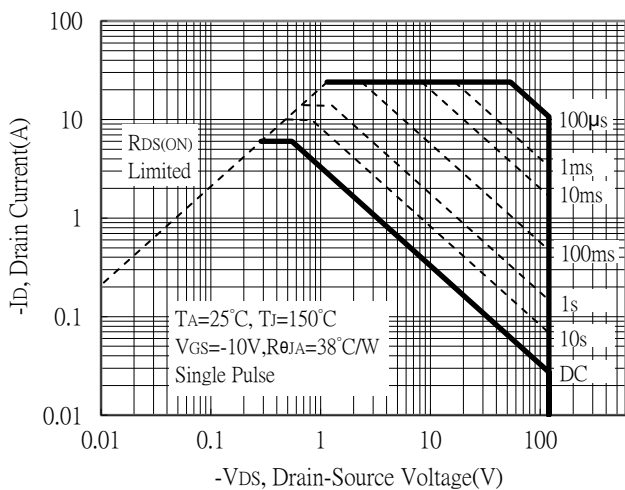
Forward Transfer Admittance vs Drain Current



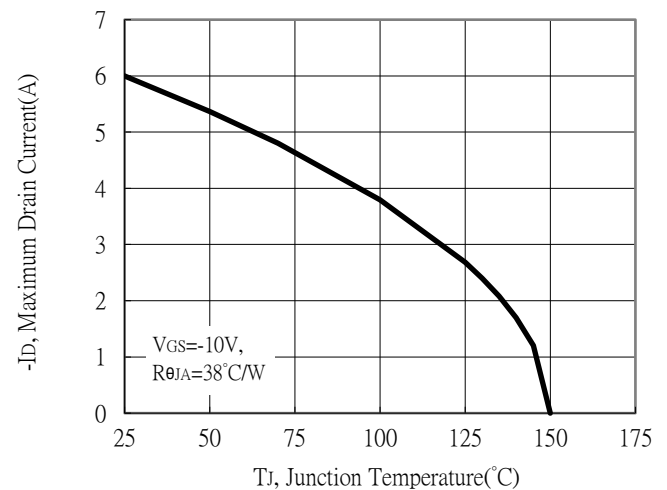
Gate Charge Characteristics



Maximum Safe Operating Area



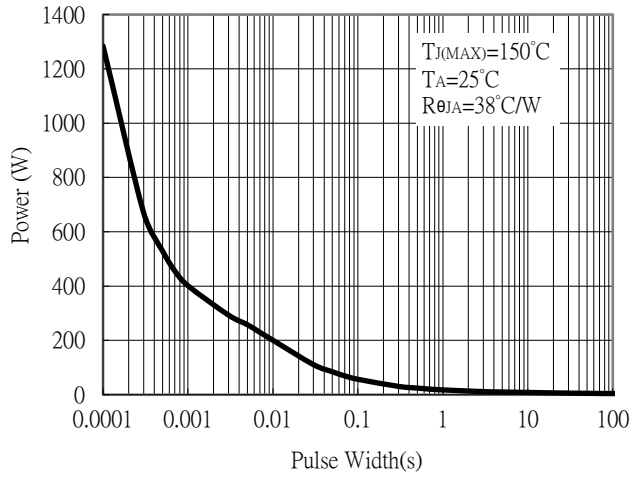
Maximum Drain Current vs Junction Temperature



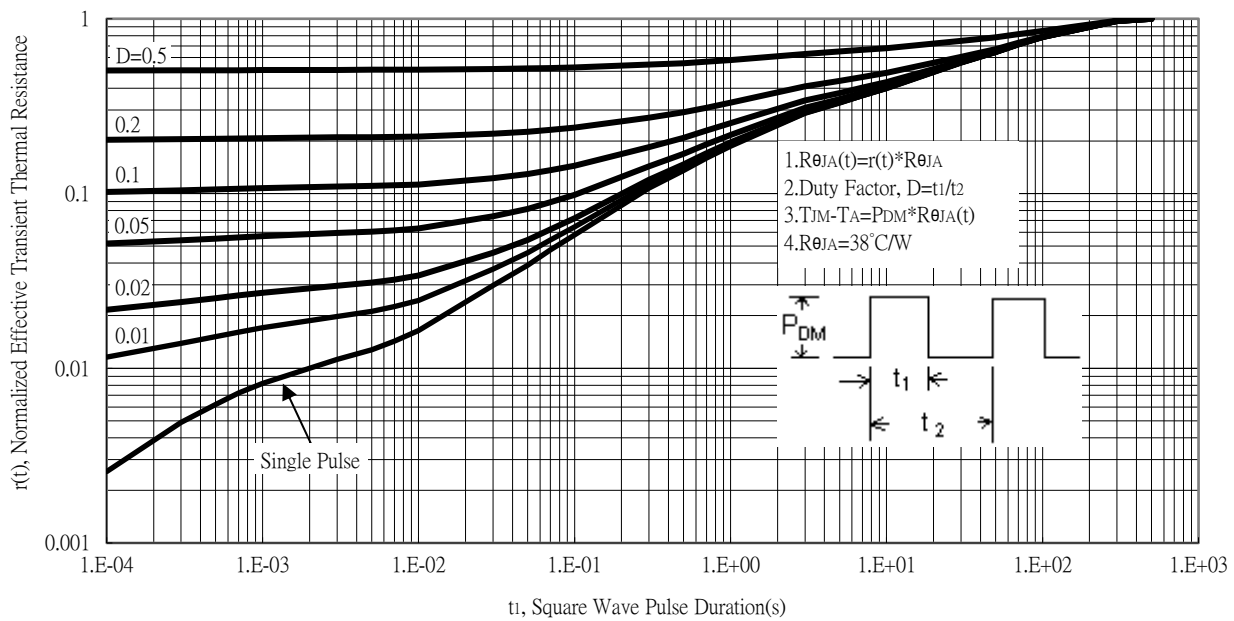


### Typical Characteristics (Cont.)

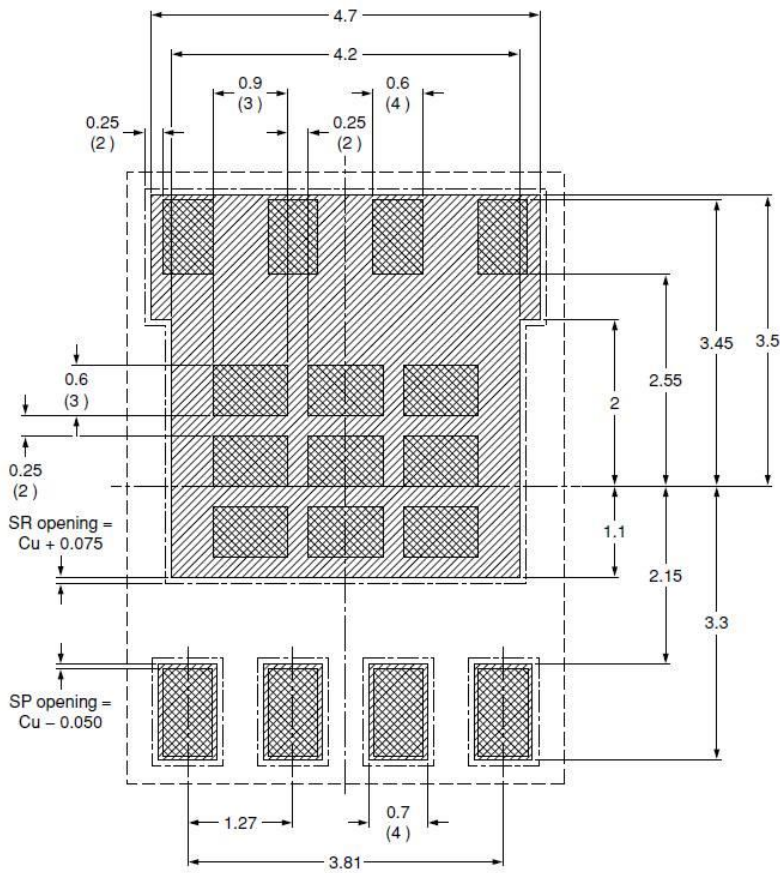
Single Pulse Power Rating, Junction to Ambient







Transient Thermal Response Curves



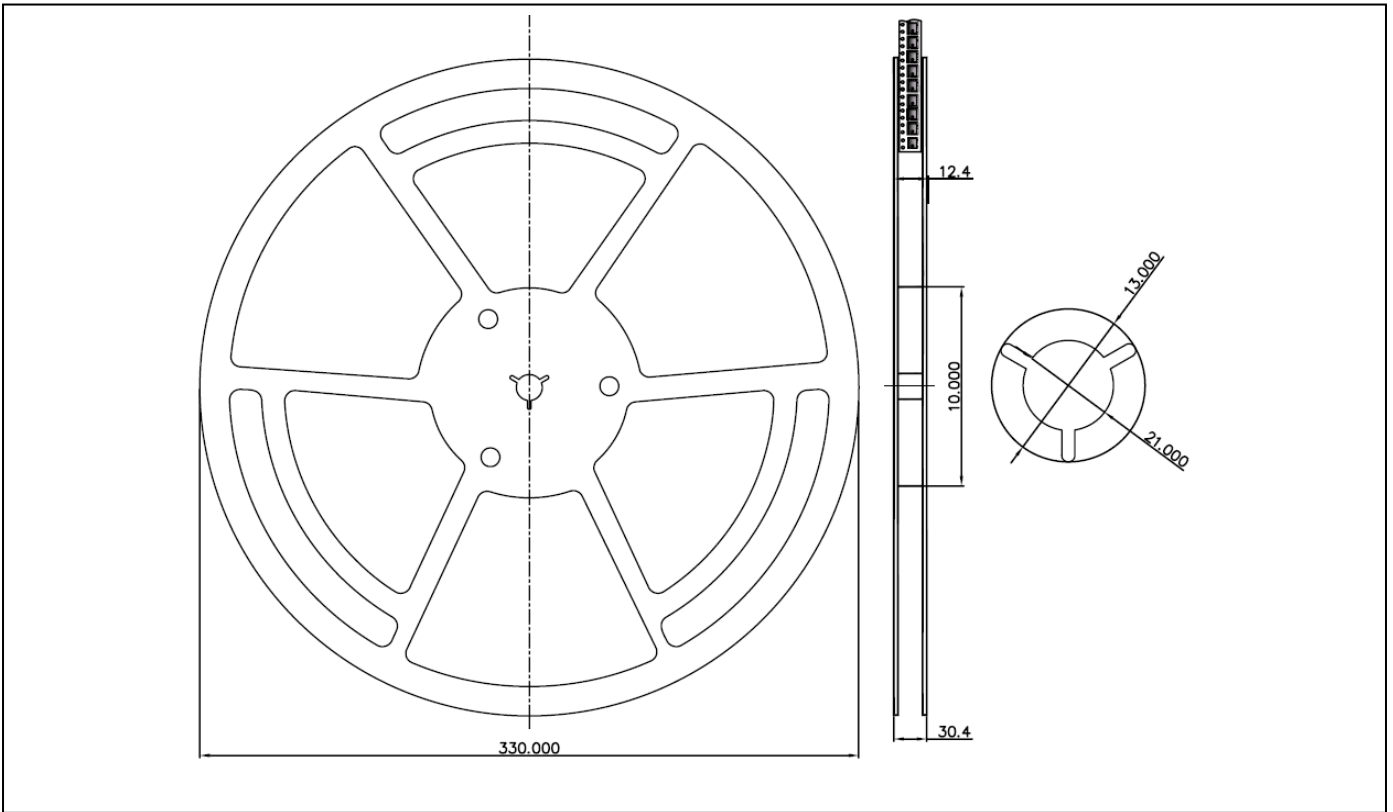
**Recommended Soldering Footprint & Stencil Design**



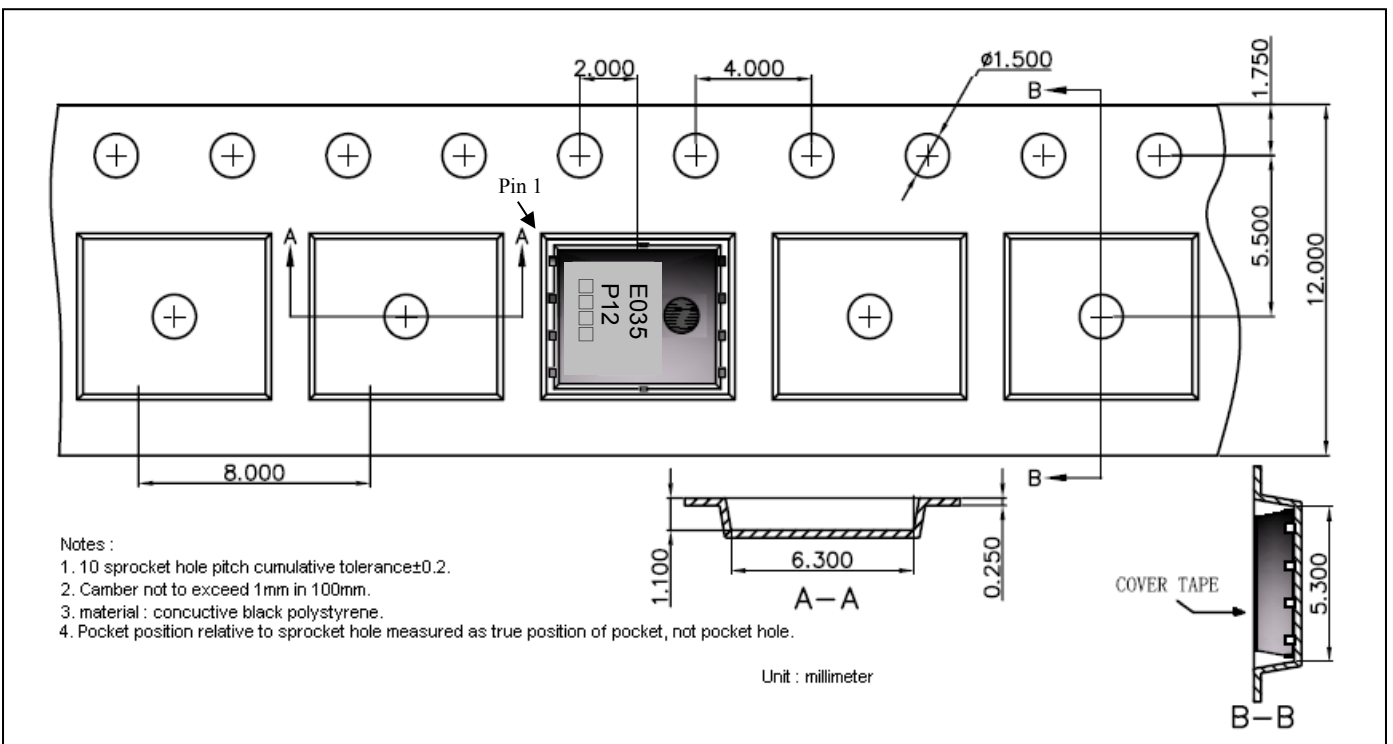
-  solder lands
  -  solder paste
  -  solder resist
  -  occupied area
- 125 μm stencil

unit : mm

**Reel Dimension**



**Carrier Tape Dimension**

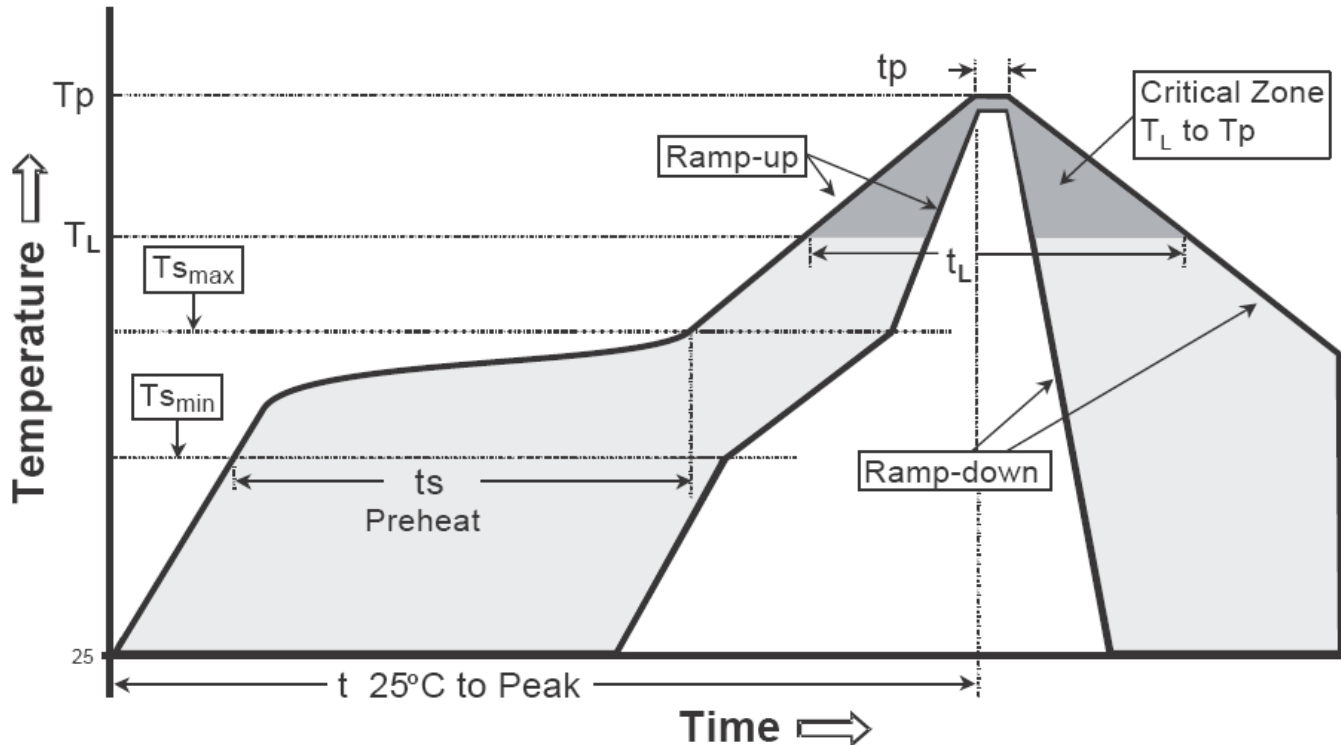




**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

**Recommended temperature profile for IR reflow**

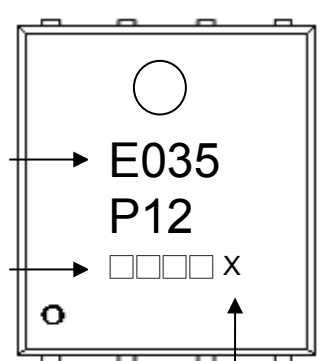


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T <sub>s min</sub> )	100°C	150°C
-Temperature Max(T <sub>s max</sub> )	150°C	200°C
-Time(t <sub>s min</sub> to t <sub>s max</sub> )	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T <sub>L</sub> )	183°C	217°C
- Time (t <sub>L</sub> )	60-150 seconds	60-150 seconds
Peak Temperature(T <sub>P</sub> )	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

**DFN5x6 Dimension**

**Marking :**



Device Name → E035  
 P12

Date Code → [ ][ ][ ][ ] X

Assembly site code :  
 Blank : site 1  
 G : site 2

Date Code(counting from left to right) :  
 1<sup>st</sup> code: year code, the last digit of Christian year  
 2<sup>nd</sup> code : month code, Jan→A, Feb→B, Mar→C, Apr→D  
 May→E, Jun→F, Jul→G, Aug→H, Sep→J,  
 Oct→K, Nov→L, Dec→M  
 3<sup>rd</sup> and 4<sup>th</sup> codes : production serial number, 01~99

**8-Lead DFN5x6 Plastic Package**  
 CYS Package Code : H8

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.900	1.100	0.035	0.043	k	1.100	-	0.043	-
A3	0.200	0.300	0.008	0.012	b	0.330	0.510	0.013	0.020
D	4.944	5.096	0.195	0.201	e	1.270	TYP.	0.050	TYP.
E	5.900	6.126	0.232	0.241	L	0.510	0.711	0.020	0.028
D1	3.670	4.110	0.144	0.162	L1	0.310	0.576	0.012	0.023
E1	3.375	3.780	0.133	0.149	H	0.410	0.726	0.016	0.029
D2	4.800	5.000	0.189	0.197	θ	8°	12°	8°	12°
E2	5.674	5.826	0.223	0.229					

**Notes:** 1.Controlling dimension: millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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