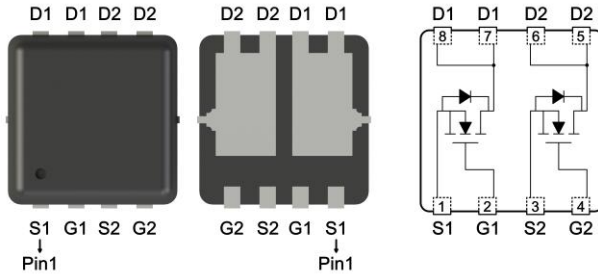


Product Summary

BV_{DSS}	100	V
$R_{DS(ON)}$ typ. @ $V_{GS}=10V, I_D=2A$	34	m Ω
I_D @ $V_{GS}=10V, T_C=25^\circ C$	13	A
I_D @ $V_{GS}=10V, T_A=25^\circ C$	5.2	

DFN3x3



Ordering Information

Device	Package	Shipping
MTE032A10RV8-0-T6-G	DFN3x3	3000pcs / Tape & Reel

0: Product rank, zero for no rank products.

T6: Packing spec, T6: 3000pcs / tape & reel, 13" reel.

G: Environment friendly grade: S for RoHS compliant products, G for RoHS compliant and green compound products.

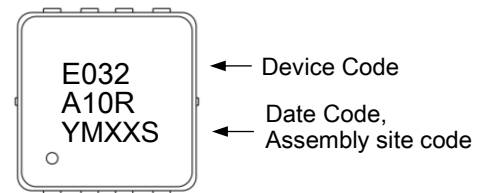
Absolute Maximum Ratings ($T_A=25^\circ C$)

Parameter	Symbol	Value	Unit	
Drain-Source Voltage	V_{DS}	100	V	
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current @ $V_{GS}=10V, T_C=25^\circ C$ (silicon limit)	I_D	14	A	
Continuous Drain Current @ $V_{GS}=10V, T_C=25^\circ C$ (package limit)		13		
Continuous Drain Current @ $V_{GS}=10V, T_C=100^\circ C$		8.8		
Continuous Drain Current @ $V_{GS}=10V, T_A=25^\circ C$		5.2		
Continuous Drain Current @ $V_{GS}=10V, T_A=70^\circ C$		4.2		
Pulsed Drain Current	I_{DM}	50		
Continuous Body Diode Forward Current @ $T_C=25^\circ C$	I_S	12		
Pulsed Body Diode Forward Current @ $T_C=25^\circ C$	I_{SM}	48		
Avalanche Current @ $L=0.1mH$	I_{AS}	4		
Avalanche Energy @ $L=0.5mH$	E_{AS}	6.3	mJ	
Total Power Dissipation	P_D	$T_C=25^\circ C$	15	W
		$T_C=100^\circ C$	6	
		$T_A=25^\circ C$	2	
		$T_A=70^\circ C$	1.3	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55~+150	$^\circ C$	
Steady State Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	8.3	$^\circ C/W$	
Steady State Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	63		

Features

- Low On Resistance
- Low Gate Charge
- Fast Switching Characteristic
- Pb-free lead plating and halogen-free

Marking



YMXX: Date Code Marking

Y: Year Code, the last digit of Christian year

M: Month Code

A: Jan	B: Feb	C: Mar	D: Apr	E: May	F: Jun
G: Jul	H: Aug	J: Sep	K: Oct	L: Nov	M: Dec

XX: Production Serial Number, 01~99

S: Assembly site code, Site 1: G, Site 2: A



Electrical Characteristics (T_A=25°C, unless otherwise specified)

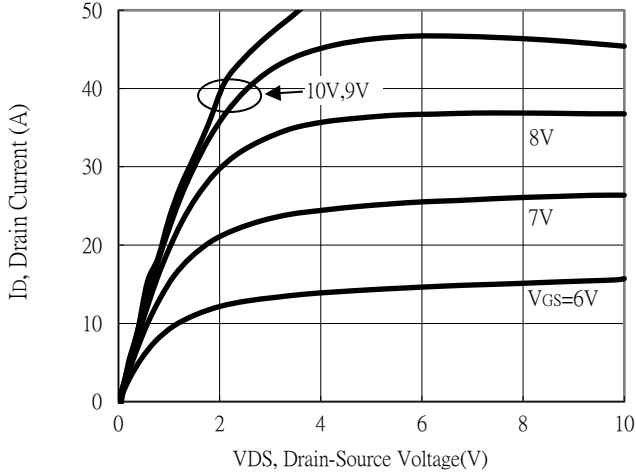
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	100	-	-	V	V _{GS} =0V, I _D =250μA
V _{GS(th)}	2	-	4		V _{DS} =V _{GS} , I _D =250μA
G _{FS}	-	3	-	S	V _{DS} =10V, I _D =2A
I _{GSS}	-	-	±100	nA	V _{GS} =±20V, V _{DS} =0V
I _{DSS}	-	-	1	μA	V _{DS} =80V, V _{GS} =0V
R _{DS(ON)}	-	34	44	mΩ	V _{GS} =10V, I _D =2A
Dynamic					
C _{iss}	-	495	-	pF	V _{DS} =50V, V _{GS} =0V, f=1MHz
C _{oss}	-	74	-		
C _{rss}	-	22	-		
R _g	-	0.9	-	Ω	f=1MHz
Q _g *d,e	-	8.5	-	nC	V _{DS} =50V, I _D =2A, V _{GS} =10V
Q _{gs} *d,e	-	2.7	-		
Q _{gd} *d,e	-	2	-		
t _{d(ON)} *d,e	-	9.4	-	ns	V _{DS} =50V, I _D =2A, V _{GS} =10V, R _{GS} =1Ω
tr *d,e	-	16	-		
t _{d(OFF)} *d,e	-	16	-		
t _f *d,e	-	8.9	-		
Source-Drain Diode					
V _{SD} *d	-	0.79	1.2	V	I _S =2A, V _{GS} =0V
t _{rr}	-	21	-	ns	I _F =2A, di/dt=100A/μs
Q _{rr}	-	17	-	nC	

Note:

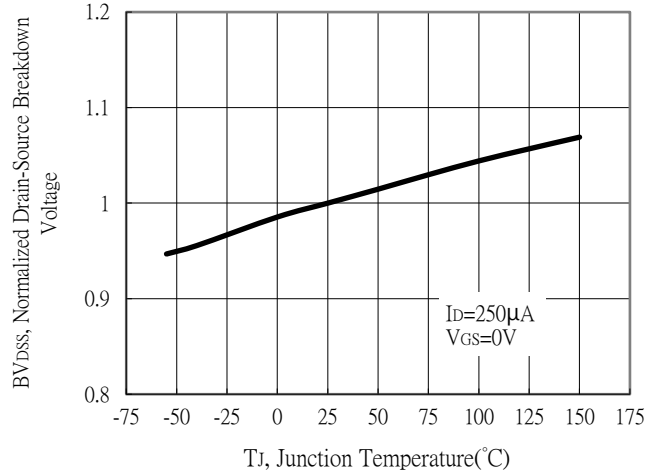
- *a. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper Dissipation.
- *b. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz copper, in a still air environment with T_A=25°C. The power dissipation P_D is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
- *c. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and low duty cycles to keep initial T_J=25°C.
- *d. Pulse Test : Pulse Width≤300μs, Duty Cycle≤2%.
- *e. Independent of operating temperature.

Typical Characteristics

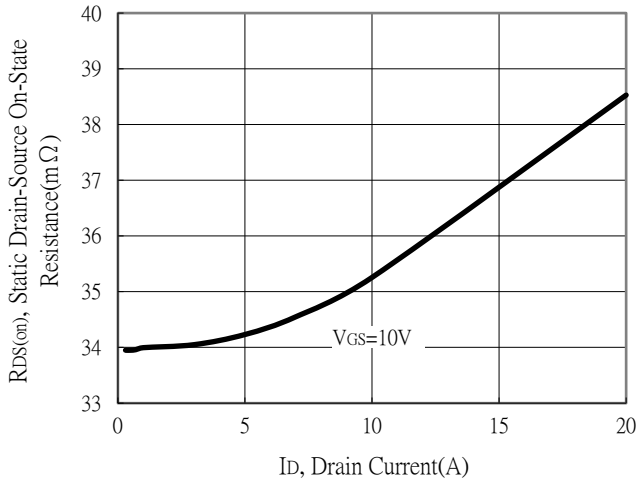
Typical Output Characteristics



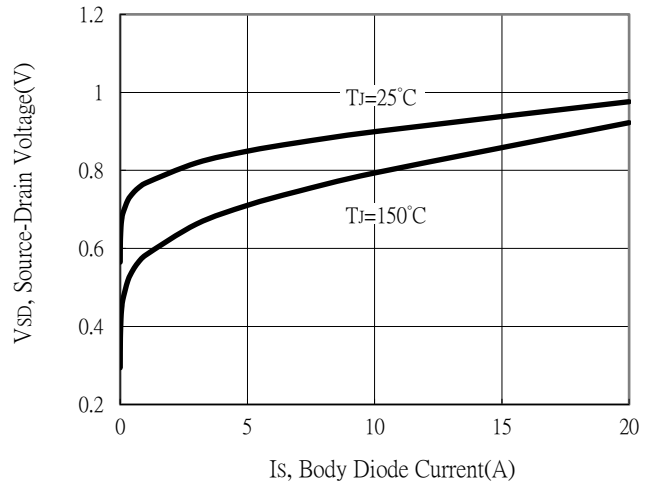
Breakdown Voltage vs Junction Temperature



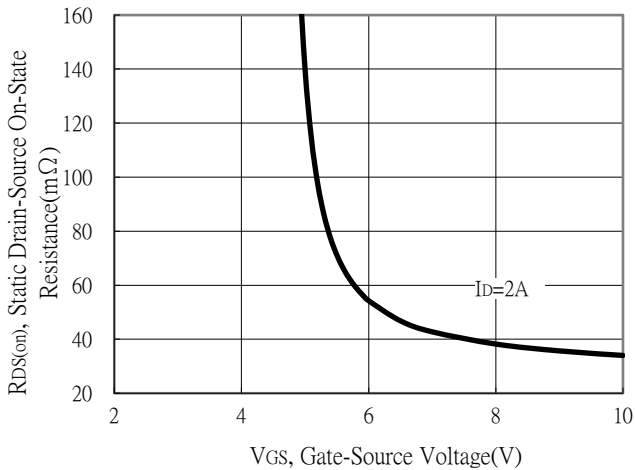
Static Drain-Source On-State resistance vs Drain Current



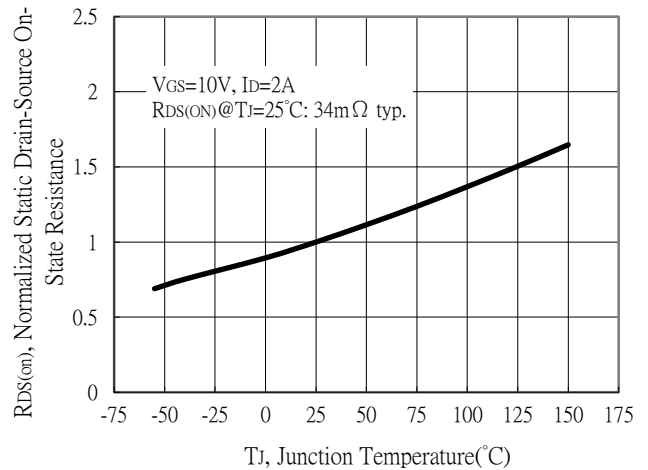
Body Diode Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

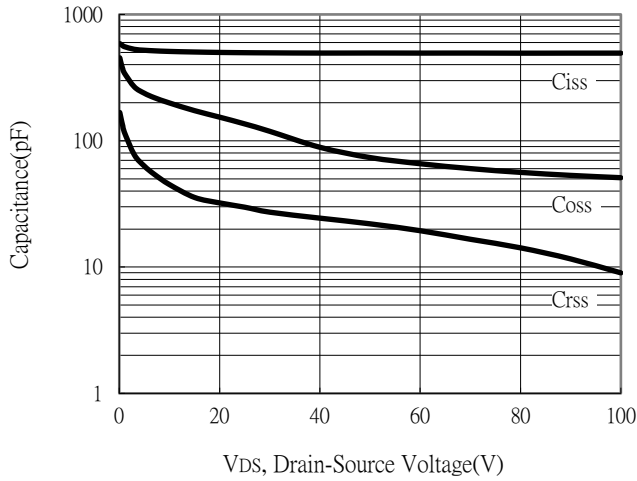


Drain-Source On-State Resistance vs Junction Temperature

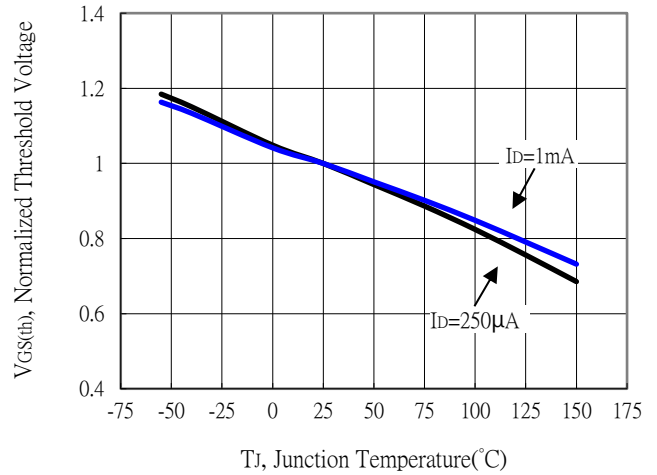


Typical Characteristics

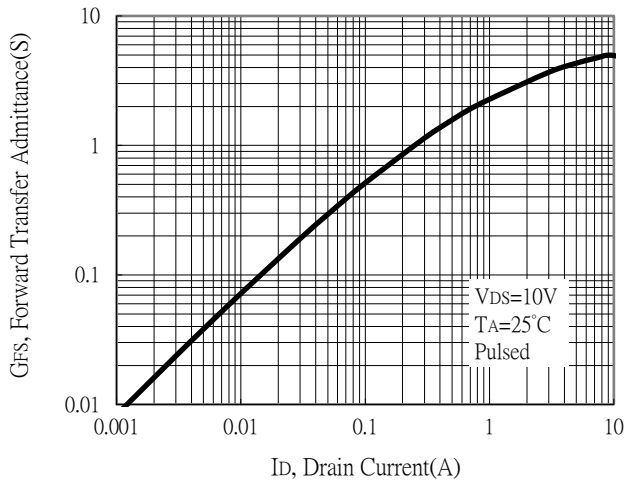
Capacitance vs Drain-to-Source Voltage



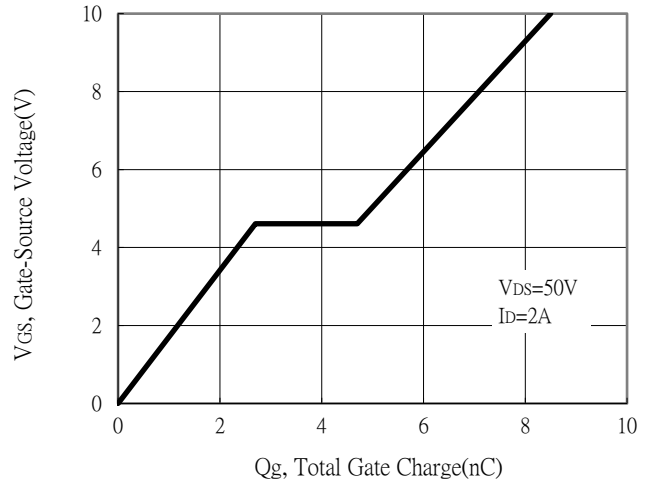
Threshold Voltage vs Junction Temperature



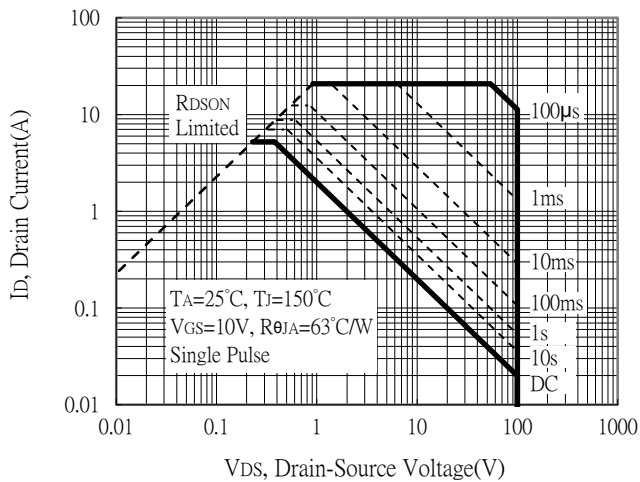
Forward Transfer Admittance vs Drain Current



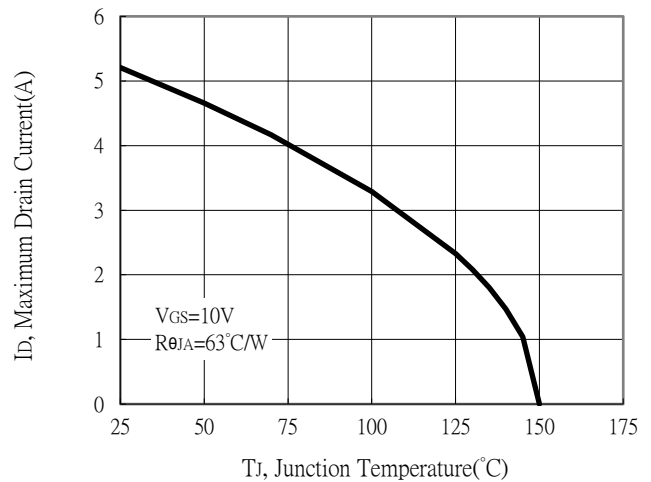
Gate Charge Characteristics



Maximum Safe Operating Area

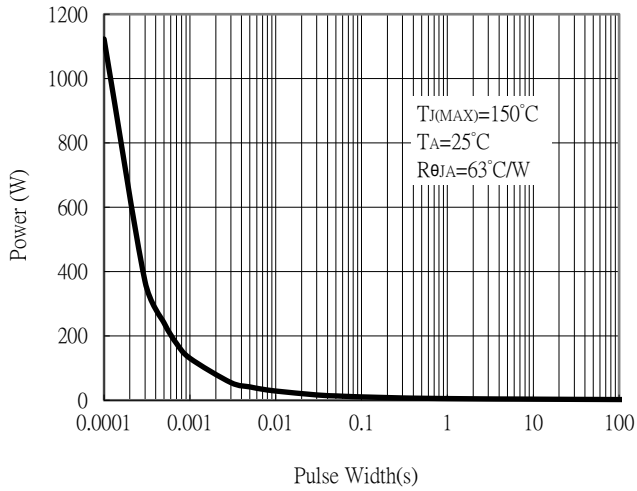


Maximum Drain Current vs Junction Temperature

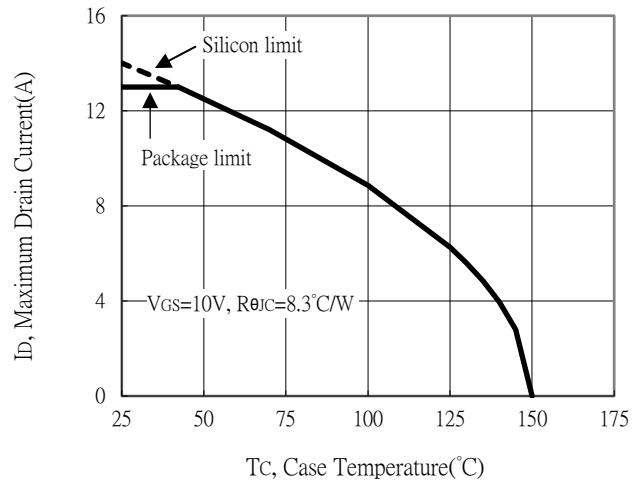


Typical Characteristics

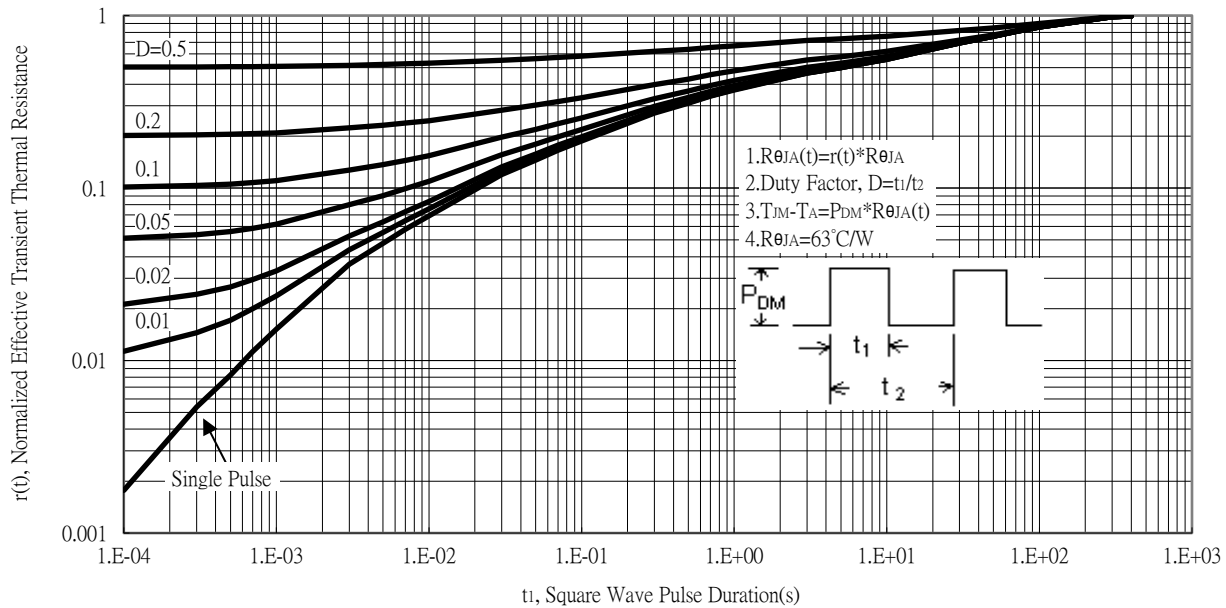
Single Pulse Power Rating, Junction to Ambient



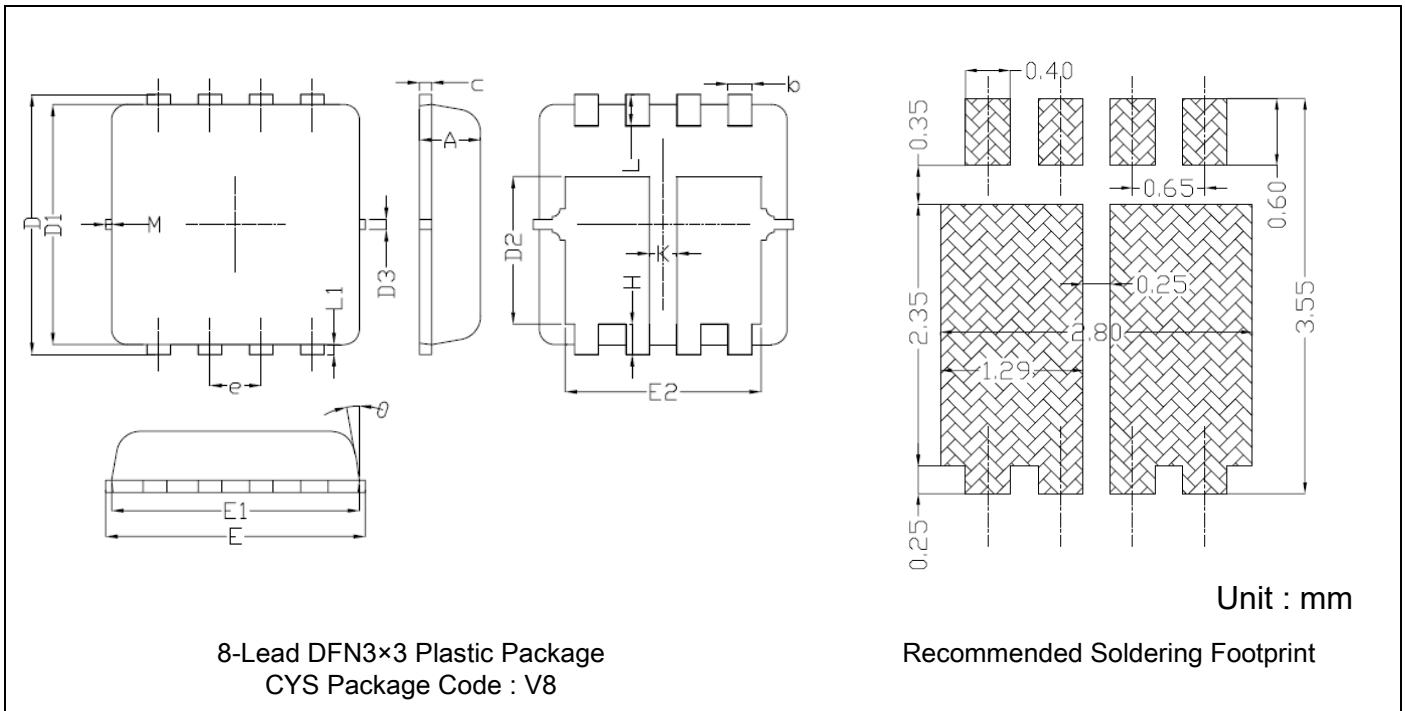
Maximum Drain Current vs Case Temperature



Transient Thermal Response Curves



DFN3×3 Dimension



DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Min.		Min.	Max.	Min.	Max.
A	0.70	0.80	0.028	0.031	E2	2.39	2.59	0.094	0.102
b	0.25	0.35	0.010	0.014	e	0.65	BSC	0.026	BSC
c	0.10	0.25	0.004	0.010	H	0.30	0.50	0.012	0.020
D	3.25	3.45	0.128	0.136	L	0.30	0.50	0.012	0.020
D1	3.00	3.20	0.118	0.126	L1	0.13	TYP	0.005	TYP
D2	1.78	1.98	0.070	0.077	K	0.30	-	0.012	-
D3	0.13	TYP	0.005	TYP	θ	-	12°	-	12°
E	3.00	3.40	0.118	0.134	M	-	0.15	-	0.006
E1	3.00	3.20	0.118	0.126					

Note:

- Controlling dimension: millimeters.
- Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
- If there is any question with packing specification or packing method, please contact your local CYStek sales office.

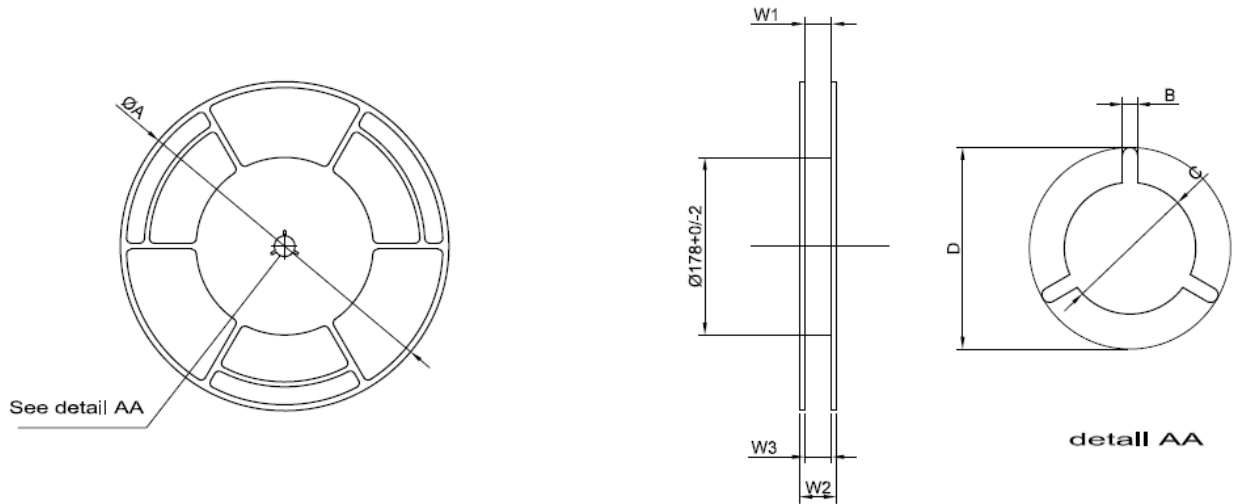
Material:

- Lead: pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.

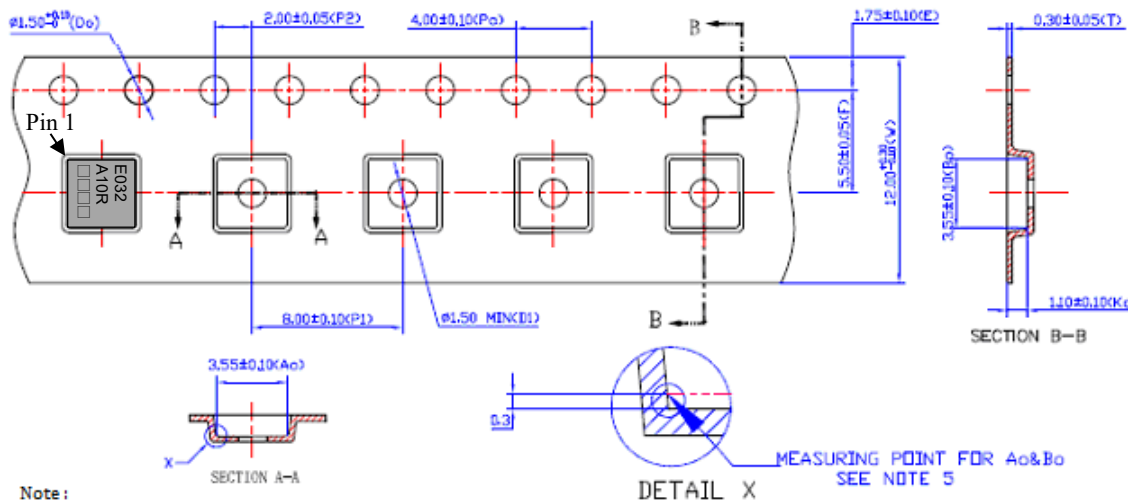
Reel Dimension



TAPE SIZE	A	B	C	D	W1	W2	W3
12mm	330±2.0	2.9±0.5	13.0+0.5/-0	23±1.0	12.4 +2/-0	18.4±0.5	12~15

Unit : mm

Carrier Tape Dimension



Note :

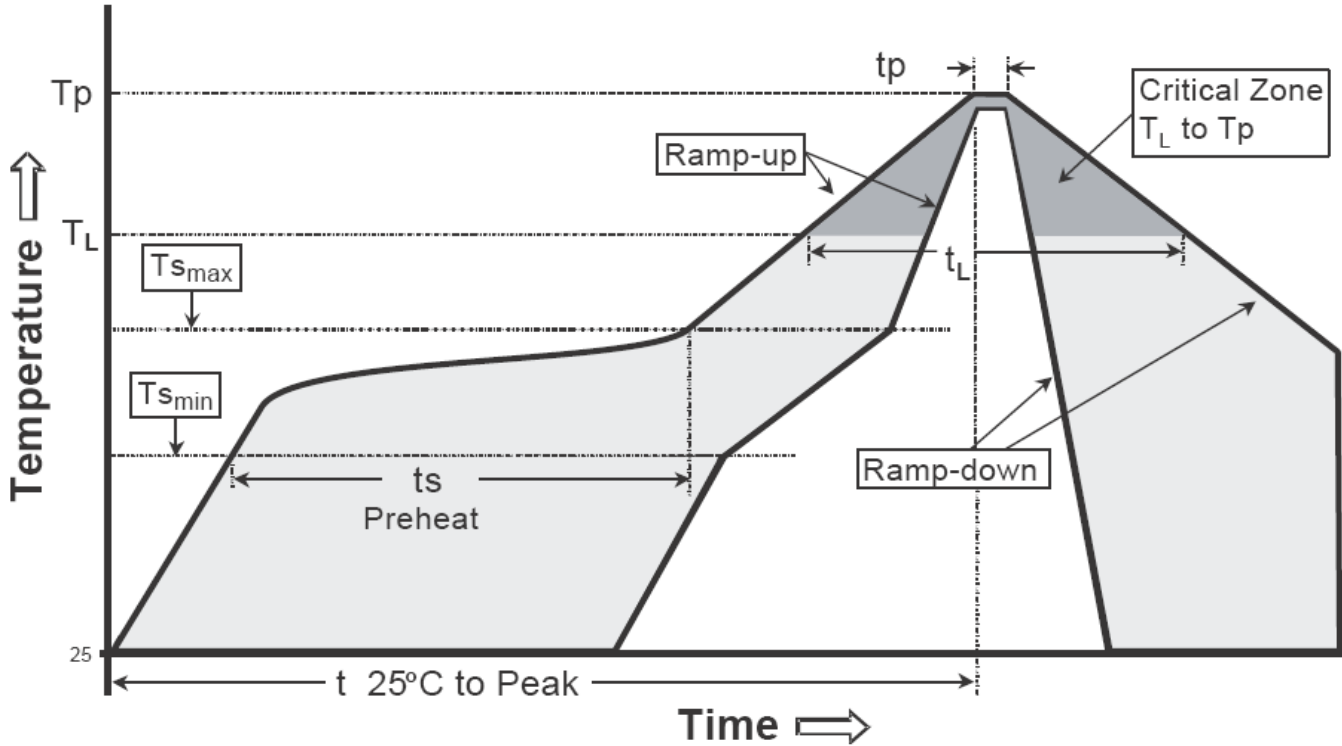
- 1.10 sprocket hole pitch cumulative tolerance : ±0.2mm.
- 2.Camber : Reference to carrier tape inspection manual.
- 3.Material : black conductive polystyrene.
- 4.All dimensions are in millimeters(unless otherwise specified).
- 5.Ao and Bo measured on a plane 0.3mm above the bottom of the pocket.
- 6.Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
- 7.Pocket position relative to sprocket hole measured as true position of the pocket, not pocket hole.
- 8.Surface resistivity : $1 \times 10^4 \sim 1 \times 10^{11}$ ohms/sq

Unit : mm

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (TS max to TP)	3°C/second max.	3°C/second max.
Preheat -Temperature Min (TS min) -Temperature Max (TS max) -Time (ts min to ts max)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: -Temperature (TL) -Time (tL)	183°C 60-150 seconds	217°C 60-150 seconds
Peak Temperature (TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature (tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note:

- All temperatures refer to topside of the package, measured on
- For devices mounted on FR-4 PCB of 1.6mm or equivalent grade PCB. If other grade PCB is used, care should be taken to match the coefficients of thermal expansion between components and PCB. If they are not matched well, the solder joints may crack or the bodies of the parts may crack or shatter as the assembly cools.