

Dual N-Channel Enhancement Mode Power MOSFET

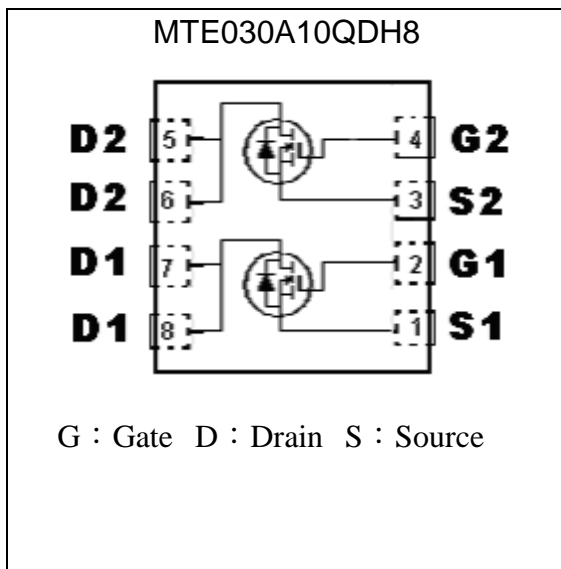
MTE030A10QDH8

Features

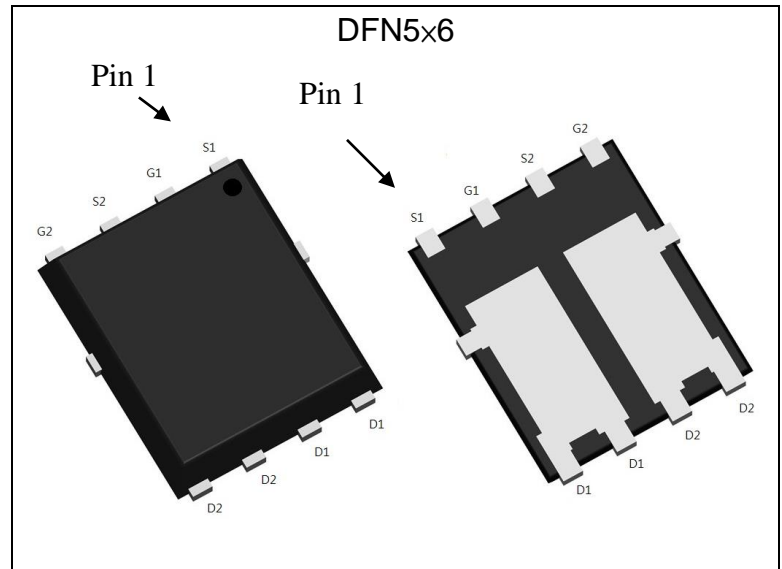
- Low On Resistance
- Simple Drive Requirement
- Low Gate Charge
- Fast Switching Characteristic
- Pb-free lead plating and Halogen-free package

BV_{DSS}	100V
I_D@V_{GS}=10V, T_C=25°C	28A
I_D@V_{GS}=10V, T_C=100°C	18A
I_D@V_{GS}=10V, T_A=25°C	5.0A
I_D@V_{GS}=10V, T_A=70°C	4.0A
R_{DS(ON)}@V_{GS}=10V, I_D=5A	27mΩ (typ)
R_{DS(ON)}@V_{GS}=7V, I_D=4A	31mΩ (typ)

Equivalent Circuit

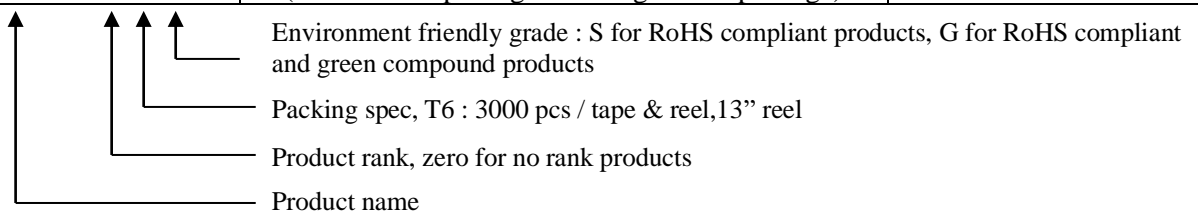


Outline



Ordering Information

Device	Package	Shipping
MTE030A10QDH8-0-T6-G	DFN 5 ×6 (Pb-free lead plating and halogen-free package)	3000 pcs / tape & reel





Absolute Maximum Ratings (T_C=25°C, unless otherwise noted)

Parameter		Symbol	Limits	Unit
Drain-Source Voltage		V _{DS}	100	V
Gate-Source Voltage		V _{GS}	±20	
Continuous Drain Current @T _C =25°C, V _{GS} =10V (Note 1)		I _D	28	A
Continuous Drain Current @T _C =100°C, V _{GS} =10V (Note 1)			18	
Continuous Drain Current @T _A =25°C, V _{GS} =10V (Note 2)		I _{DSM}	5.0	
Continuous Drain Current @T _A =70°C, V _{GS} =10V (Note 2)			4.0	
Pulsed Drain Current @ V _{GS} =10V (Note 3)		I _{DM}	56	
Avalanche Current @L=0.1mH(Typical) (Note 3)		I _{AS}	18	
Avalanche Energy @L=0.5mH		E _{AS}	25	mJ
Power Dissipation	T _C =25°C (Note 1)	P _D	56	W
	T _C =100°C (Note 1)		22	
	T _A =25°C (Note 2)	P _D SM	1.7	
	T _A =70°C (Note 2)		1.1	
Operating Junction and Storage Temperature		T _J , T _{stg}	-55~+150	°C

*Drain current limited by maximum junction temperature

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	R _{θJC}	2.2	°C/W
Thermal Resistance, Junction-to-ambient, max (Note 4)	R _{θJA}	72	

- Note :
1. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
 2. The value of R_{θJA} is measured with the device mounted on 1 in²FR-4 board with 2 oz. copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The power dissipation P_DSM is based on R_{θJA} and the maximum allowed junction temperature of 150°C.
 3. Ratings are based on low frequency and low duty cycles to keep initial T_J=25°C.
 4. When mounted on 1 in² copper pad of FR-4 board ; 125°C/W when mounted on minimum copper pad.

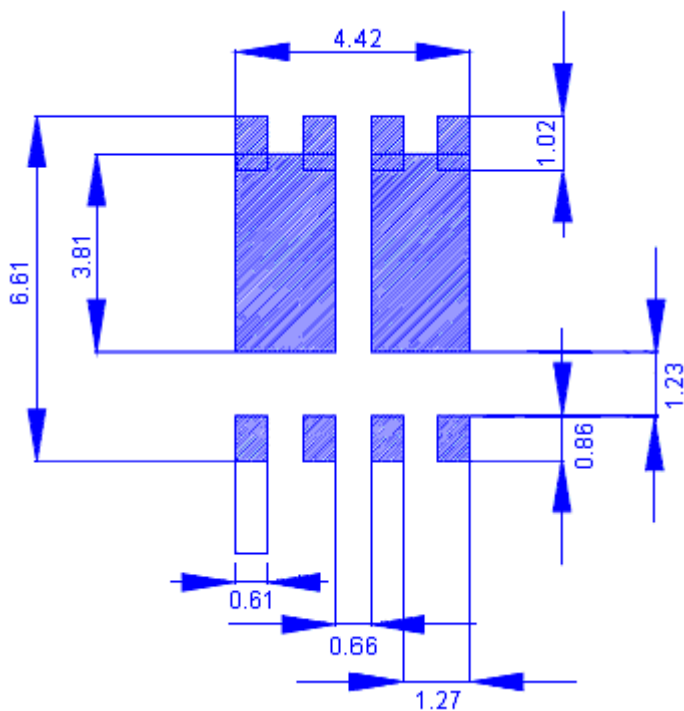
Characteristics (T_J=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	100	-	-	V	V _{GS} =0V, I _D =250μA
ΔBV _{DSS} /ΔT _J	-	0.05	-	V/°C	Reference to 25°C, I _D =250μA
V _{GS(th)}	2	-	4	V	V _{DS} = V _{GS} , I _D =250μA
*G _{FS}	-	6.7	-	S	V _{DS} =10V, I _D =5A
I _{GSS}	-	-	±100	nA	V _{GS} =±20V
I _{DSS}	-	-	1	μA	V _{DS} =80V, V _{GS} =0V
	-	-	25		V _{DS} =80V, V _{GS} =0V, T _J =85°C
*R _{DS(ON)}	-	27	35	mΩ	V _{GS} =10V, I _D =5A
	-	31	42		V _{GS} =7V, I _D =4A

Dynamic					
*Q _g	16.2	23.2	30.2	nC	V _{DS} =50V, I _D =5A, V _{GS} =10V
*Q _{gs}	1.6	3.2	6.4		
*Q _{gd}	5.5	11	15		
*t _{d(ON)}	-	12.6	-	ns	V _{DS} =50V, I _D =5A, V _{GS} =10V, R _G =3Ω
*t _r	-	24.6	-		
*t _{d(OFF)}	-	30.8	-		
*t _f	-	16.2	-		
C _{iss}	536	767	997	pF	V _{GS} =0V, V _{DS} =50V, f=1MHz
C _{oss}	63	91	118		
C _{rss}	67	96	125		
R _g	-	0.7	-	Ω	f=1MHz
Source-Drain Diode					
*I _S	-	-	28	A	
*I _{SM}	-	-	45		
*V _{SD}	-	0.74	1	V	I _S =1A, V _{GS} =0V
*t _{rr}	-	36	-	ns	V _{GS} =0V, I _F =5A, dI _F /dt=100A/μs
*Q _{rr}	-	48.2	-	nC	

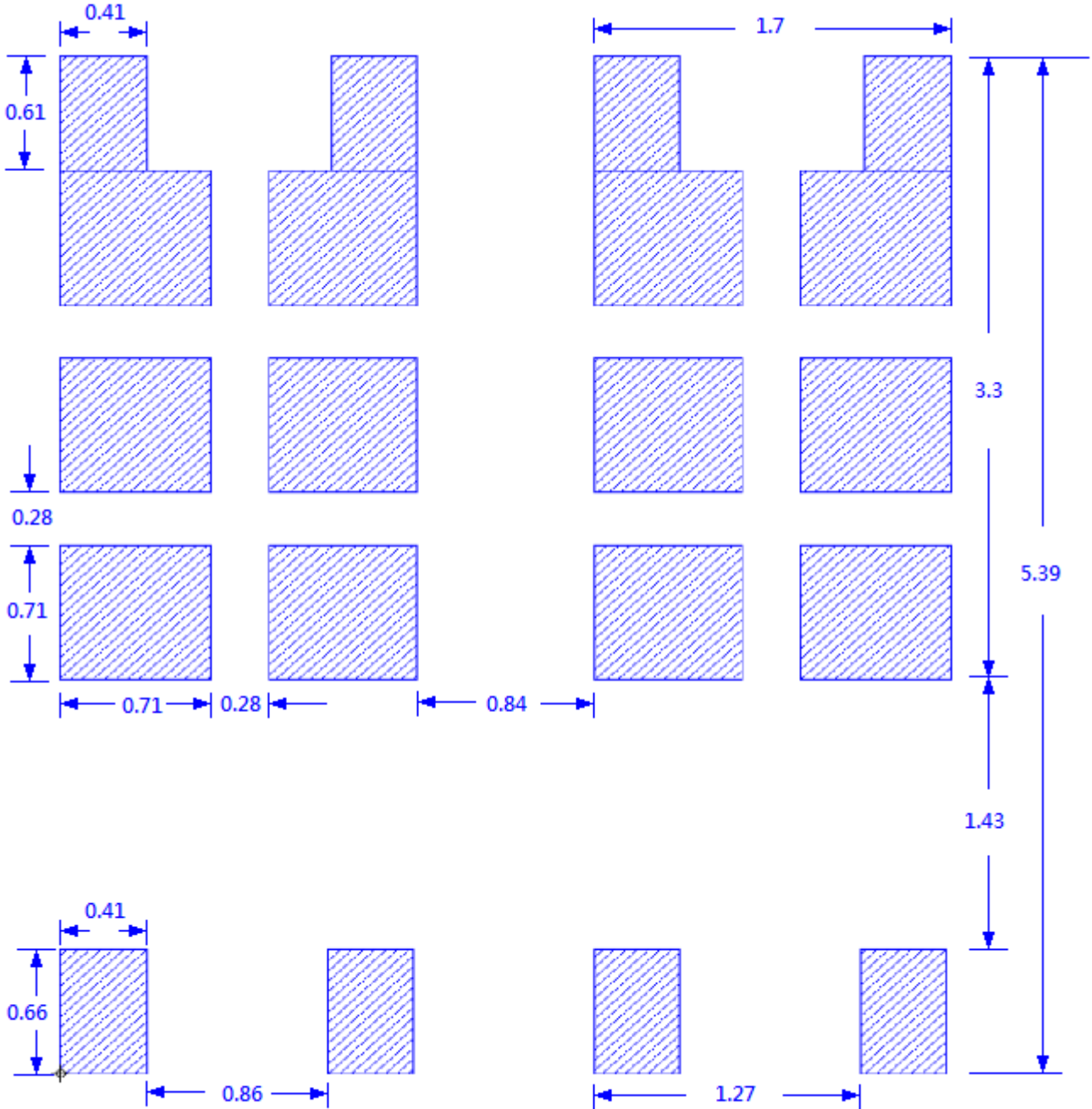
*Pulse Test : Pulse Width ≤300μs, Duty Cycle ≤2%

Recommended Soldering Footprint



unit : mm

Recommended Stencil Design



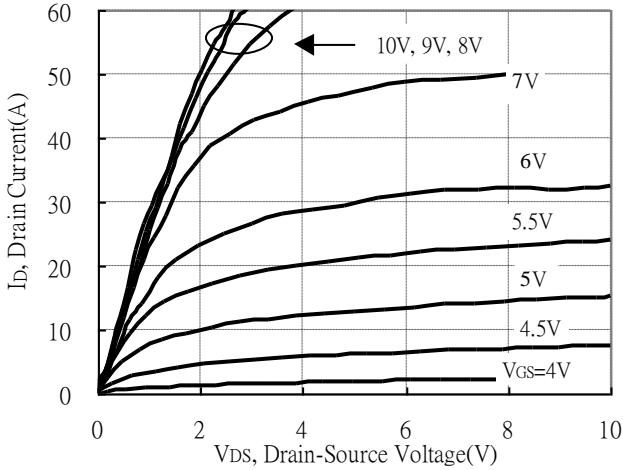
unit : mm

- Note :**
1. Stencil thickness 5 mil (0.127mm)
 2. May need to be adjusted to specific requirements.

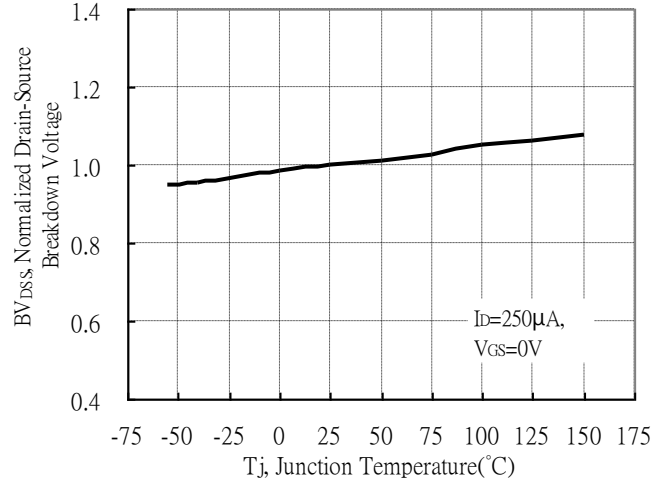


Typical Characteristics

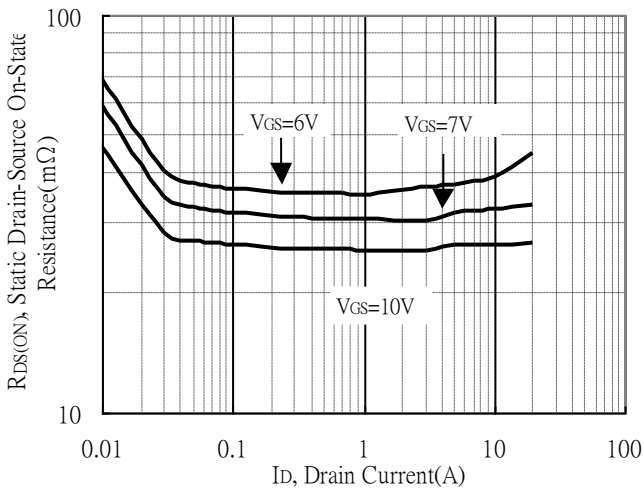
Typical Output Characteristics



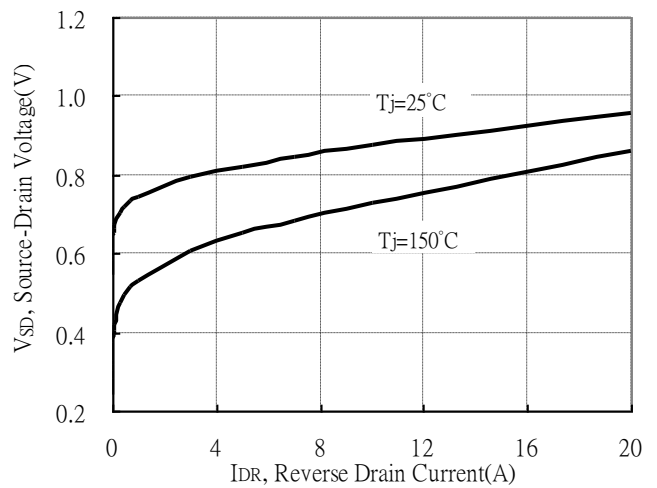
Brekdown Voltage vs Ambient Temperature



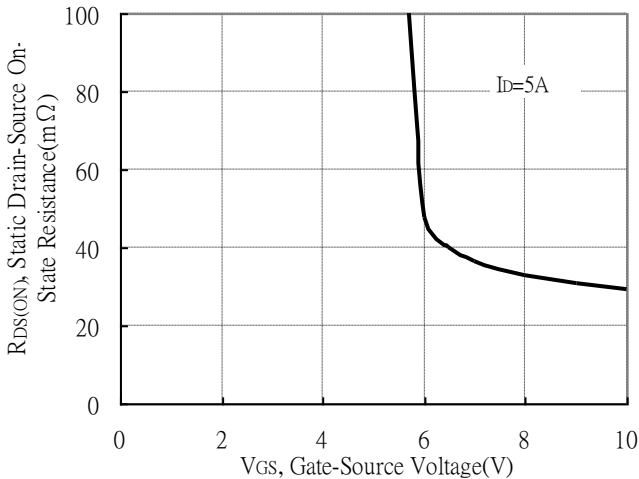
Static Drain-Source On-State resistance vs Drain Current



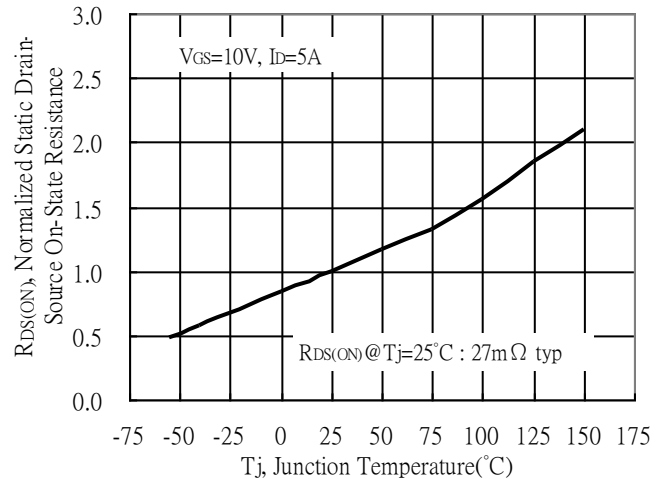
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

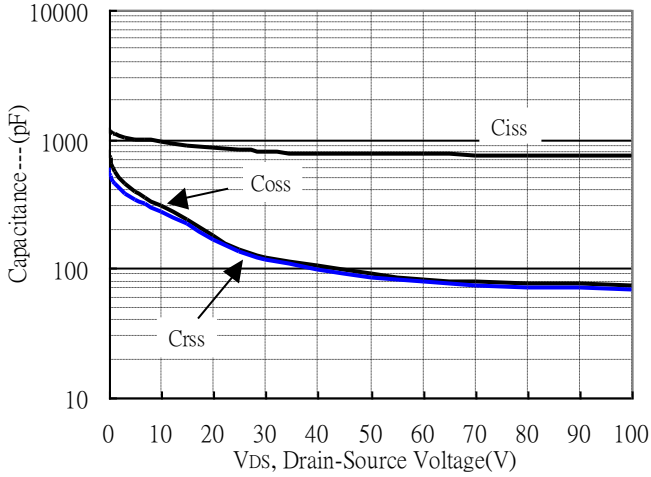


Drain-Source On-State Resistance vs Junction Temperature

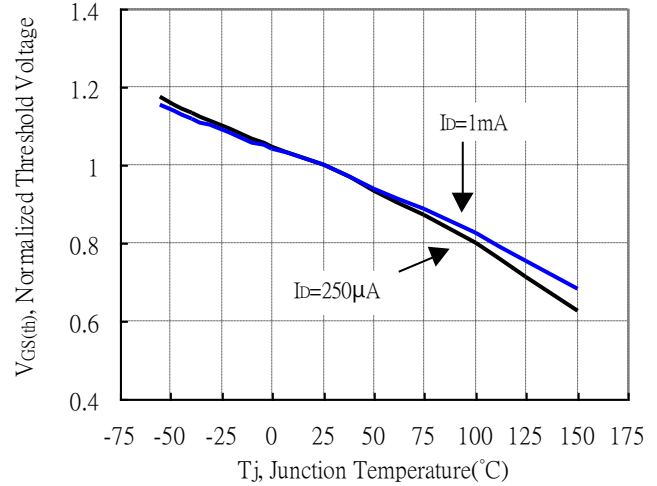


Typical Characteristics(Cont.)

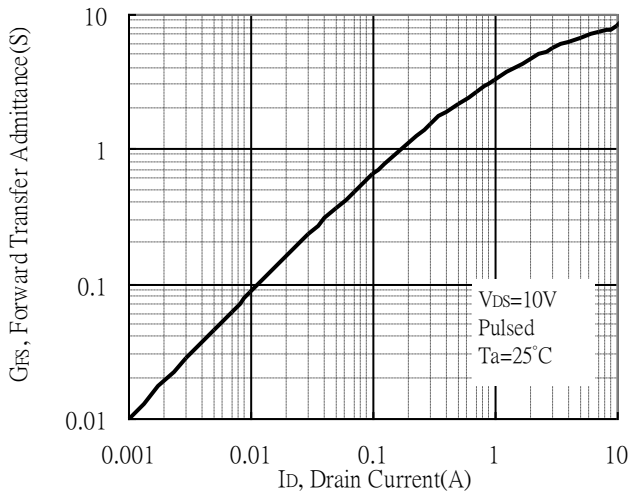
Capacitance vs Drain-to-Source Voltage



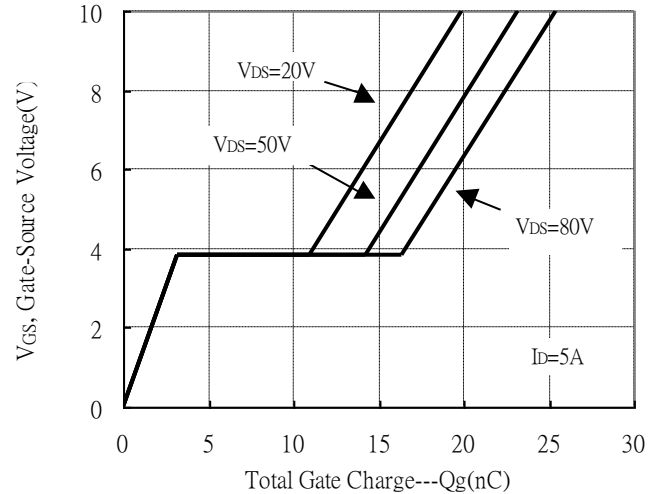
Normalized Threshold Voltage vs Junction Temperature



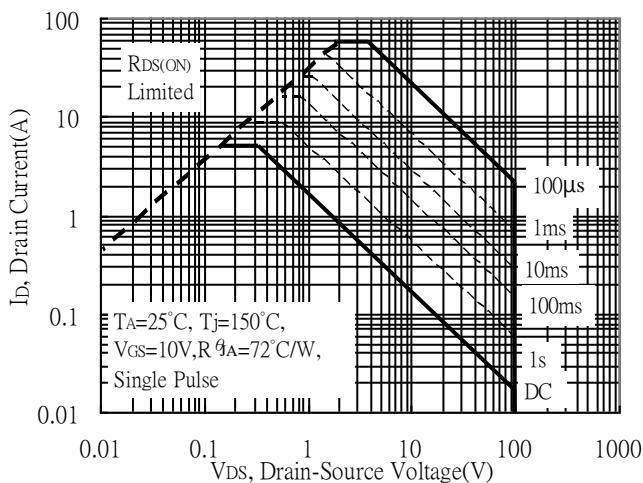
Forward Transfer Admittance vs Drain Current



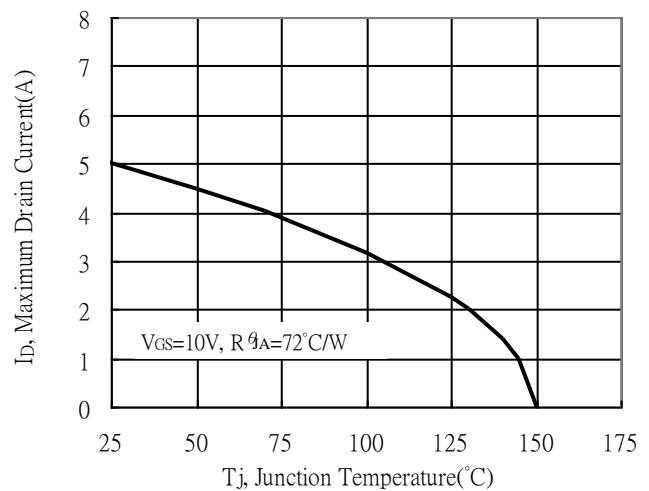
Gate Charge Characteristics



Maximum Safe Operating Area



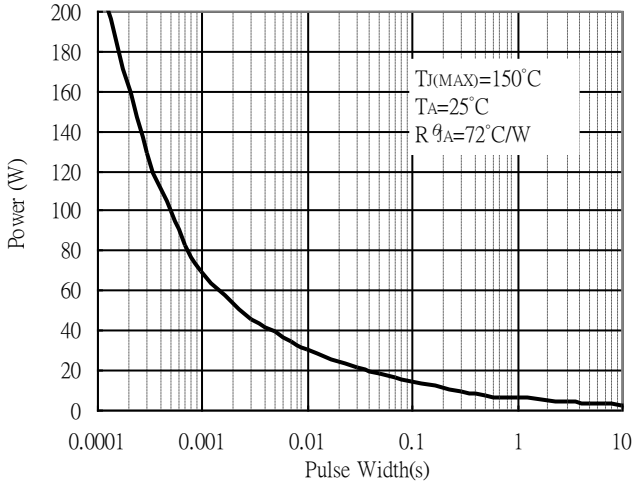
Maximum Drain Current vs Junction Temperature



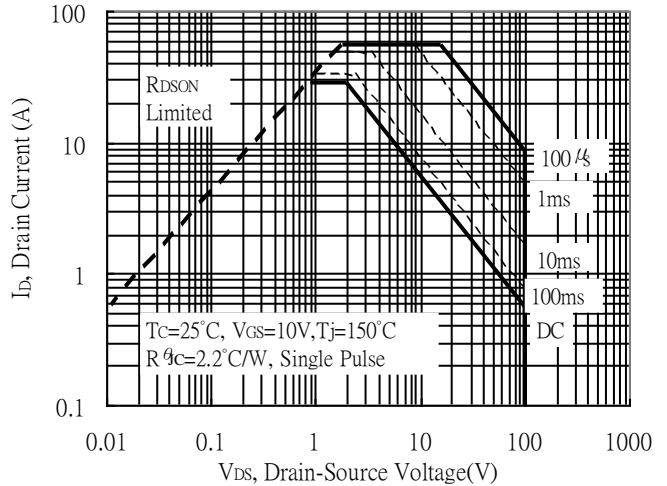


Typical Characteristics(Cont.)

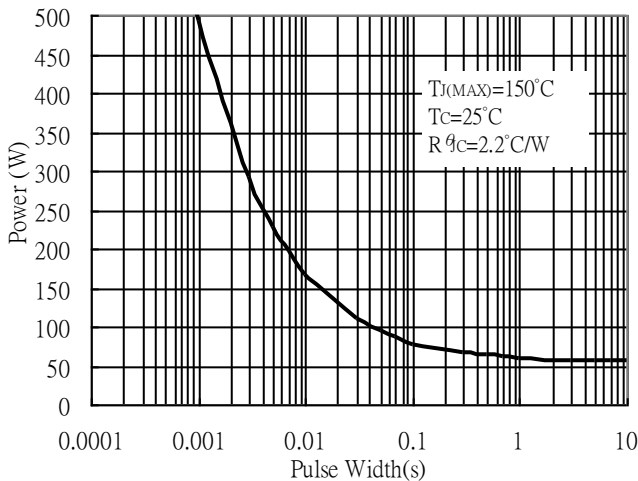
Single Pulse Maximum Power Dissipation



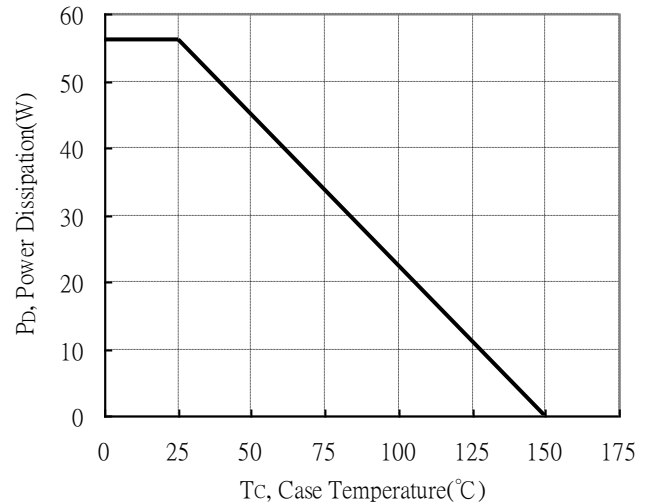
Maximum Safe Operating Area



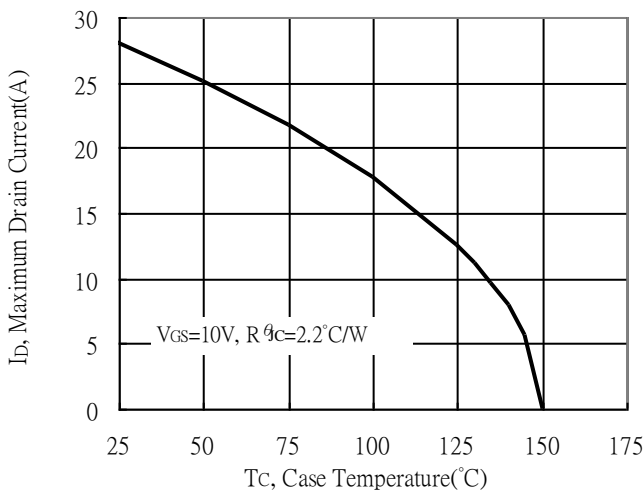
Single Pulse Maximum Power Dissipation



Power Derating Curve

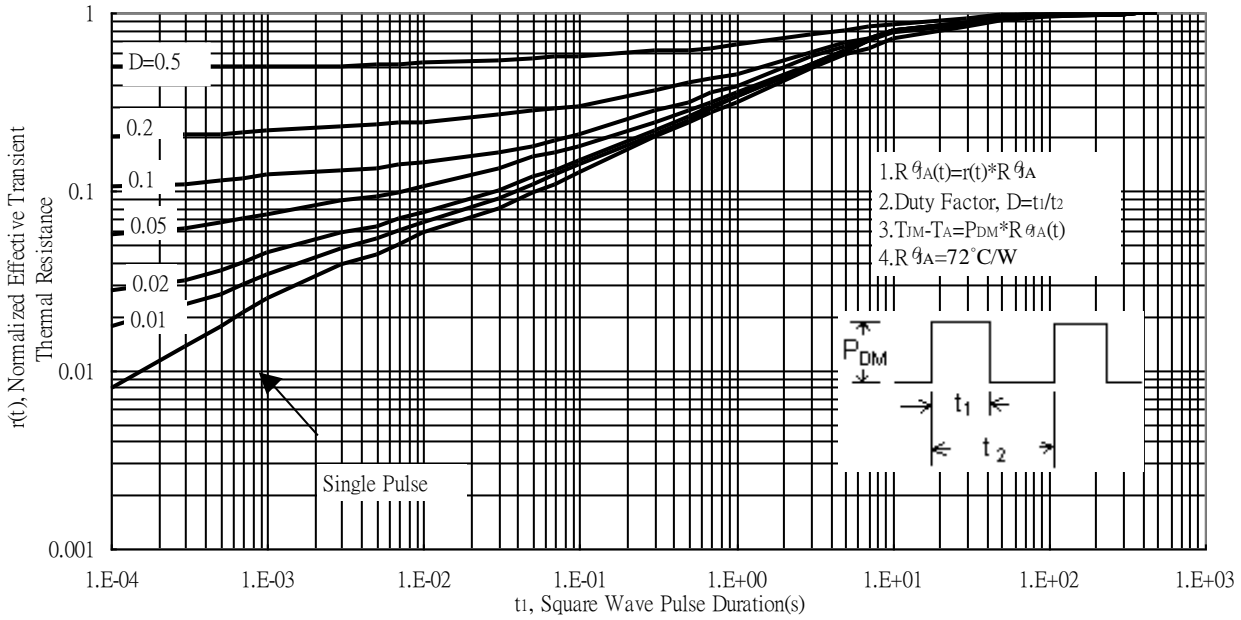


Maximum Drain Current vs Case Temperature

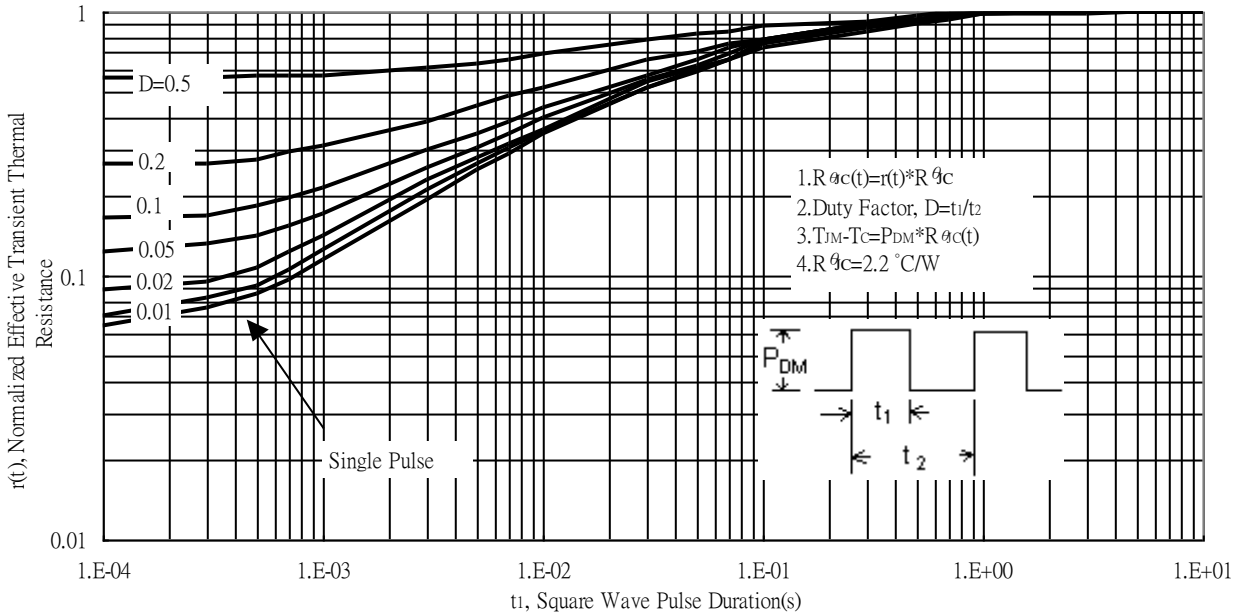


Typical Characteristics(Cont.)

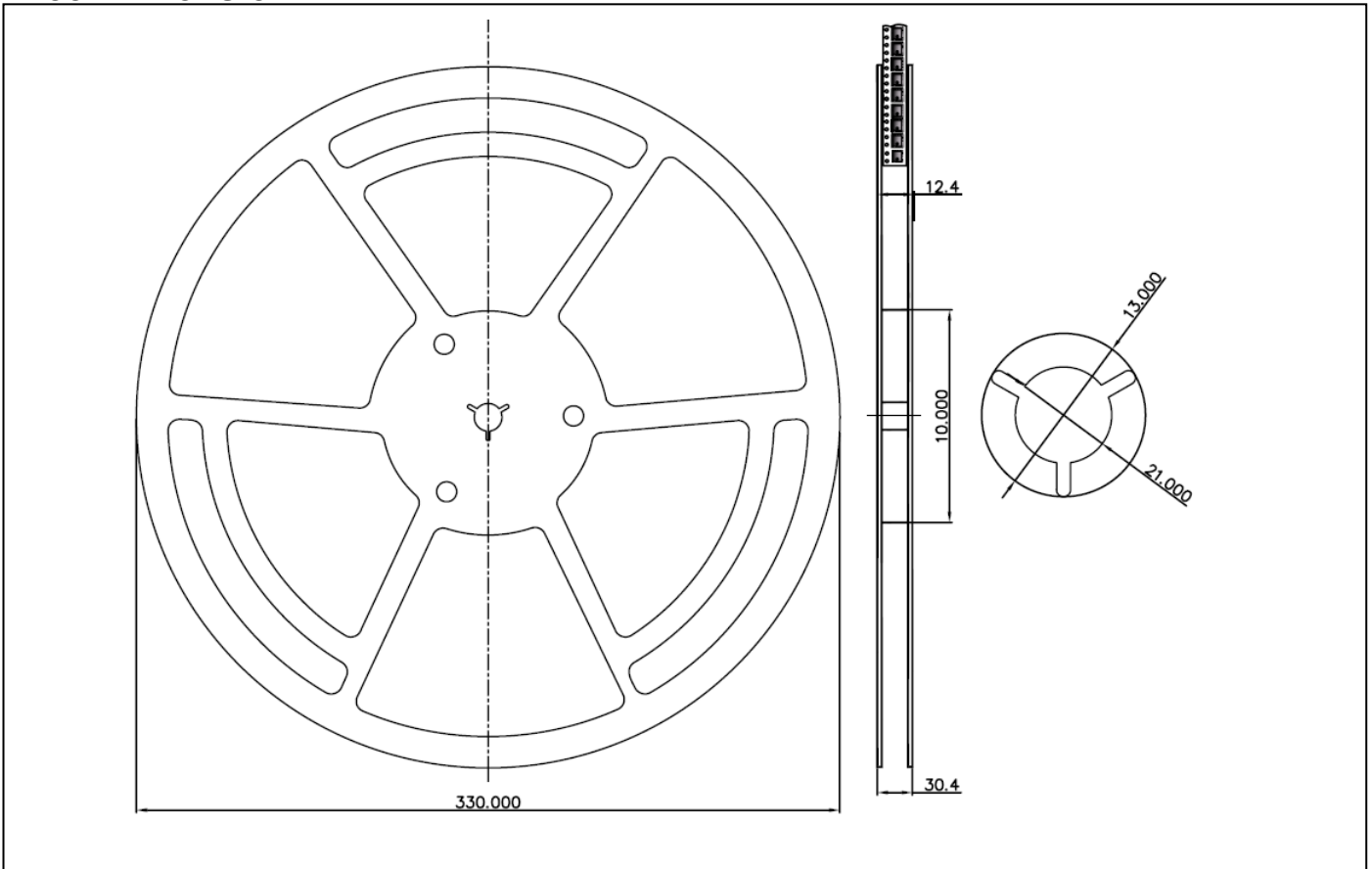
Transient Thermal Response Curves



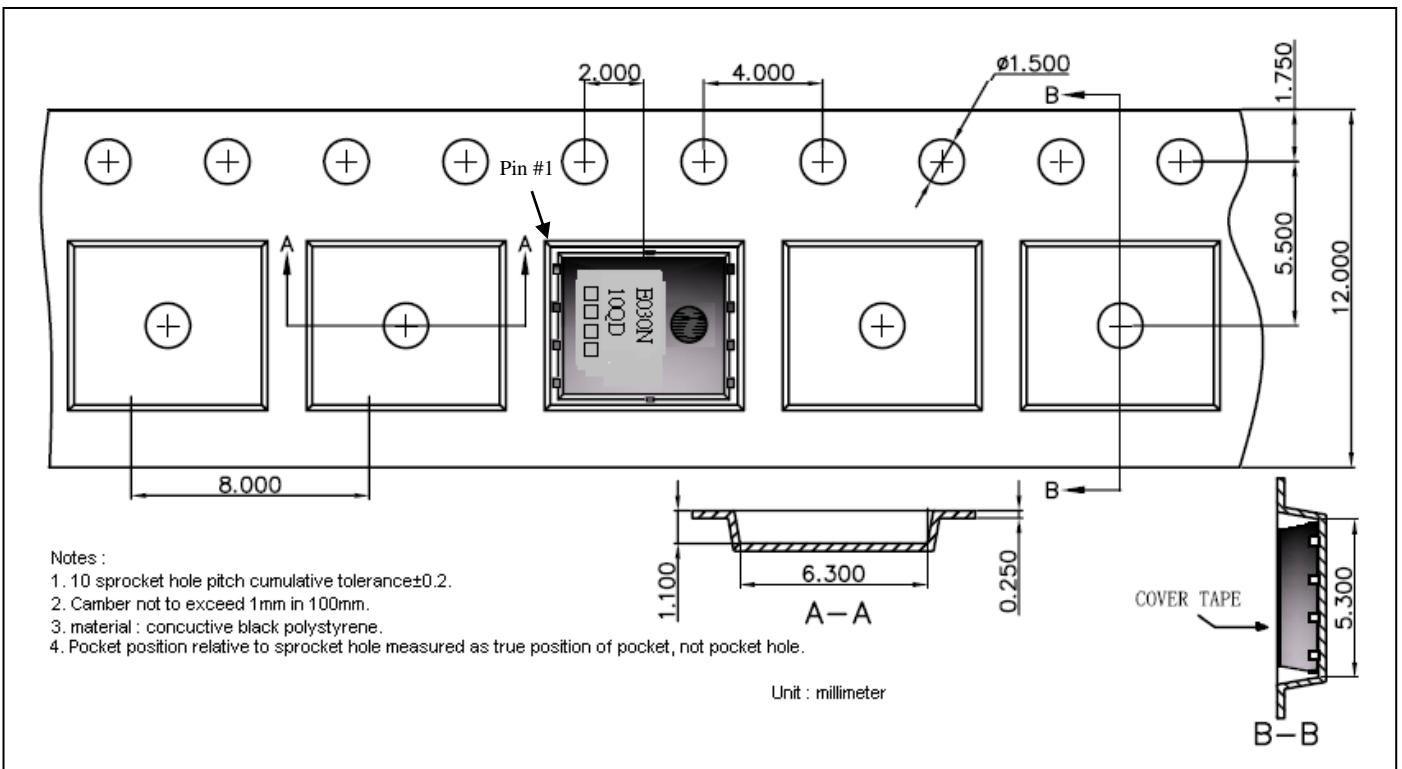
Transient Thermal Response Curves



Reel Dimension



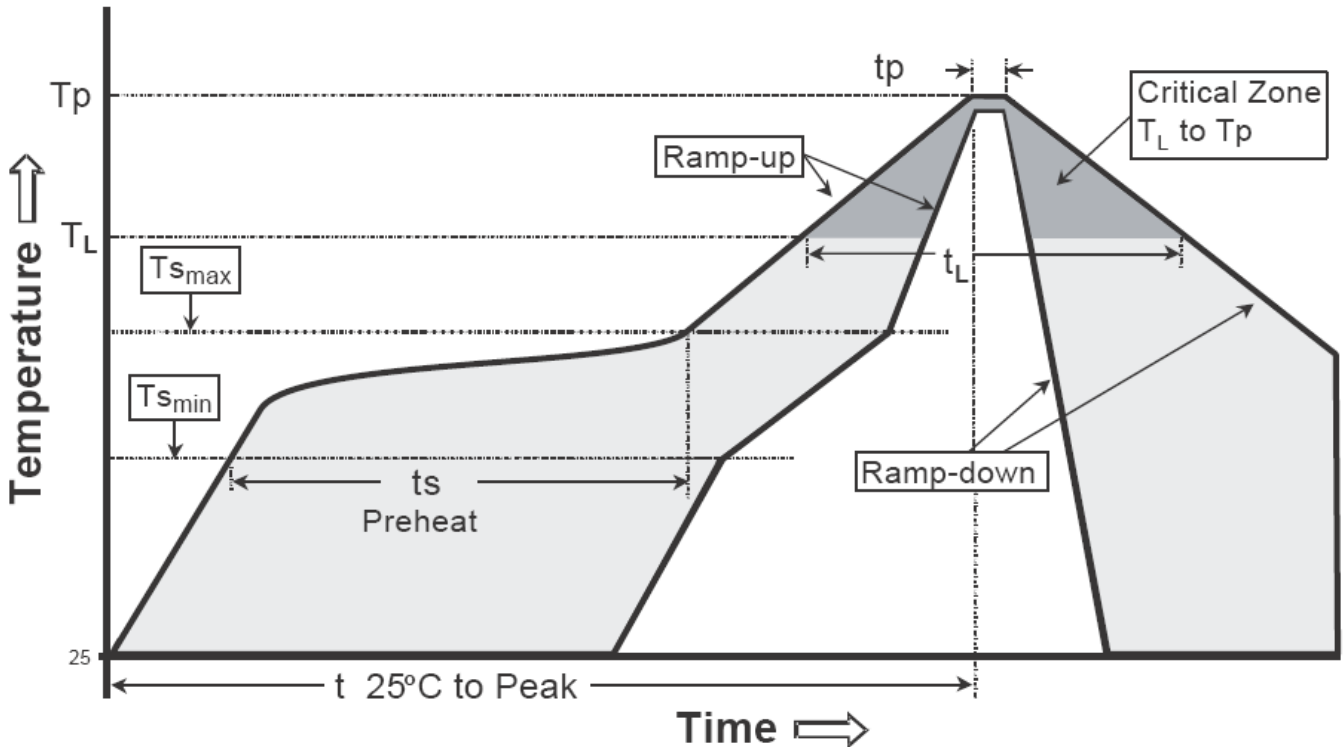
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note :1. All temperatures refer to topside of the package, measured on the package body surface.
 2.For devices mounted on FR-4 PCB of 1.6mm or equivalent grade PCB. If other grade PCB is used, care should be taken to match the coefficients of thermal expansion between components and PCB. If they are not matched well, the solder joints may crack or the bodies of the parts may crack or shatter as the assembly cools.

DFN5x6 Dimension

Marking:

Device Code → **E030N**
10QD

Date Code → □□□□ (G)

Assembly site code :
 Blank : JCET
 G : GEM

Date code : (From left to right)
 First code : Year code, the last digit of Christine year.
 For example, 2017→7, 2018→8, 2019→9, ..., etc.
 Second code : Month code, Jan→A, Feb→B, Mar→C, Apr→D,
 May→E, Jun→F, Jul→G, Aug→H, Sep→J, Oct→K,
 Nov→L, Dec→M
 Third and fourth codes : production serial number, 01~99

8-Lead DFN5x6 Plastic Package
 CYS Package Code : H8

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039	E2	5.674	5.826	0.223	0.229
A3	0.254	REF	0.010	REF	k	1.190	1.390	0.047	0.055
D	4.944	5.096	0.195	0.201	b	0.350	0.450	0.014	0.018
E	5.974	6.126	0.235	0.241	e	1.270	TYP	0.050	TYP
D1	1.470	1.870	0.058	0.074	L	0.559	0.711	0.022	0.028
D2	0.470	0.870	0.019	0.034	L1	0.424	0.576	0.017	0.023
E1	3.375	3.575	0.133	0.141	H	0.574	0.726	0.023	0.029
D3	4.824	4.976	0.190	0.196	θ	10°	12°	10°	12°

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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