

Dual P-Channel Enhancement Mode Power MOSFET

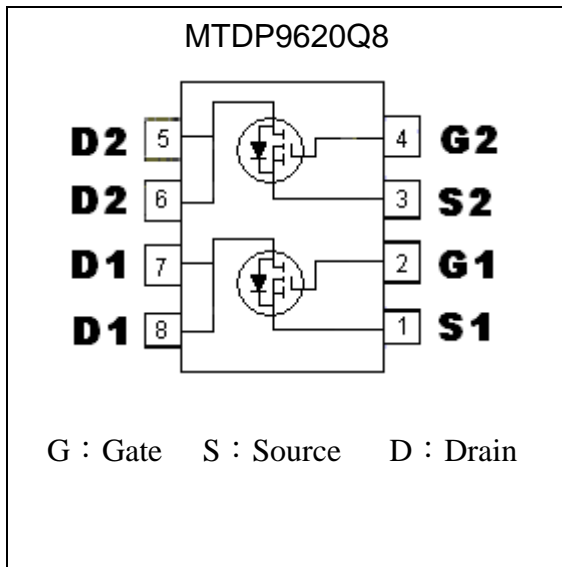
MTDP9620Q8

BVDSS	-20V
ID@VGS=-4.5V, TA=25°C	-5.2A
ID@VGS=-4.5V, TC=25°C	-8.8A
RDSON@VGS=-4.5V, ID=-6.5A	16.4mΩ (typ)
RDSON@VGS=-2.5V, ID=-4.2A	19.8mΩ (typ)
RDSON@VGS=-1.8V, ID=-3.5A	24.7mΩ (typ)

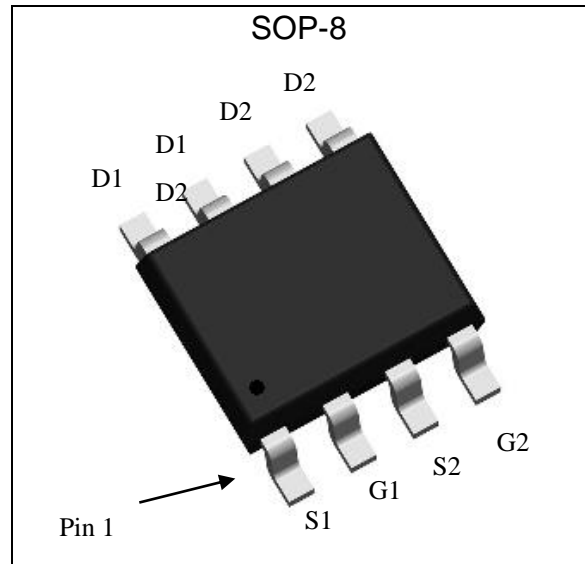
Features

- Simple drive requirement
- Low on-resistance
- Fast switching speed
- Pb-free lead plating and halogen-free package

Equivalent Circuit

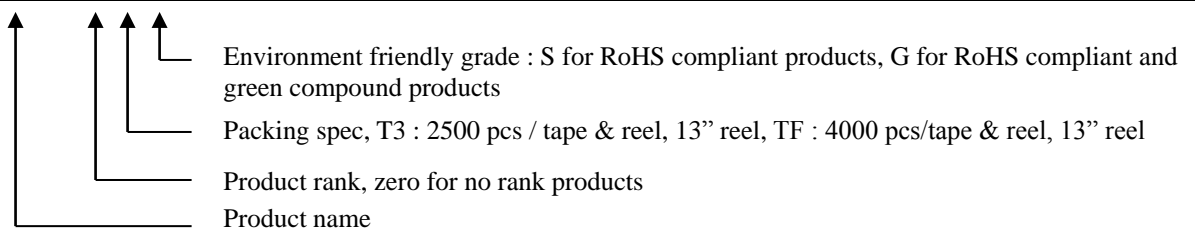


Outline



Ordering Information

Device	Package	Shipping
MTDP9620Q8-0-T3-G	SOP-8 (Pb-free lead plating and halogen-free package)	2500 pcs / tape & reel
MTDP9620Q8-0-TF-G	SOP-8 (Pb-free lead plating and halogen-free package)	4000 pcs / tape & reel





Absolute Maximum Ratings (Ta=25°C)

Parameter		Symbol	10s	Steady State	Unit
Drain-Source Voltage		V _{DS}	-20		V
Gate-Source Voltage		V _{GS}	±8		
Continuous Drain Current @ T _C =25°C, V _{GS} =-4.5V (Note1)		I _D	-8.8		A
Continuous Drain Current @ T _C =100°C, V _{GS} =-4.5V (Note1)			-5.6		
Continuous Drain Current @ T _A =25°C, V _{GS} =-4.5V (Note2)		I _{DSM}	-7.0	-5.2	
Continuous Drain Current @ T _A =70°C, V _{GS} =-4.5V (Note2)			-5.6	-4.2	
Pulsed Drain Current (Note3)		I _{DM}	-40 *1,2		
Total Power Dissipation	T _C =25°C (Note1)	P _D	3.1		
	T _C =100°C (Note1)		1.2		
	T _A =25°C (Note2)	P _{DSM}	2.0	1.1	
	T _A =70°C (Note2)		1.3	0.7	
Operating Junction and Storage Temperature Range		T _j , T _{stg}	-55~+150		°C

Thermal Data

Parameter	Symbol	Typical	Maximum	Unit
Thermal Resistance, Junction-to-case	R _{th,j-c}	34	40	°C/W
Thermal Resistance, Junction-to-ambient (Note2)	R _{th,j-a}	t≤10s	58	
		Steady State	91	
			110	

- Note : 1.The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
2. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2 oz. copper, in a still air environment with T_A=25°C. The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
3. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and low duty cycles to keep initial T_J=25°C.

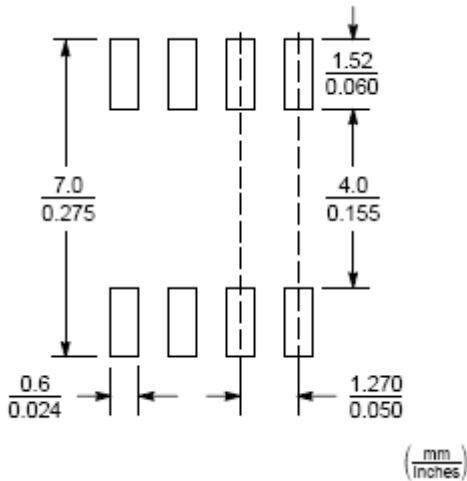
Electrical Characteristics (Tc=25°C, unless otherwise noted)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	-20	-	-	V	V _{GS} =0V, I _D =-250μA
V _{GS(th)}	-0.3	-	-0.8		V _{DS} =V _{GS} , I _D =-250μA
I _{GSS}	-	-	±100	nA	V _{GS} =±8V, V _{DS} =0V
I _{DSS}	-	-	-1	μA	V _{DS} =-20V, V _{GS} =0V
I _{DSS}	-	-	-5		V _{DS} =-20V, V _{GS} =0V, T _j =55°C
R _{DS(ON)} (Note 1)	-	16.4	28	mΩ	I _D =-6.5A, V _{GS} =-4.5V
	-	19.8	35		I _D =-4.2A, V _{GS} =-2.5V
	-	24.7	45		I _D =-3.5A, V _{GS} =-1.8V
G _{FS} (Note 1)	-	19.1	-	S	V _{DS} =-5V, I _D =-4.8A

Dynamic					
Ciss	-	2378	3567	pF	V _{DS} =-10V, V _{GS} =0V, f=1MHz
Coss	-	217	326		
Crss	-	181	272		
t _{d(ON)} (Note 1&2)	-	14.6	22	ns	V _{DS} =-10V, I _D =-1A, V _{GS} =-4.5V, R _G =6Ω
t _r (Note 1&2)	-	24.6	37		
t _{d(OFF)} (Note 1&2)	-	196.2	294		
t _f (Note 1&2)	-	166	249		
Q _g (Note 1&2)	-	24.7	37	nC	V _{DS} =-10V, I _D =-6.5A, V _{GS} =-4.5V
Q _{gs} (Note 1&2)	-	2.9	-		
Q _{gd} (Note 1&2)	-	4.9	-		
R _g	-	13.5	-	Ω	f=1MHz
Source-Drain Diode					
I _S	-	-	-1.7	A	
I _{SM} (Note 3)	-	-	-10		
V _{SD} (Note 1)	-	-0.72	-1.2	V	I _S =-1.7A, V _{GS} =0V
t _{rr}	-	40.7	-	ns	I _F =-1.7A, dI _F /dt=100A/μs
Q _{rr}	-	15	-	nC	

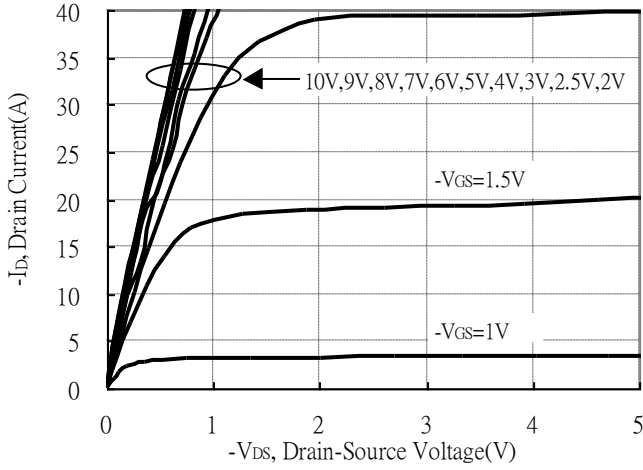
Note : 1.Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%
 2.Independent of operating temperature
 3.Pulse width limited by maximum junction temperature

Recommended Soldering Footprint

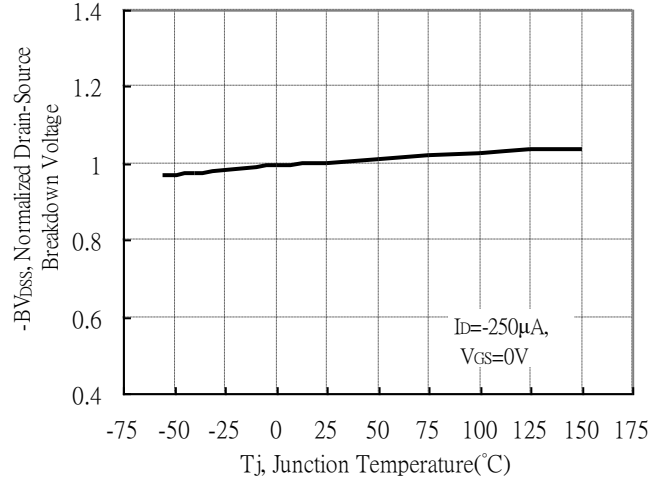


Typical Characteristics

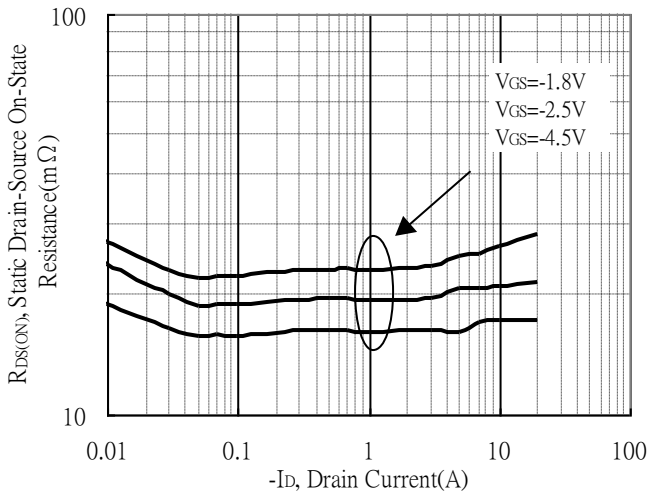
Typical Output Characteristics



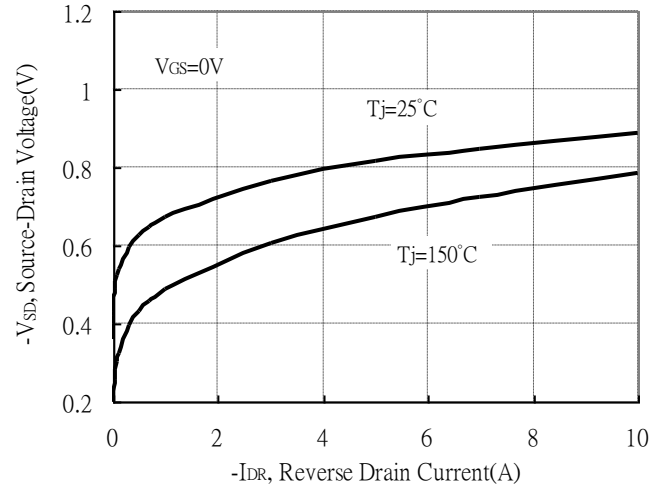
Breakdown Voltage vs Ambient Temperature



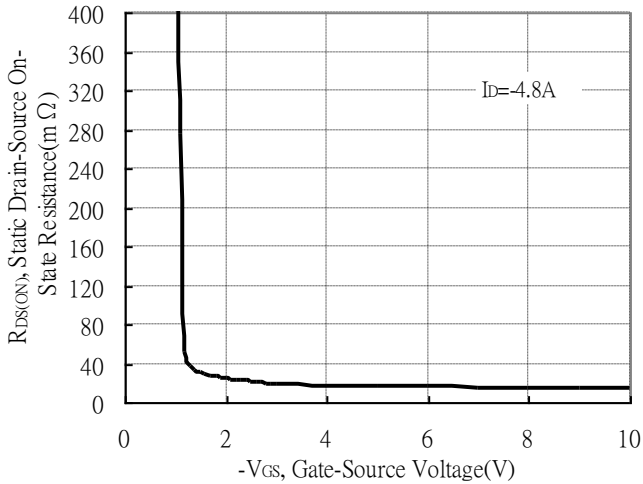
Static Drain-Source On-State resistance vs Drain Current



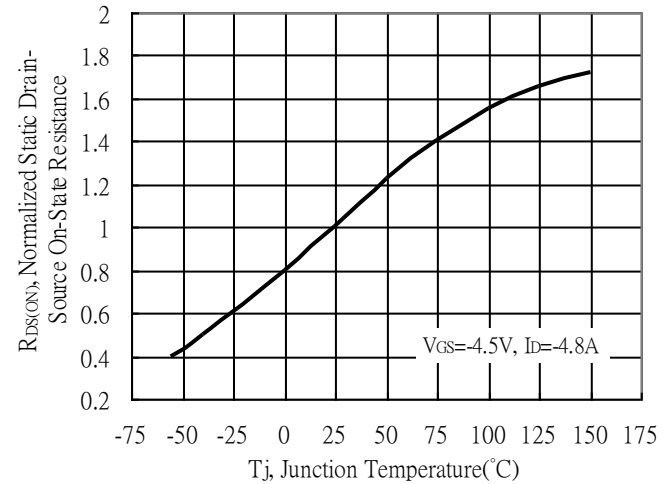
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

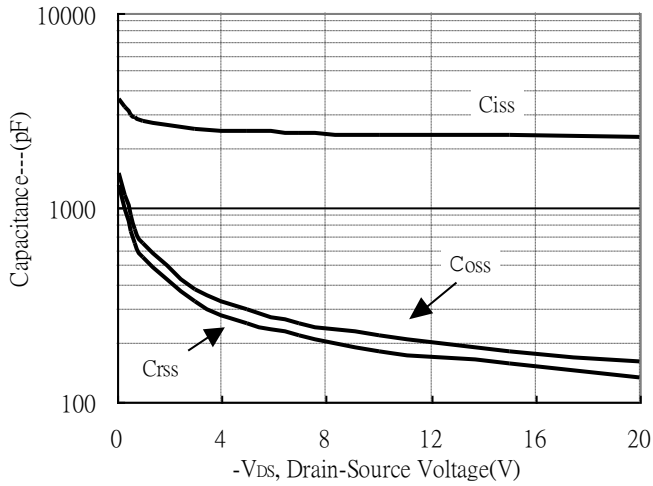


Drain-Source On-State Resistance vs Junction Temperature

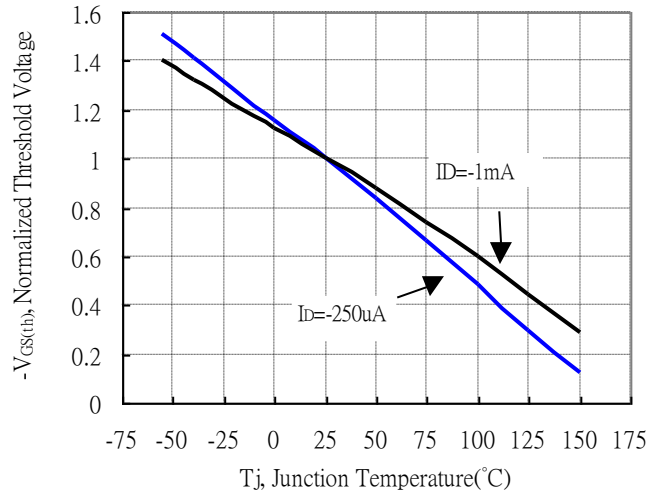


Typical Characteristics(Cont.)

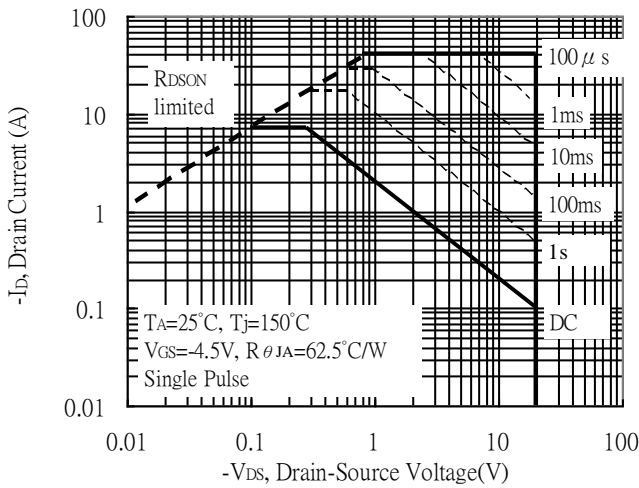
Capacitance vs Drain-to-Source Voltage



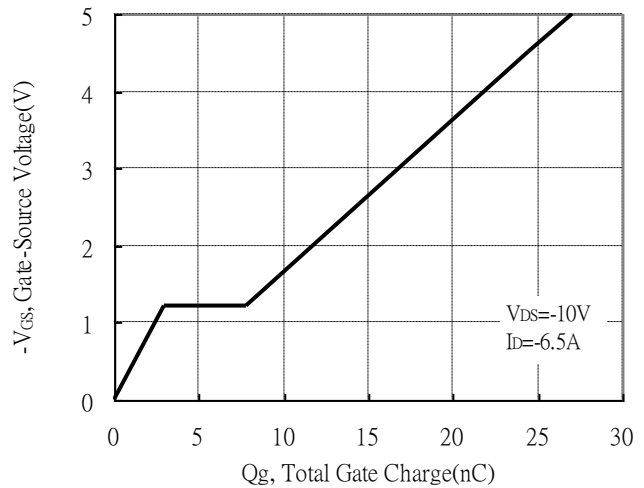
Threshold Voltage vs Junction Temperature



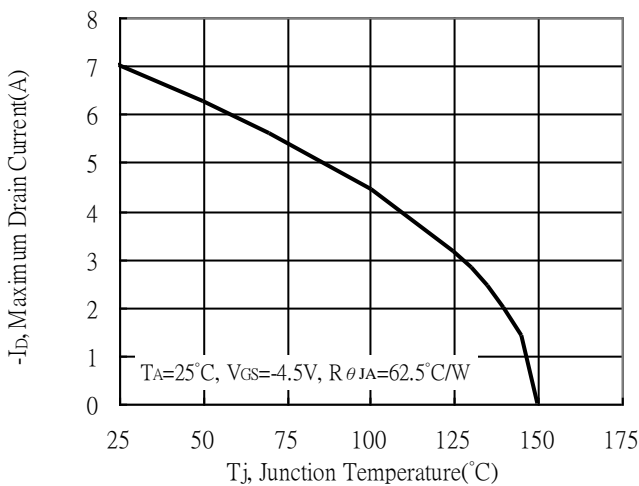
Maximum Safe Operating Area



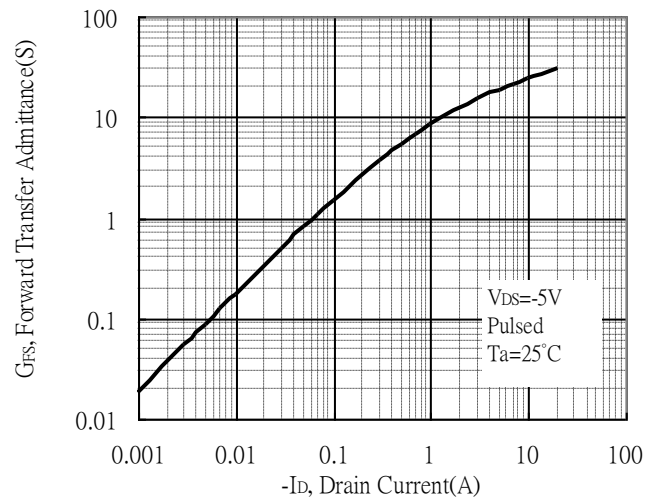
Gate Charge Characteristics



Maximum Drain Current vs Junction Temperature

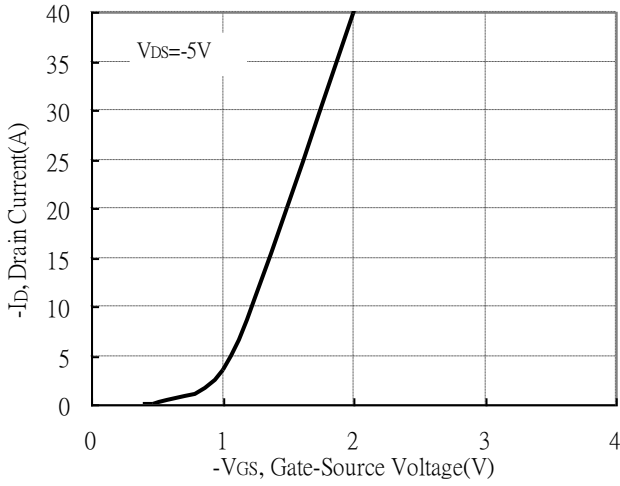


Forward Transfer Admittance vs Drain Current

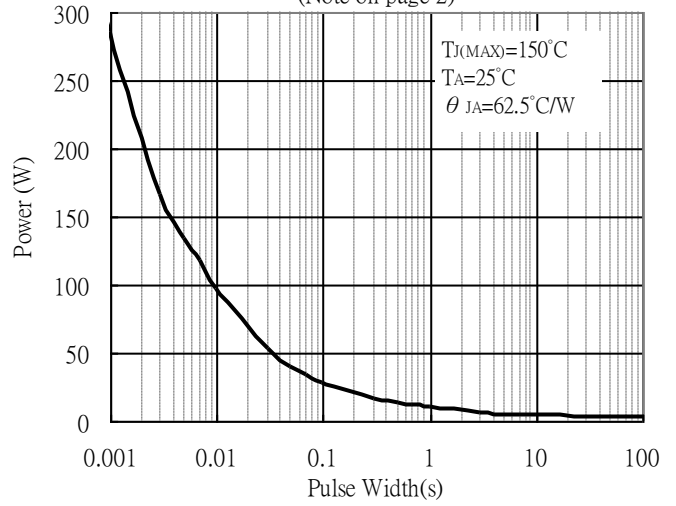


Typical Characteristics(Cont.)

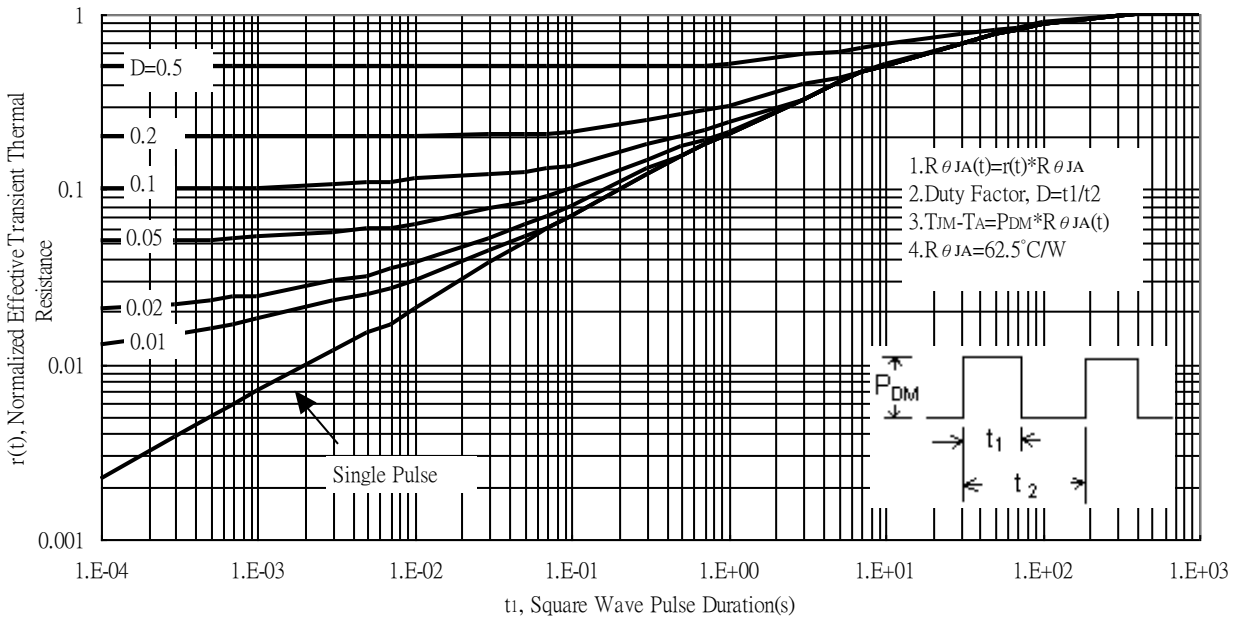
Typical Transfer Characteristics



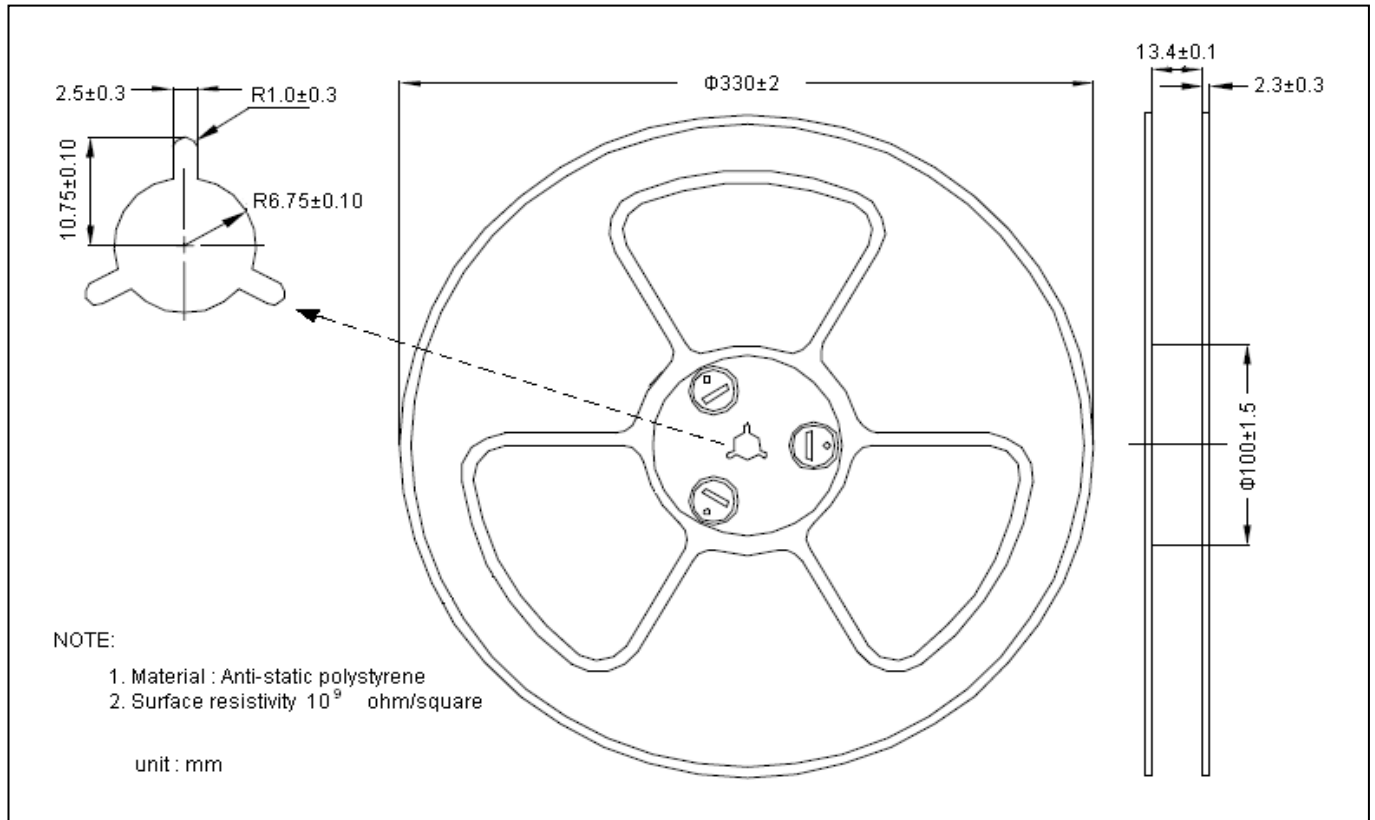
Single Pulse Power Rating, Junction to Ambient
 (Note on page 2)



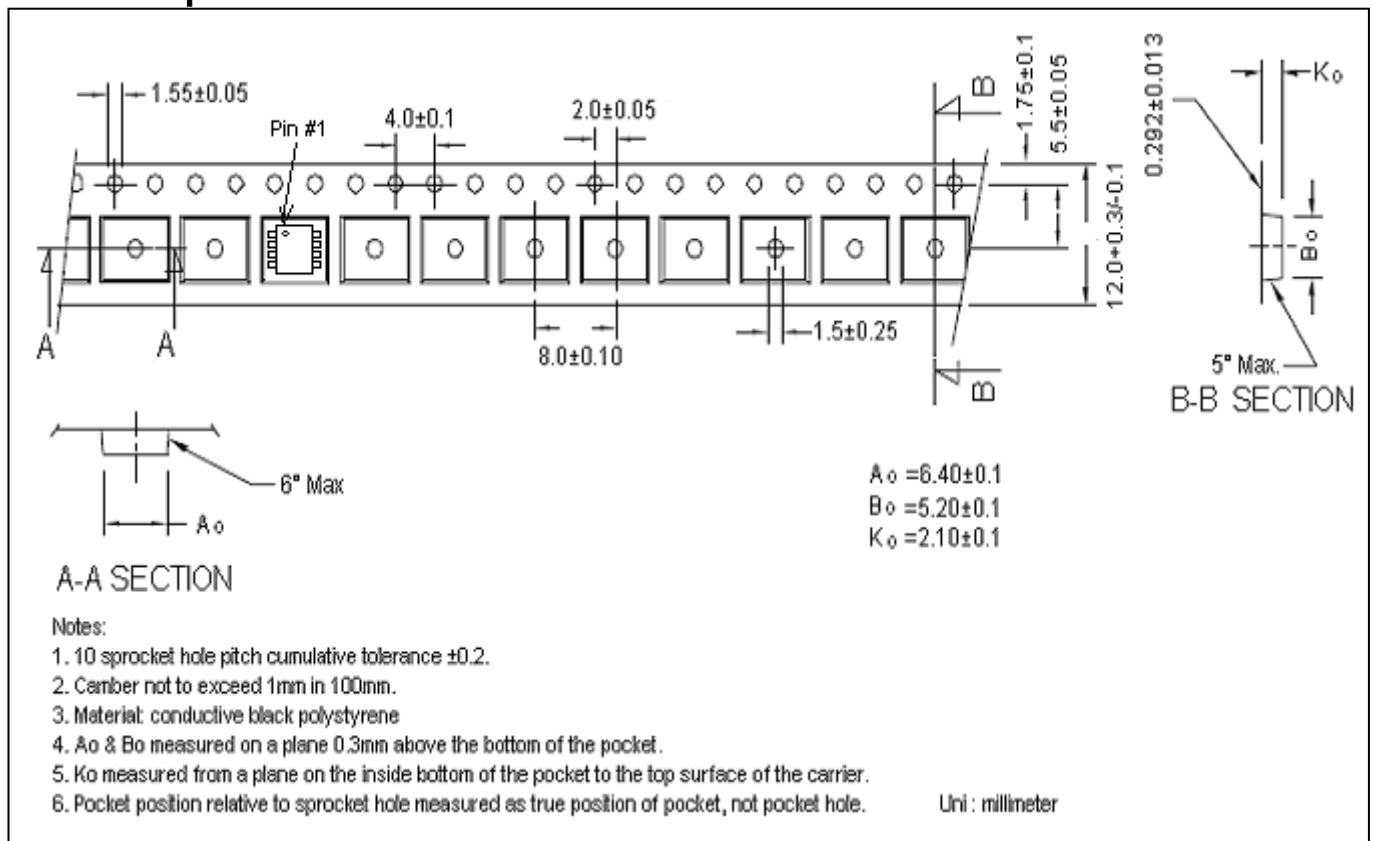
Transient Thermal Response Curves



Reel Dimension



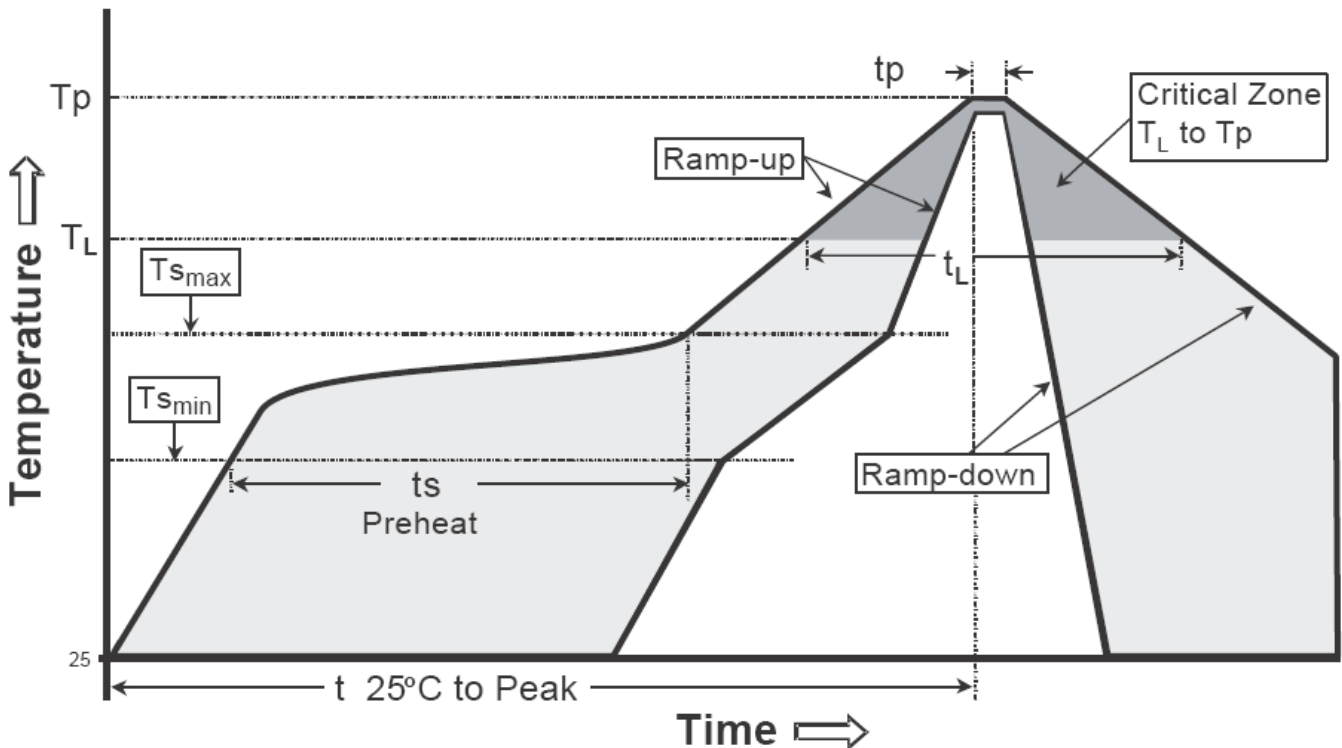
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

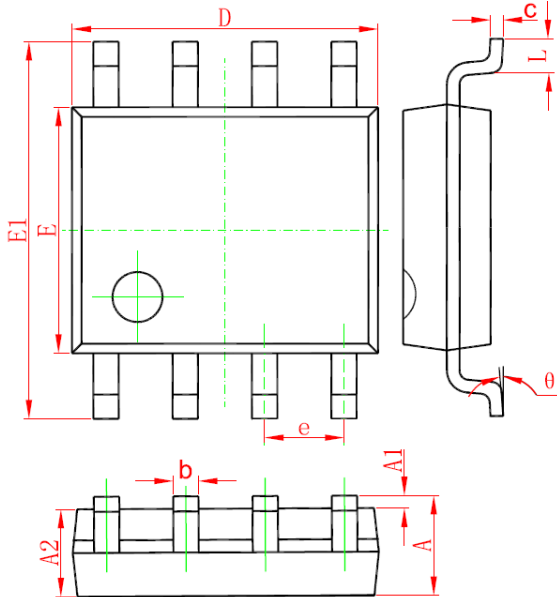
Recommended temperature profile for IR reflow



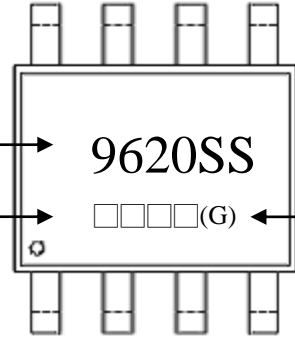
Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

SOP-8 Dimension



Marking:



Device Code → **9620SS**

Date Code → [][][][](G) ← Assembly site code

Date Code(counting from left to right) :

1st code: year code, the last digit of Christian year

2nd code : month code, Jan→A, Feb→B, Mar→C, Apr→D
 May→E, Jun→F, Jul→G, Aug→H, Sep→J,
 Oct→K, Nov→L, Dec→M

3rd and 4th codes : production serial number, 01~99

Assembly site code : blank→ JCET, G →GEM

8-Lead SOP-8 Plastic Package
 CYStek Package Code: Q8

*: Typical

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069	E	3.800	4.000	0.150	0.157
A1	0.100	0.250	0.004	0.010	E1	5.800	6.200	0.228	0.244
A2	1.350	1.550	0.053	0.061	e	*1.270		*0.050	
b	0.330	0.510	0.013	0.020	L	0.400	1.270	0.016	0.050
c	0.170	0.250	0.006	0.010	θ	0°	8°	0°	8°
D	4.700	5.100	0.185	0.200					

- Notes:** 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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