

# P-Channel Enhancement Mode MOSFET

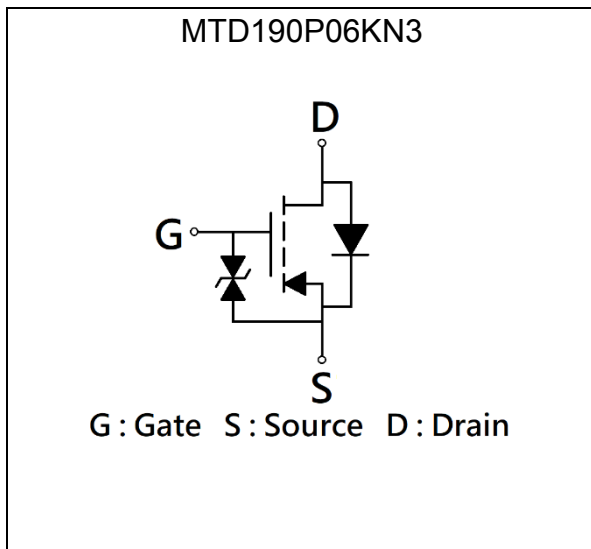
## MTD190P06KN3

### Features

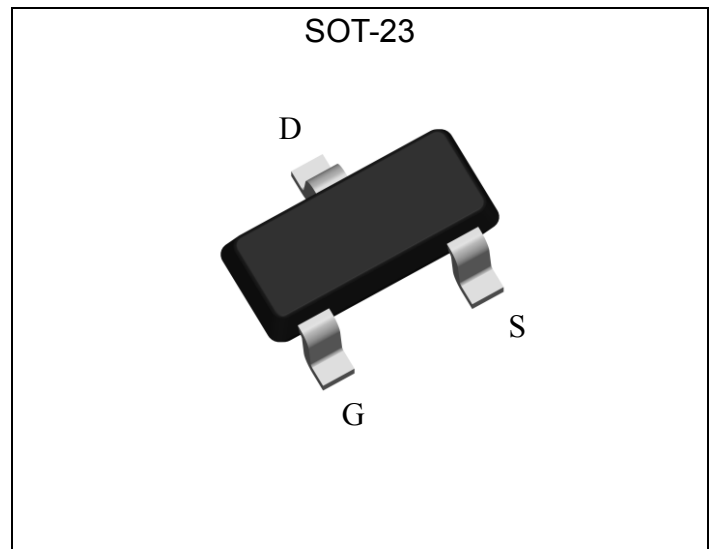
- Low On Resistance
- Low Gate Charge
- Fast Switching Characteristic
- ESD protected gate

$BV_{DSS}$	-60V
$I_D @ V_{GS} = -10V, T_A = 25^\circ C$	-2.2A
$R_{DS(ON) typ.} @ V_{GS} = -10V, I_D = -2A$	165m $\Omega$
$R_{DS(ON) typ.} @ V_{GS} = -4.5V, I_D = -1A$	270m $\Omega$

### Equivalent Circuit

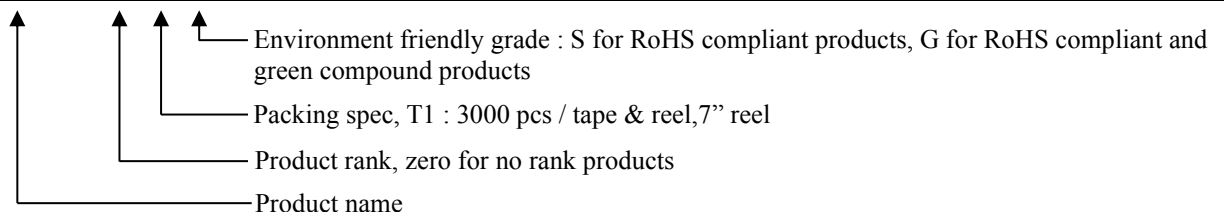


### Outline



### Ordering Information

Device	Package	Shipping
MTD190P06KN3-0-T1-G	SOT-23 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel



**Absolute Maximum Ratings (T<sub>A</sub>=25°C)**

Parameter	Symbol	Limits	Unit	
Drain-Source Voltage	V <sub>DS</sub>	-60	V	
Gate-Source Voltage	V <sub>GS</sub>	±20		
Continuous Drain Current @ V <sub>GS</sub> =-10V, T <sub>A</sub> =25°C	I <sub>D</sub>	-2.2	A	
Continuous Drain Current @ V <sub>GS</sub> =-10V, T <sub>A</sub> =70°C		-1.8		
Pulsed Drain Current	I <sub>DM</sub>	-8.8		
Continuous Body Diode Forward Current @ T <sub>A</sub> =25°C	I <sub>S</sub>	-1		
Total Power Dissipation	P <sub>D</sub>	T <sub>A</sub> =25°C	1.4	W
		T <sub>A</sub> =70°C	0.9	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55~+150	°C	

**Thermal Data**

Parameter	Symbol	Steady State	Unit
Thermal Resistance, Junction-to-ambient	R <sub>θJA</sub>	90	°C/W

Note:

- \*a. The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2 oz. copper, in a still air environment with T<sub>A</sub>=25°C. The power dissipation P<sub>D</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
- \*b. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C. Ratings are based on low frequency and low duty cycles to keep initial T<sub>J</sub>=25°C.



**Electrical Characteristics (T<sub>A</sub>=25°C, unless otherwise specified)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
<b>Static</b>					
BV <sub>DSS</sub>	-60	-	-	V	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA
V <sub>GS(th)</sub>	-1.5	-	-3		V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA
G <sub>FS</sub>	-	3.2	-	S	V <sub>DS</sub> =-10V, I <sub>D</sub> =-2A
I <sub>GSS</sub>	-	-	±10	μA	V <sub>GS</sub> =±16V, V <sub>DS</sub> =0V
I <sub>DSS</sub>	-	-	-1		V <sub>DS</sub> =-48V, V <sub>GS</sub> =0V
R <sub>DS(ON)</sub>	-	165	210	mΩ	V <sub>GS</sub> =-10V, I <sub>D</sub> =-2A
	-	270	350		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-1A
<b>Dynamic</b>					
C <sub>iss</sub>	-	337	-	pF	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V, f=1MHz
C <sub>oss</sub>	-	36	-		
C <sub>rss</sub>	-	9	-		
Q <sub>g</sub> *1, 2	-	6.9	-	nC	V <sub>DS</sub> =-30V, I <sub>D</sub> =-2A, V <sub>GS</sub> =-10V
Q <sub>gs</sub> *1, 2	-	0.9	-		
Q <sub>gd</sub> *1, 2	-	1.8	-		
t <sub>d(ON)</sub> *1, 2	-	40	-	ns	V <sub>DS</sub> =-30V, I <sub>D</sub> =-1A, V <sub>GS</sub> =-10V, R <sub>GS</sub> =6Ω
t <sub>r</sub> *1, 2	-	59	-		
t <sub>d(OFF)</sub> *1, 2	-	156	-		
t <sub>f</sub> *1, 2	-	259	-		
<b>Source-Drain Diode</b>					
V <sub>SD</sub> *1	-	-0.86	-1.2	V	I <sub>S</sub> =-2A, V <sub>GS</sub> =0V
t <sub>rr</sub>	-	10	-	ns	I <sub>F</sub> =-2A, dI <sub>F</sub> /dt=100A/μs
Q <sub>rr</sub>	-	5.2	-	nC	

Note:

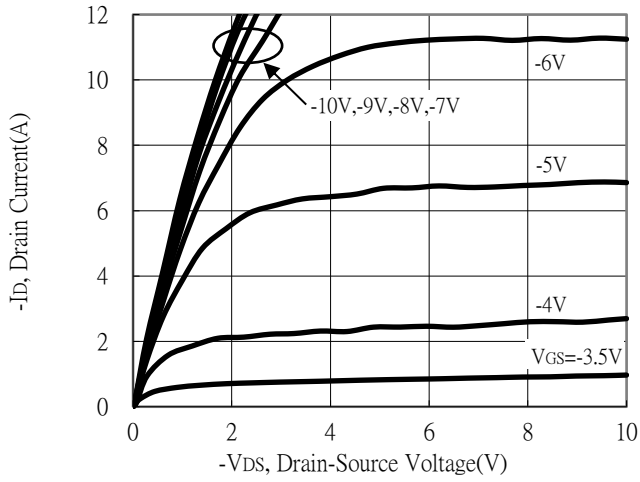
\*1. Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

\*2. Independent of operating temperature

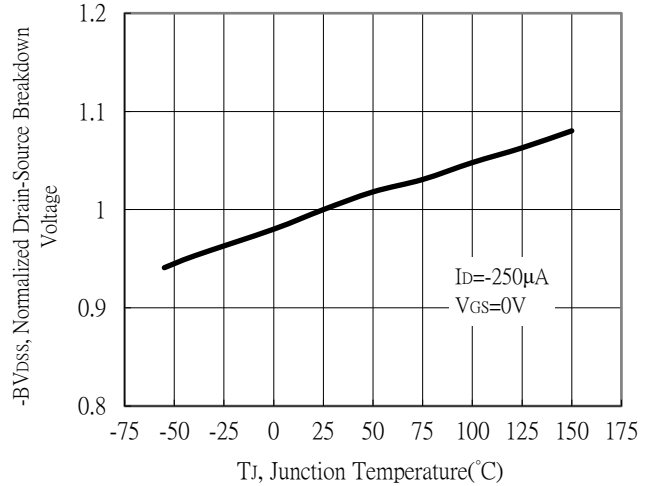


**Typical Characteristics**

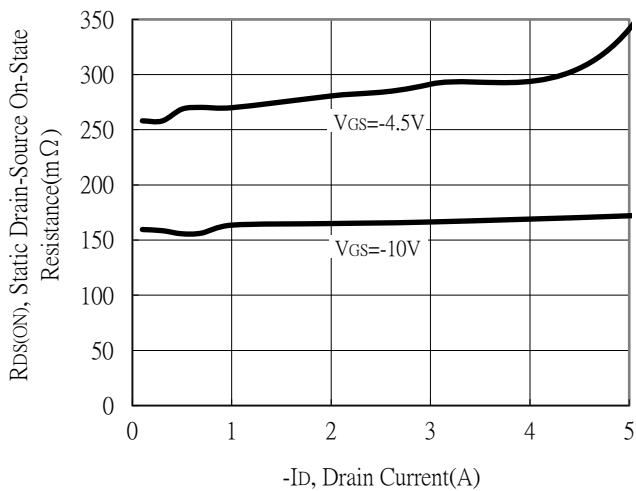
Typical Output Characteristics



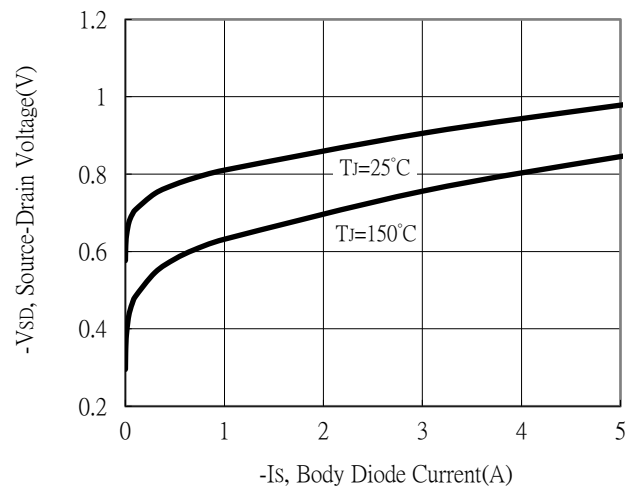
Breakdown Voltage vs Ambient Temperature



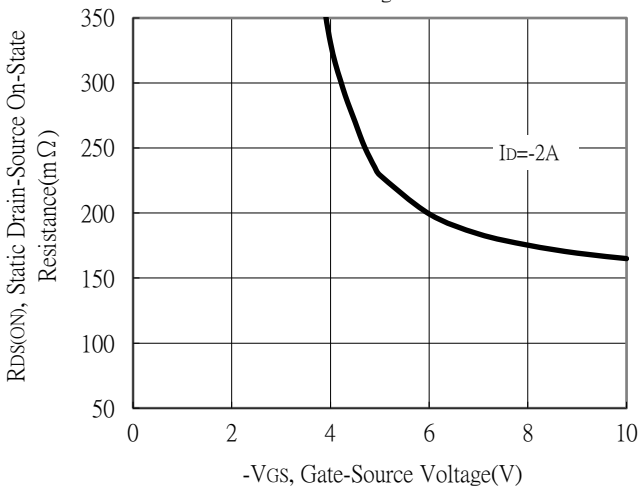
Static Drain-Source On-State resistance vs Drain Current



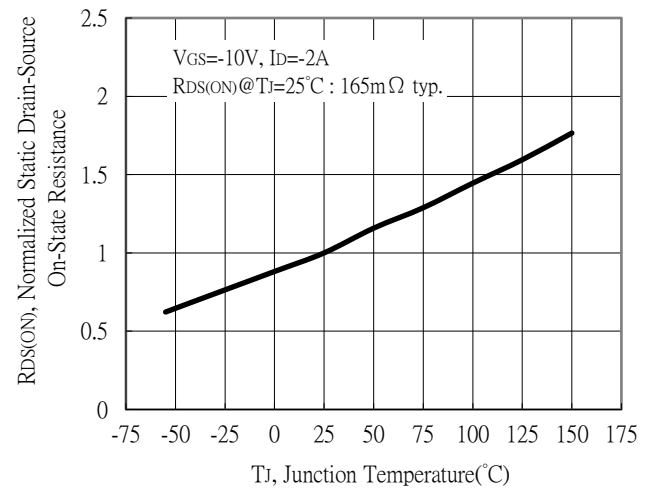
Body Diode Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

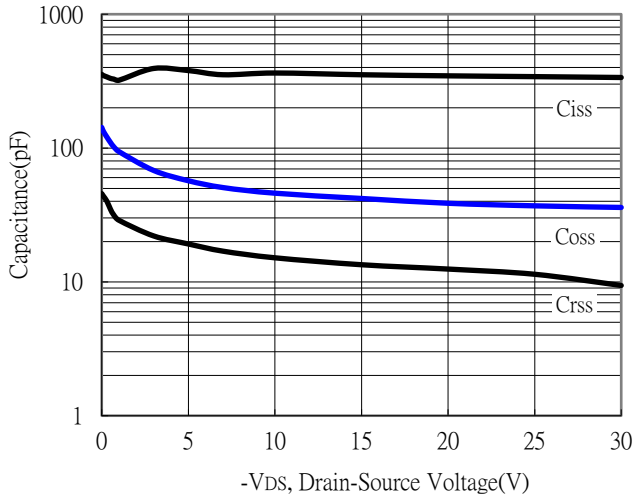


Drain-Source On-State Resistance vs Junction Temperature

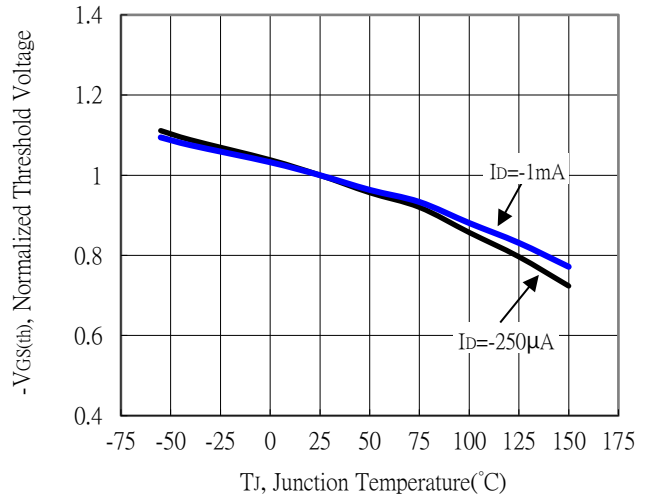


## Typical Characteristics (Cont.)

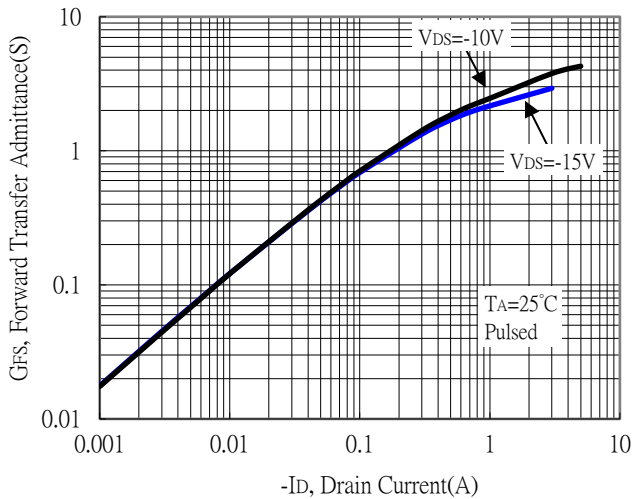
Capacitance vs Drain-to-Source Voltage



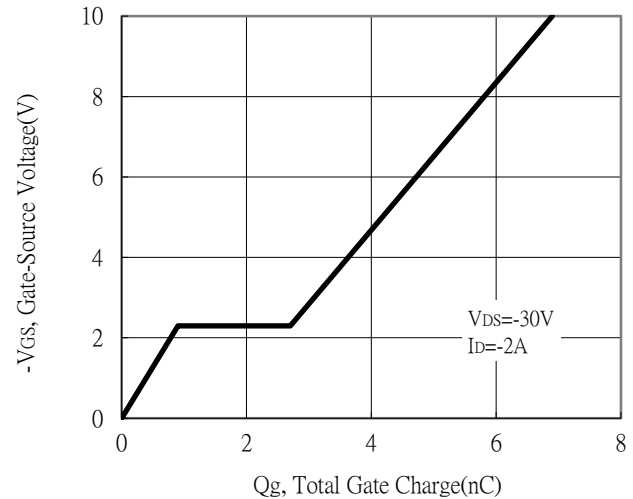
Threshold Voltage vs Junction Temperature



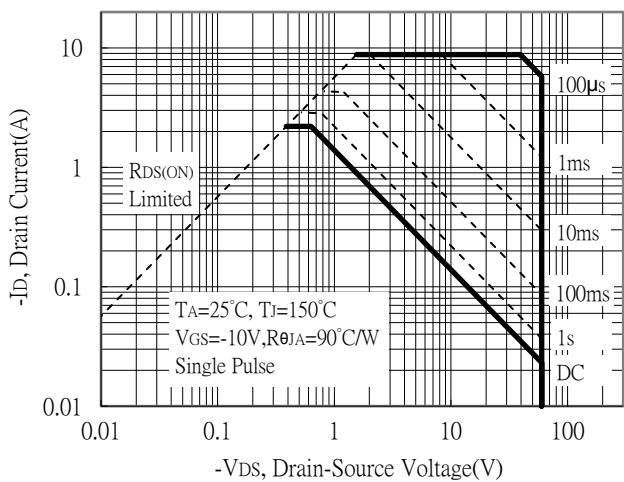
Forward Transfer Admittance vs Drain Current



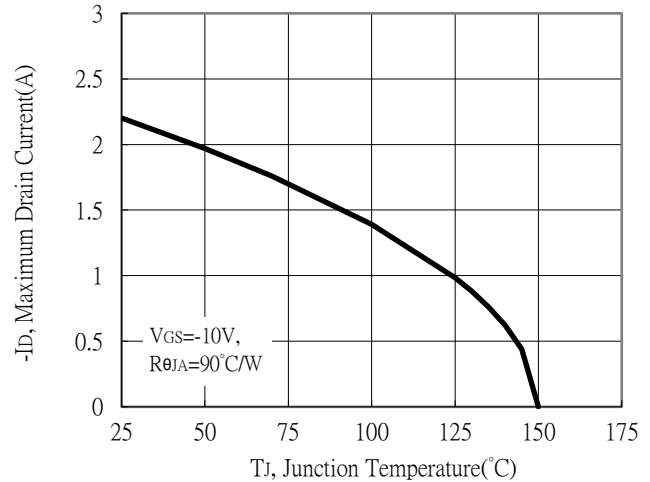
Gate Charge Characteristics



Maximum Safe Operating Area

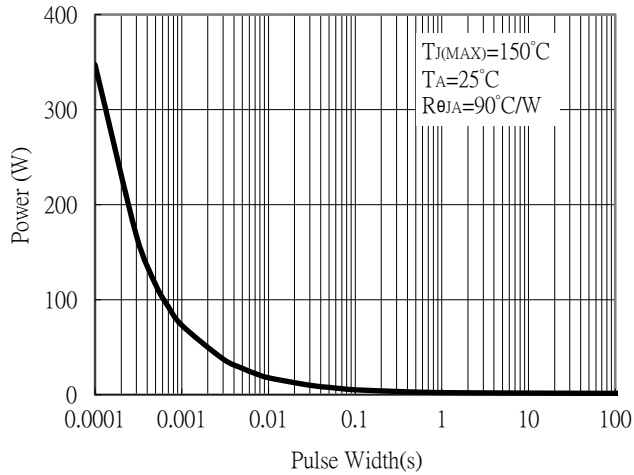


Maximum Drain Current vs Junction Temperature

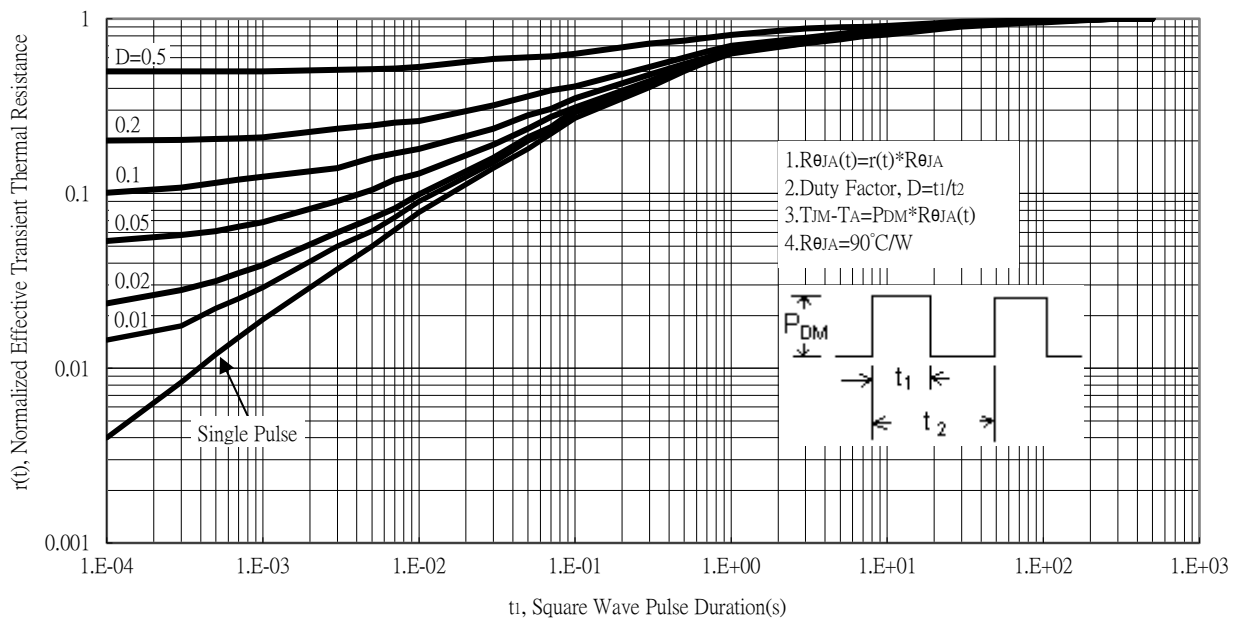


## Typical Characteristics (Cont.)

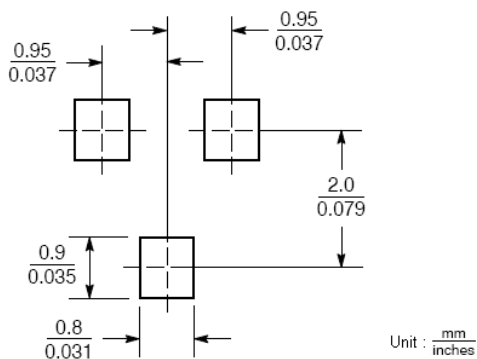
Single Pulse Power Rating, Junction to Ambient



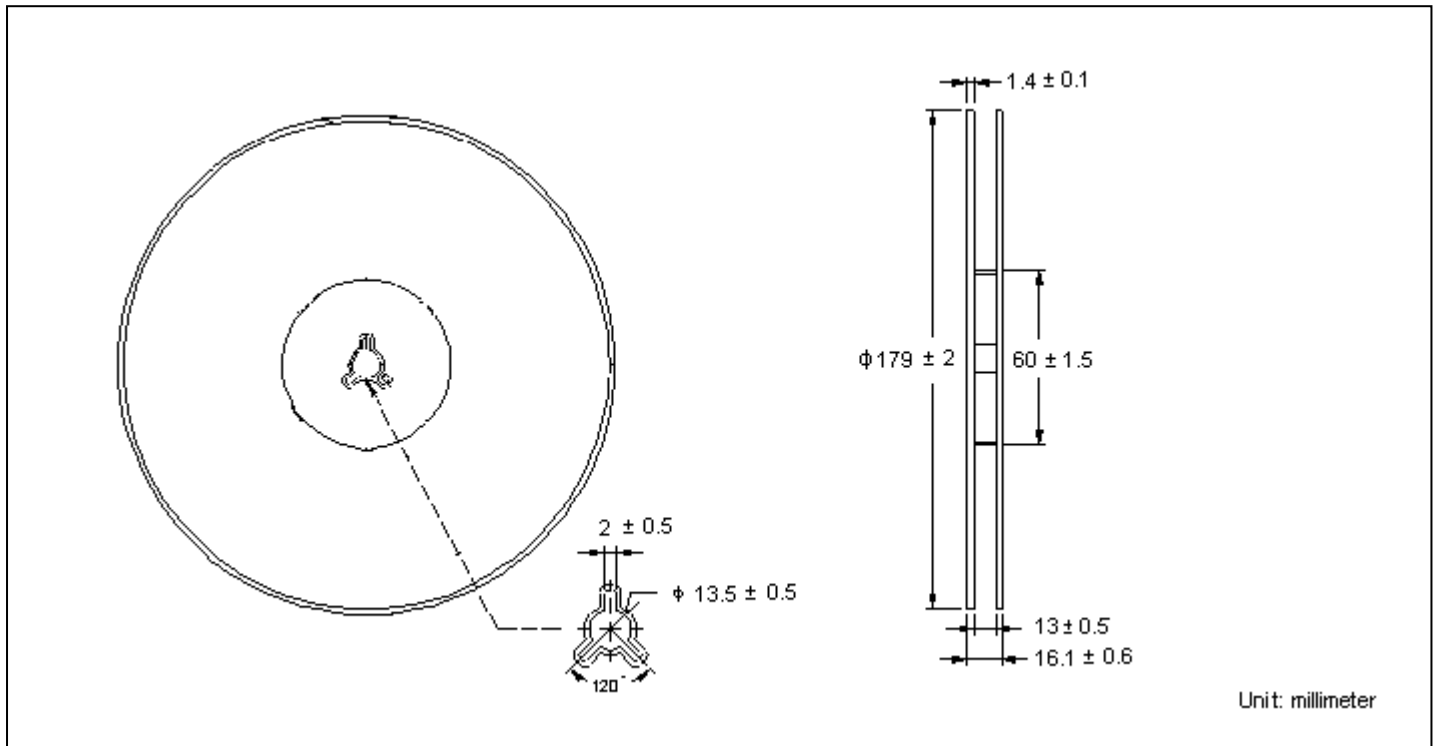
Transient Thermal Response Curves



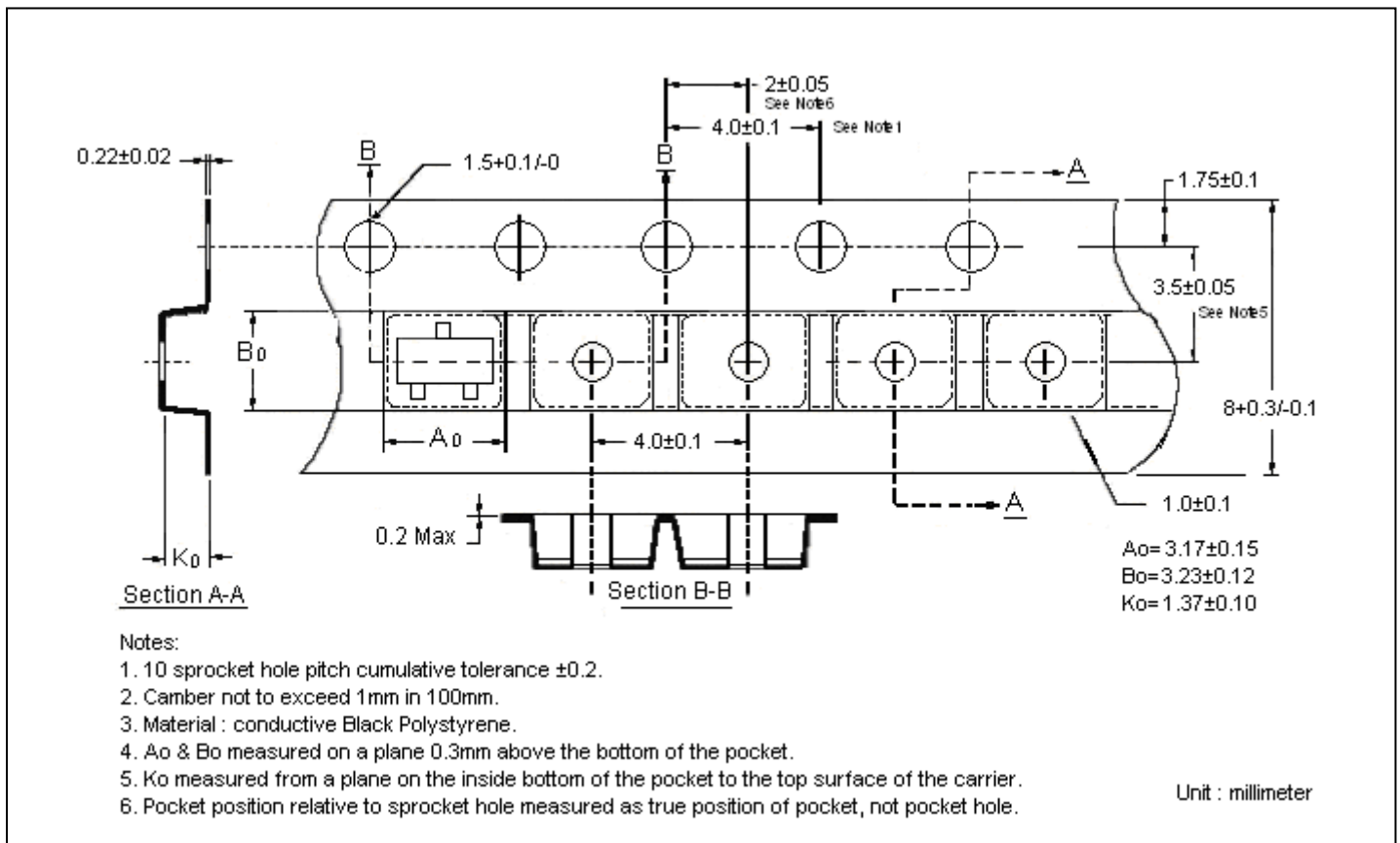
## Recommended Soldering Footprint



### Reel Dimension



### Carrier Tape Dimension



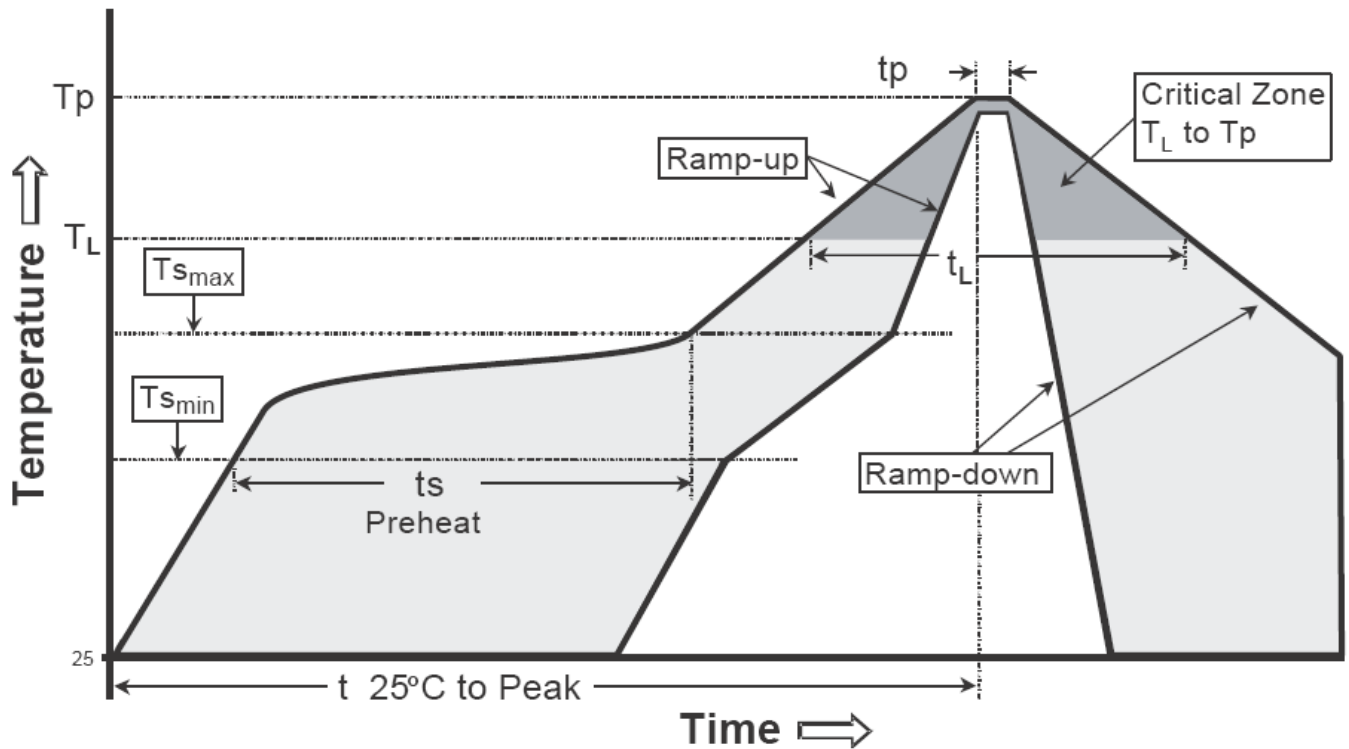
**Notes:**

1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.2$ .
2. Camber not to exceed 1mm in 100mm.
3. Material : conductive Black Polystyrene.
4. Ao & Bo measured on a plane 0.3mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

**Recommended temperature profile for IR reflow**

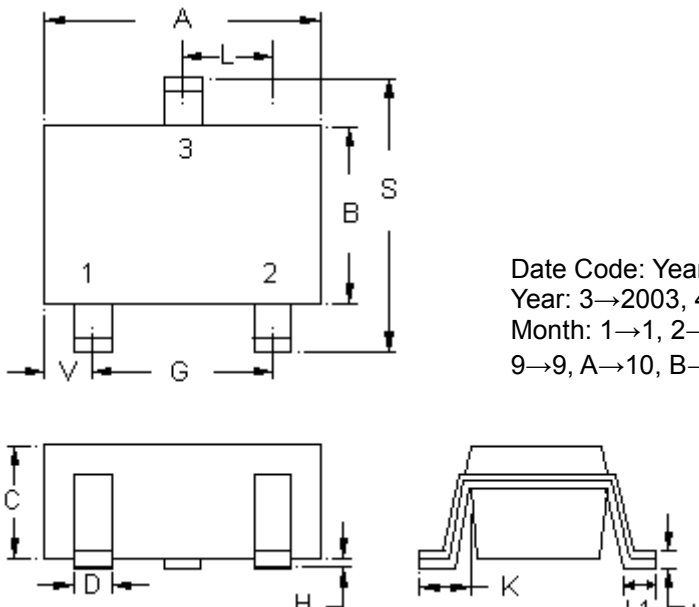


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T <sub>s min</sub> )	100°C	150°C
-Temperature Max(T <sub>s max</sub> )	150°C	200°C
-Time(t <sub>s min</sub> to t <sub>s max</sub> )	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T <sub>L</sub> )	183°C	217°C
- Time (t <sub>L</sub> )	60-150 seconds	60-150 seconds
Peak Temperature(T <sub>P</sub> )	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

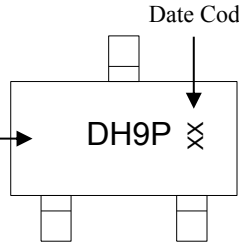


**SOT-23 Dimension**



The diagram shows four views of the SOT-23 package: a top view with dimensions A, B, C, G, S, V, and L; a side view with dimension C; a perspective view with dimensions K, L1, and L2; and a bottom view with dimension H.

**Marking:**



The marking diagram shows a rectangular package with three leads. The top lead is labeled 'Date Code' with a downward arrow. The bottom-left lead is labeled 'Device Code' with a rightward arrow. The center of the package is marked with 'DH9P' followed by a crossed-circle symbol.

Date Code: Year+Month  
 Year: 3→2003, 4→2004  
 Month: 1→1, 2→2, . . .  
 9→9, A→10, B→11, C→12

3-Lead SOT-23 Plastic  
 Surface Mounted Package  
 CYStek Package Code: N3

Style: Pin 1.Gate 2.Source 3.Drain

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1102	0.1204	2.80	3.04	J	0.0032	0.0079	0.08	0.20
B	0.0472	0.0669	1.20	1.70	K	0.0118	0.0266	0.30	0.67
C	0.0335	0.0512	0.89	1.30	L	0.0335	0.0453	0.85	1.15
D	0.0118	0.0197	0.30	0.50	S	0.0830	0.1161	2.10	2.95
G	0.0669	0.0910	1.70	2.30	V	0.0098	0.0256	0.25	0.65
H	0.0000	0.0040	0.00	0.10	L1	0.0118	0.0197	0.30	0.50

**Notes:** 1.Controlling dimension: millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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