N-Channel Enhancement Mode Power MOSFET

MTB3D8N03RH8

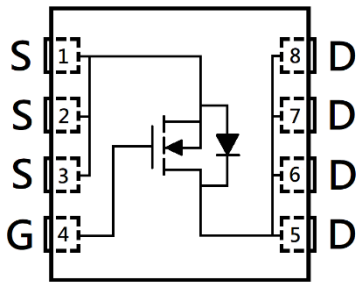
Features

- Low Gate Charge
- Fast Switching Characteristic

BV_{DSS}	30V
I_D@V_{GS}=10V, T_C=25˚C	26A
I_D@V_{GS}=10V, T_A=25˚C	19A
$R_{DS(ON)}$ typ. @V_{GS}=10V, I_D=15A	3.2mΩ
$R_{DS(ON)}$ typ. @V_{GS}=4.5V, I_D=10A	4.8mΩ

Equivalent Circuit

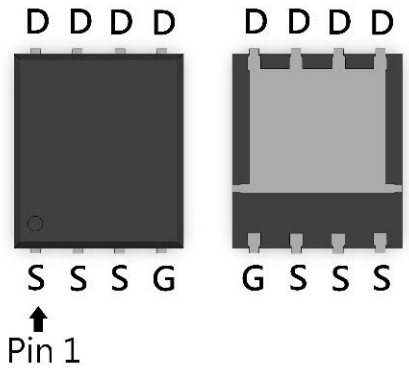
MTB3D8N03RH8



G : Gate S : Source D : Drain

Outline

DFN5×6



Ordering Information

Device	Package	Shipping
MTB3D8N03RH8-0-T6-G	DFN5×6 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel

- Environment friendly grade : S for RoHS compliant products, G for RoHS compliant and green compound products
- Packing spec, T6 : 3000 pcs / tape & reel,13” reel
- Product rank, zero for no rank products
- Product name

Absolute Maximum Ratings (T_A=25°C)

Parameter		Symbol	Limits	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current @ V_{GS}=10V, T_C=25°C (silicon limit)	*a	I_D	90	A
Continuous Drain Current @ V_{GS}=10V, T_C=25°C (package limit)	*a		26	
Continuous Drain Current @ V_{GS}=10V, T_C=100°C	*a		26	
Continuous Drain Current @ V_{GS}=10V, T_A=25°C	*b		19	
Continuous Drain Current @ V_{GS}=10V, T_A=70°C	*b		15	
Pulsed Drain Current	*c	I_{DM}	104	
Continuous Body Diode Forward Current @ T_C=25°C	*a	I_S	26	
Pulsed Body Diode Forward Current @ T_C=25°C	*a	I_{SM}	104	
Avalanche Current @ L=0.1mH		I_{AS}	18	
Avalanche Energy @ L=0.5mH		E_{AS}	25	mJ
Total Power Dissipation	T_C=25°C *a	P_D	63	W
	T_C=100°C *a		25	
	T_A=25°C *b		2.8	
	T_A=70°C *b		1.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55~+150	°C

Thermal Data

Parameter		Symbol	Steady State	Unit
Thermal Resistance, Junction-to-case		$R_{\theta JC}$	2	°C/W
Thermal Resistance, Junction-to-ambient	*b	$R_{\theta JA}$	45	

Note:

*a. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

*b. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2 oz. copper, in a still air environment with T_A=25°C. The power dissipation P_D is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

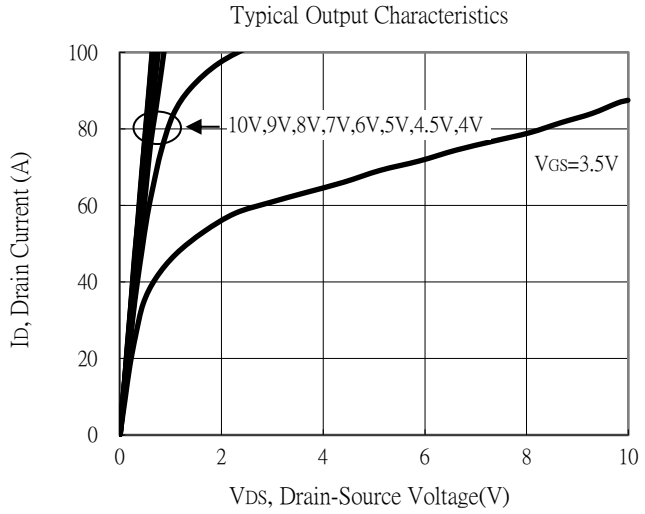
*c. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and low duty cycles to keep initial T_J=25°C.

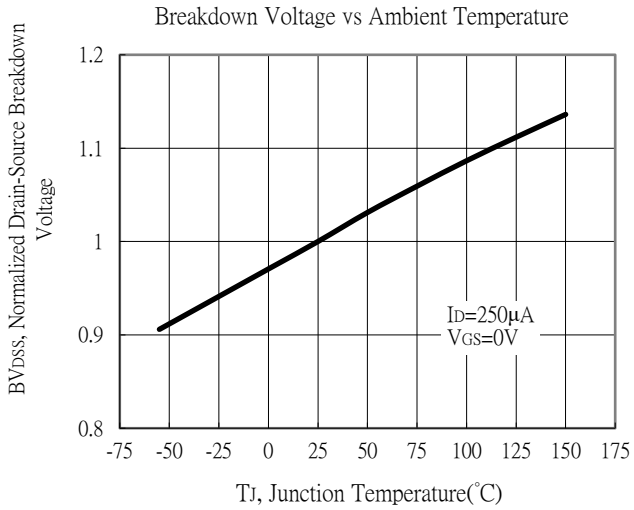
Electrical Characteristics (T_A=25°C, unless otherwise specified)

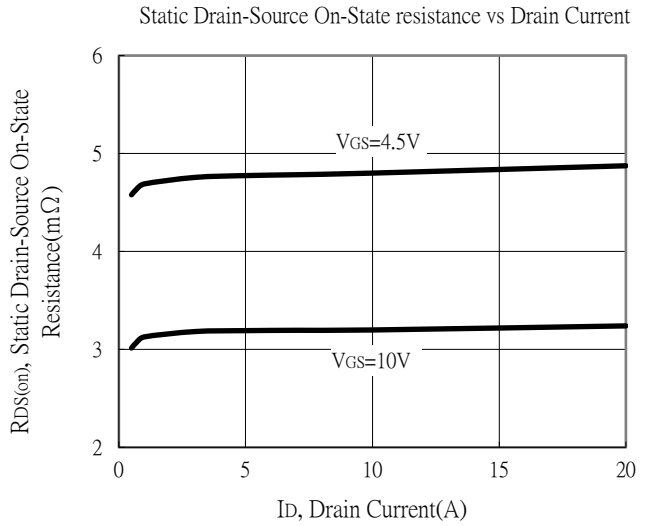
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV_{DSS}	30	-	-	V	V_{GS}=0V, I_D=250μA
$V_{GS(th)}$	1	-	2.5		V_{DS}=V_{GS}, I_D=250μA
G_{FS}	-	15	-	S	V_{DS}=10V, I_D=10A
I_{GSS}	-	-	±100	nA	V_{GS}=±20V, V_{DS}=0V
I_{DSS}	-	-	1	μA	V_{DS}=24V, V_{GS}=0V
$R_{DS(ON)}$	-	3.2	4.2	mΩ	V_{GS}=10V, I_D=15A
	-	4.8	6.7		V_{GS}=4.5V, I_D=10A
Dynamic					
Ciss	-	1280	-	pF	V_{DS}=15V, V_{GS}=0V, f=1MHz
Coss	-	860	-		
Crss	-	116	-		
Rg	-	1	-	Ω	f=1MHz
Qg *1, 2	-	11.5	-	nC	V_{DS}=15V, I_D=15A, V_{GS}=4.5V
Qg *1, 2	-	23	-		V_{DS}=15V, I_D=15A, V_{GS}=10V
Qgs *1, 2	-	4	-		
Qgd *1, 2	-	4.5	-		
$t_{d(ON)}$ *1, 2	-	12	-	ns	V_{DS}=15V, I_D=15A, V_{GS}=10V, R_{GS}=6Ω
tr *1, 2	-	14	-		
$t_{d(OFF)}$ *1, 2	-	39	-		
t_f *1, 2	-	10	-		
Source-Drain Diode					
V_{SD} *1	-	0.83	1.2	V	I_S=15A, V_{GS}=0V
trr	-	28	-	ns	I_F=15A, dI_F/dt=100A/μs
Qrr	-	14	-	nC	

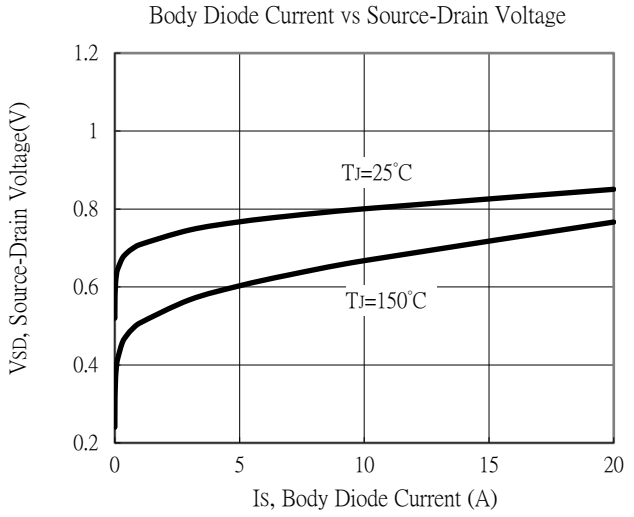
Note:
*1. Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%
*2. Independent of operating temperature

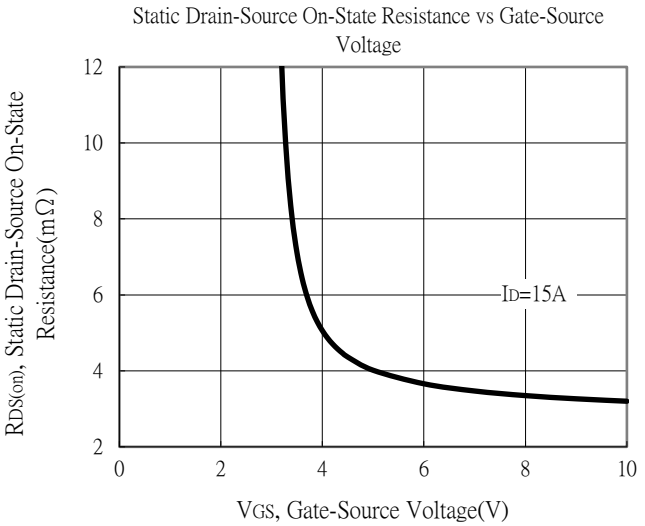
Typical Characteristics

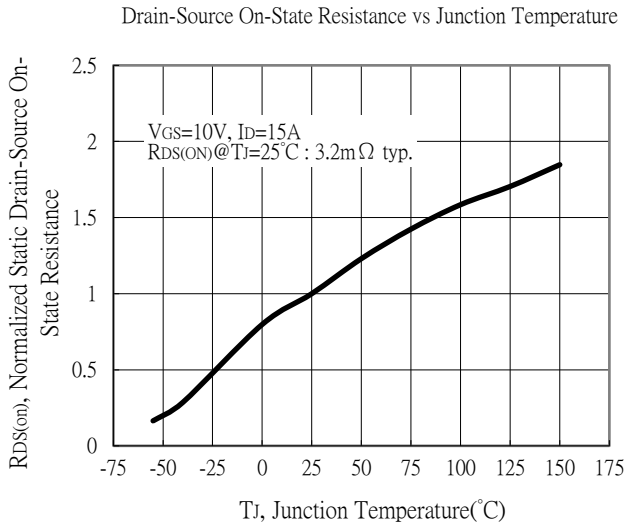






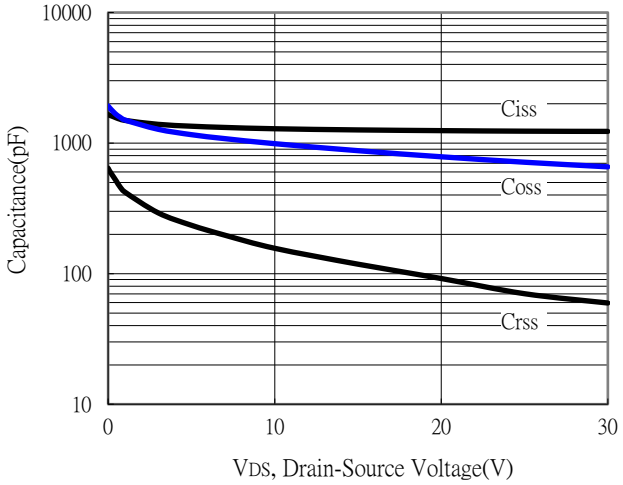




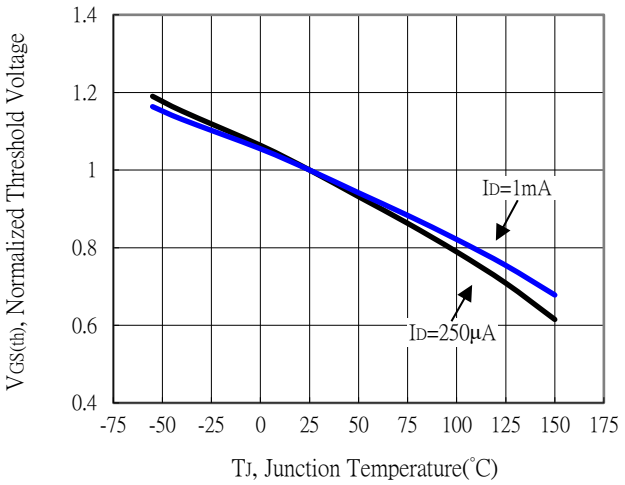


Typical Characteristics (Cont.)

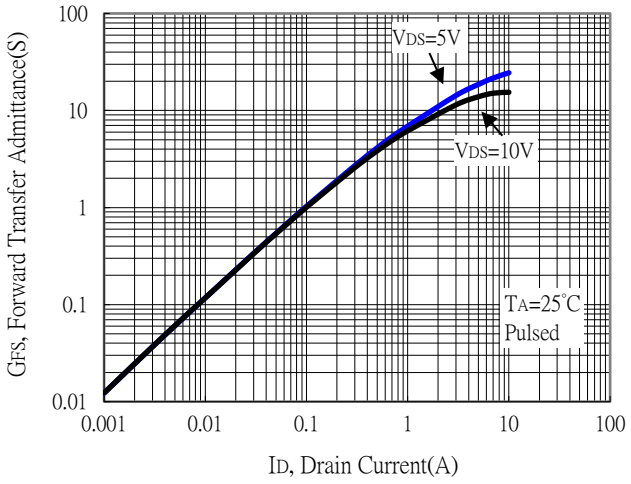
Capacitance vs Drain-to-Source Voltage



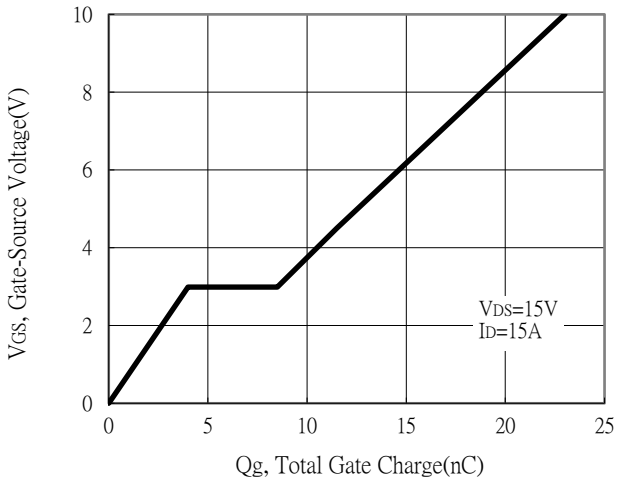
Threshold Voltage vs Junction Temperature



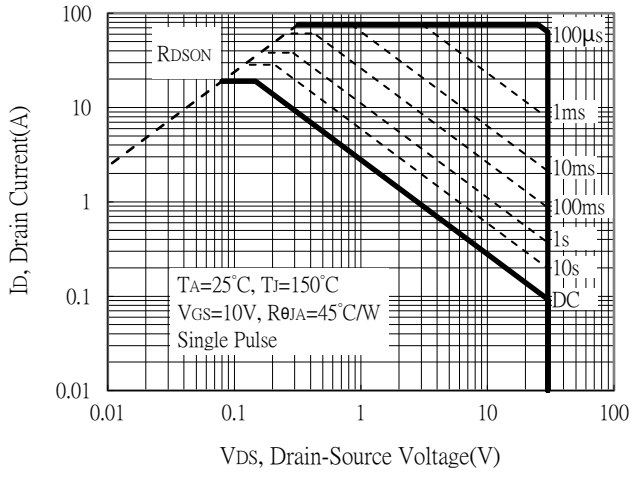
Forward Transfer Admittance vs Drain Current



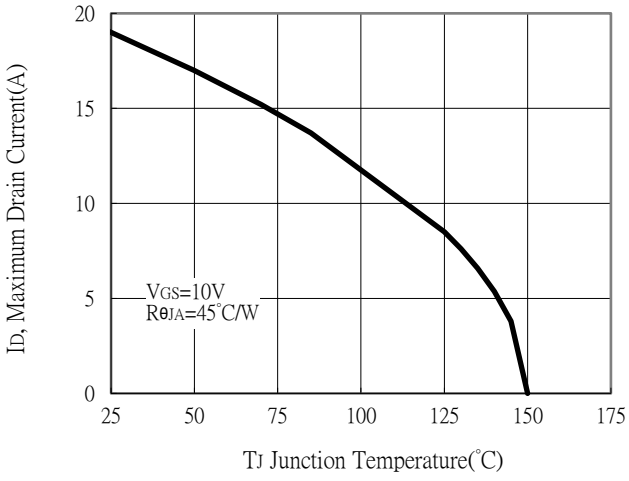
Gate Charge Characteristics



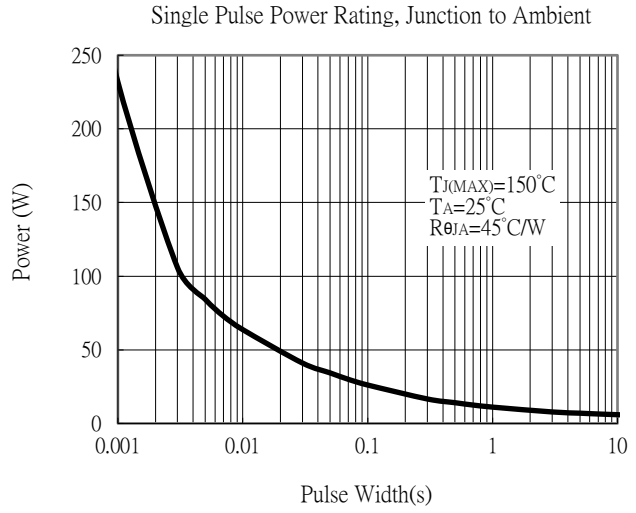
Maximum Safe Operating Area

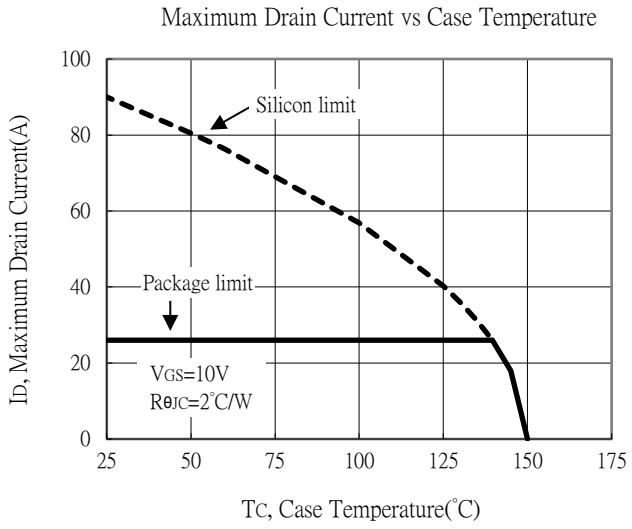


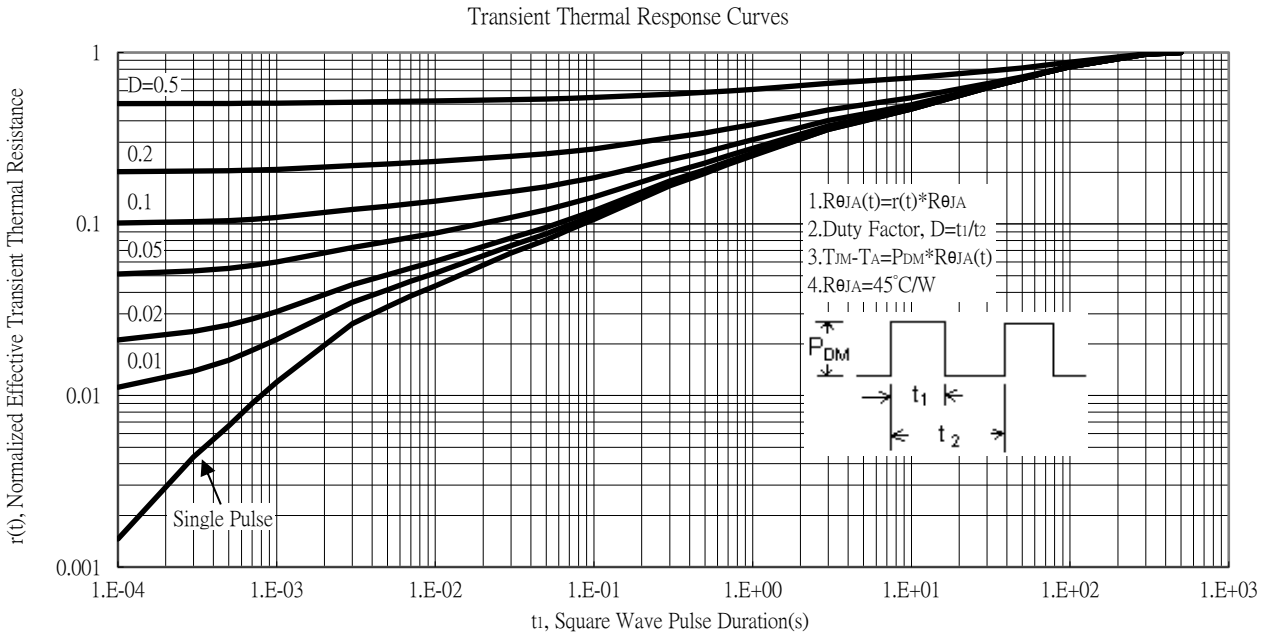
Maximum Drain Current vs Junction Temperature



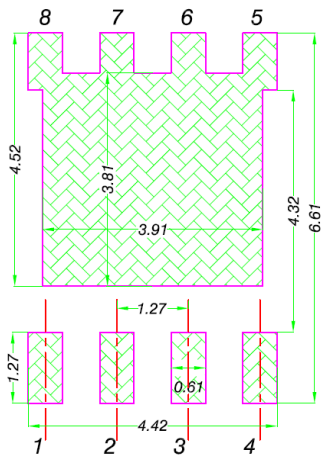
Typical Characteristics (Cont.)





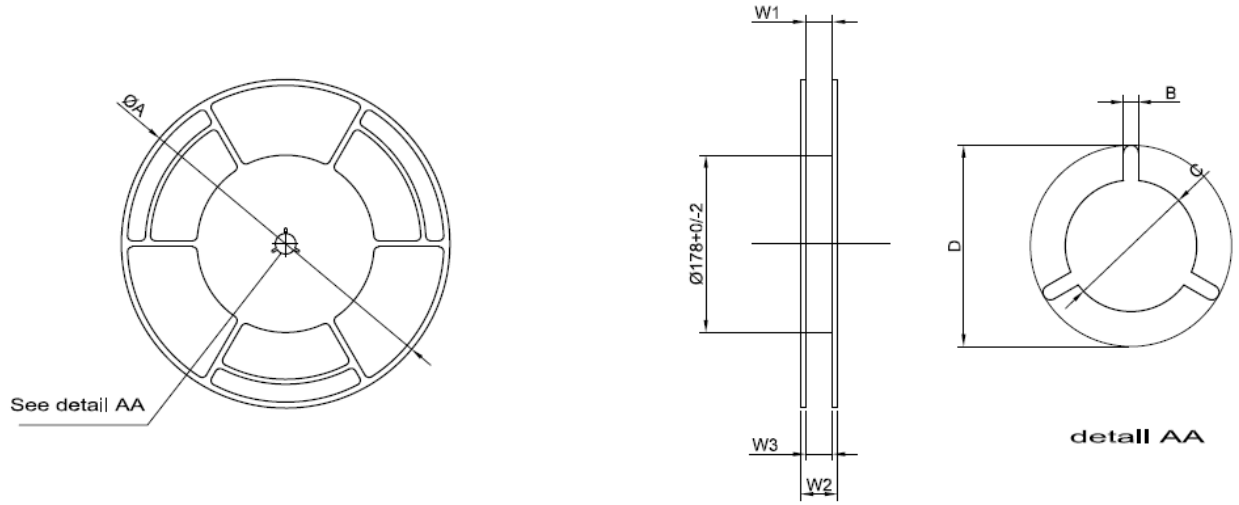


Recommended Soldering Footprint



Unit : mm

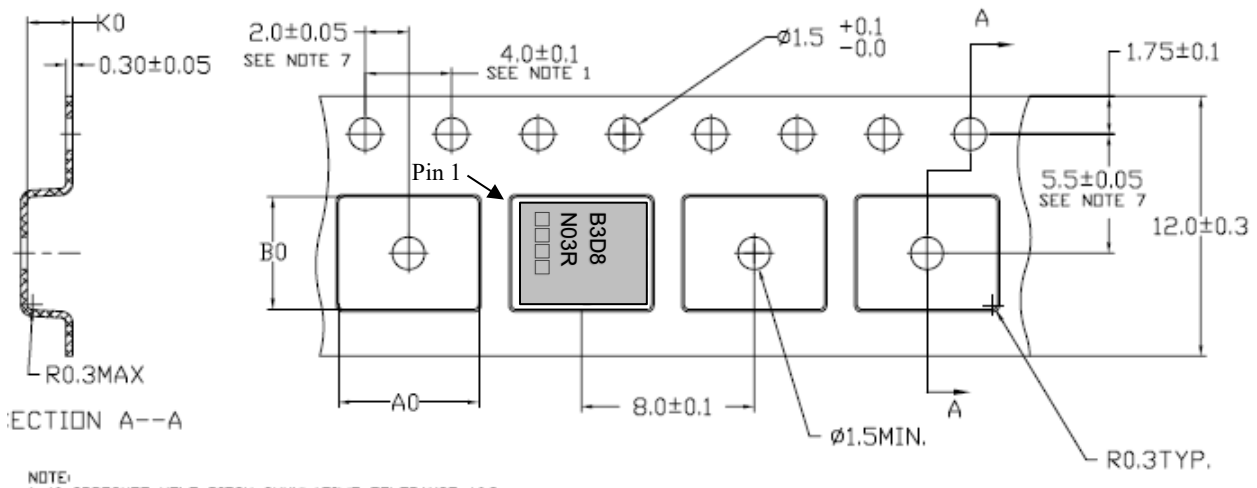
Reel Dimension



TAPE SIZE	A	B	C	D	W1	W2	W3
12mm	330±2.0	2.9±0.5	13.0+0.5/-0	23±1.0	12.4 +2/-0	18.4±0.5	12~15

Unit：mm

Carrier Tape Dimension



NOTE:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER NOT TO EXCEED 1mm IN 100mm, NONCUMULATIVE OVER 250mm.
3. MATERIAL: BLACK STATIC DISSIPATIVE PS.(POLYSTYRENE)
4. ALL DIMENSIONS ARE IN MILLIMETERS (UNLESS OTHERWISE SPECIFIED)
5. A0 AND B0 MEASURED ON A PLANE 0.3mm ABOVE THE BOTTOM OF THE POCKET
6. K0 MEASURED FROM A PLANE ON THE INSIDE BOTTOM OF THE POCKET TO THE TOP SURFACE OF THE CARRIER
7. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE
8. SURFACE RESISTIVITY
1X10E4~1X10E11 OHMS/SQ.

Direction of unreeling

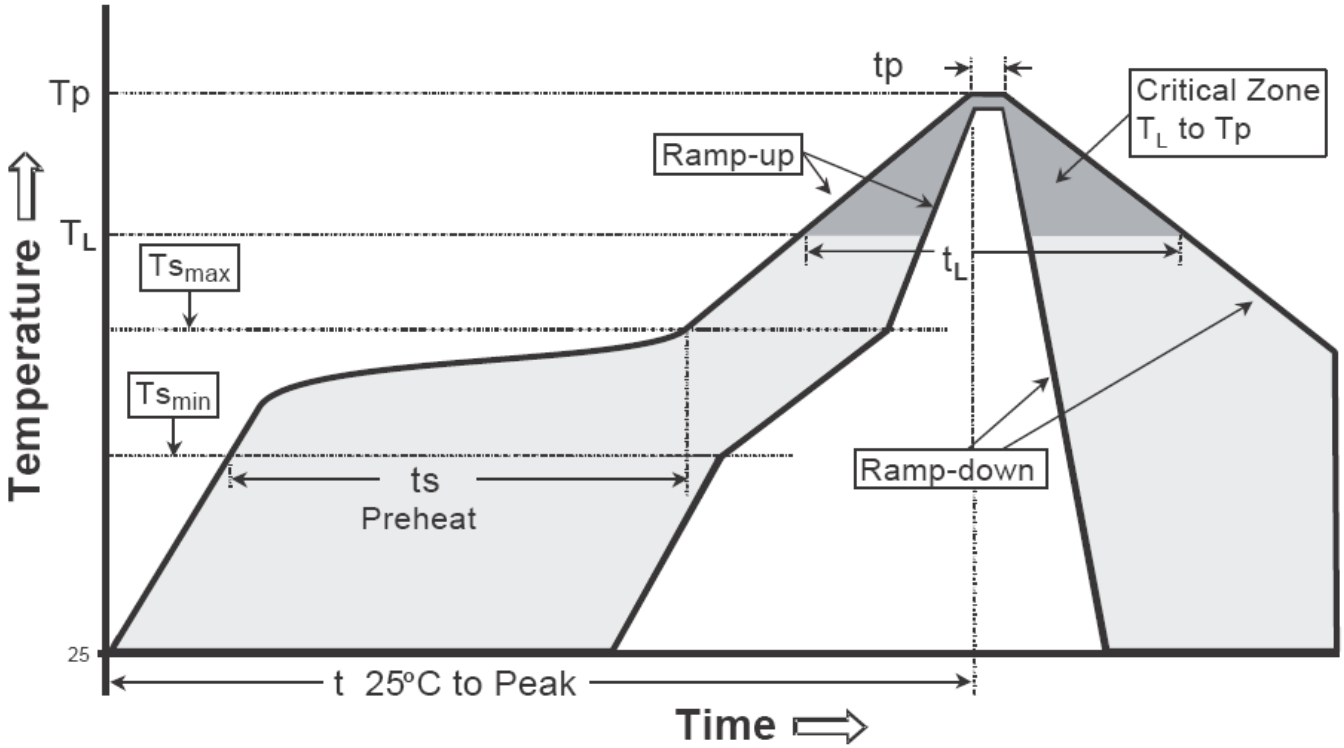
A0=6.5±0.1
B0=5.3±0.1
K0=1.4±0.1

Unit：mm

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

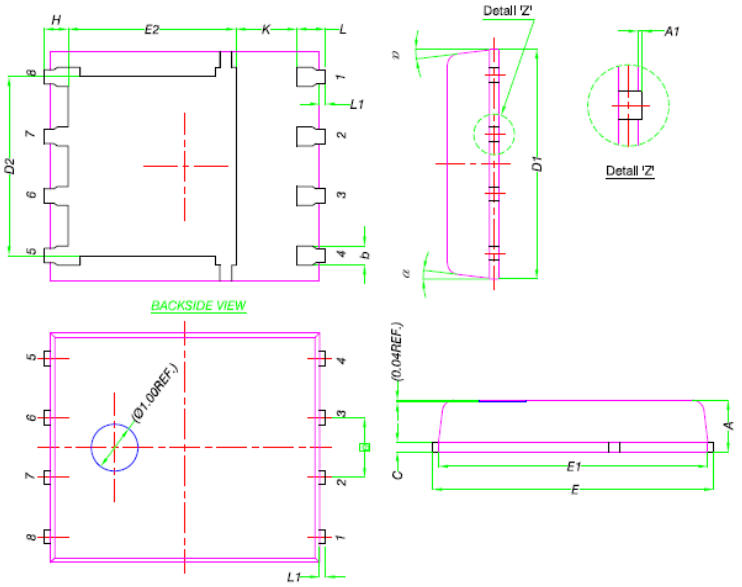
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(T_S min) −Temperature Max(T_S max) −Time($t_{s\ min}$ to $t_{s\ max}$)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: −Temperature (T_L) − Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak Temperature(T_P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

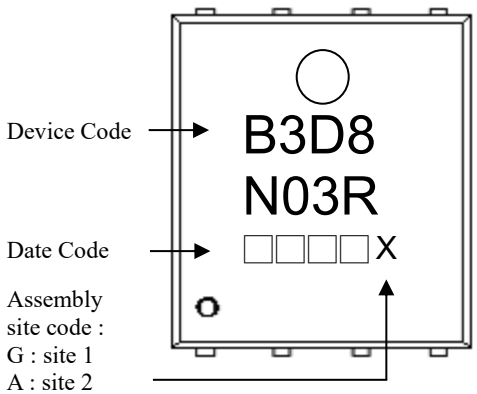
Note : All temperatures refer to topside of the package, measured on the package body surface.

DFN5×6 Dimension



8-Lead DFN5×6 Plastic Package
CYS Package Code : H8

Marking:



Date Code(counting from left to right) :
1st code: year code, the last digit of Christian year
2nd code : month code, Jan→A, Feb→B, Mar→C,
Apr→D, May→E, Jun→F, Jul→G, Aug→H,
Sep→J, Oct→K, Nov→L, Dec→M
3rd and 4th codes : production serial number, 01~99

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.90	1.10	0.035	0.043	E2	3.38	3.78	0.133	0.149
A1	0.00	0.05	0.000	0.002	e	1.27	BSC	0.050	BSC
b	0.33	0.51	0.013	0.020	H	0.41	0.61	0.016	0.024
C	0.20	0.30	0.008	0.012	K	1.10	-	0.043	-
D1	4.80	5.00	0.189	0.197	L	0.51	0.71	0.020	0.028
D2	3.61	3.96	0.142	0.156	L1	0.06	0.20	0.002	0.008
E	5.90	6.10	0.232	0.240	α	0°	12°	0°	12°
E1	5.70	5.80	0.224	0.228					

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:
- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:
- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek ***semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.***
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.