

P-Channel Enhancement Mode Power MOSFET

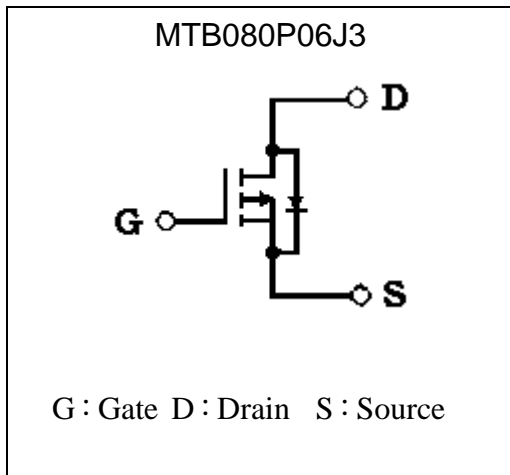
MTB080P06J3

BV_{DSS}	-60V
I_D@V_{GS}=-10V, T_C=25°C	-12.5A
R_{DS(ON)}@V_{GS}=-10V, I_D=-10A	82.5mΩ (typ)
R_{DS(ON)}@V_{GS}=-5V, I_D=-8A	107mΩ (typ)

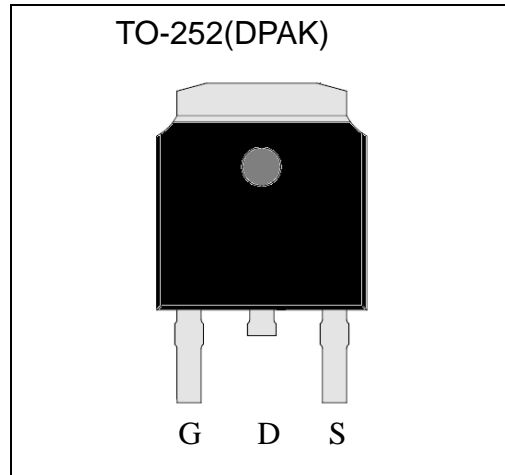
Features

- Low Gate Charge
- Simple Drive Requirement
- Pb-free Lead Plating & Halogen-free Package

Equivalent Circuit

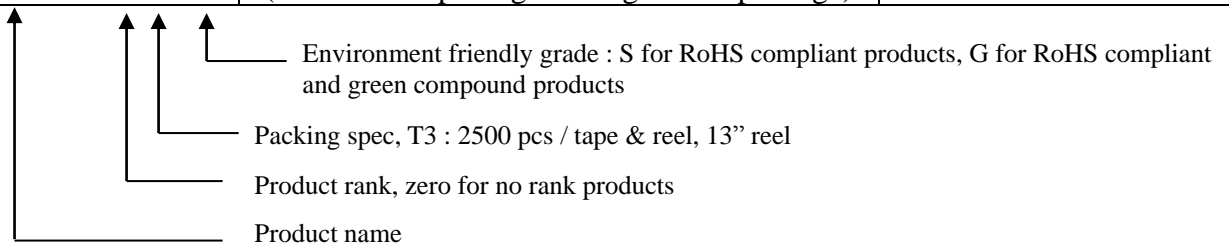


Outline



Ordering Information

Device	Package	Shipping
MTB080P06J3-0-T3-G	TO-252 (Pb-free lead plating & halogen-free package)	2500 pcs / Tape & Reel



**Absolute Maximum Ratings** ($T_C=25^{\circ}\text{C}$, unless otherwise noted)

Parameter	Symbol	Limits	Unit	
Drain-Source Voltage	V_{DS}	-60	V	
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current @ $T_C=25^{\circ}\text{C}$, $V_{GS}=-10\text{V}$	I_D	-12.5	A	
Continuous Drain Current @ $T_C=100^{\circ}\text{C}$, $V_{GS}=-10\text{V}$		-7.9		
Continuous Drain Current @ $T_A=25^{\circ}\text{C}$, $V_{GS}=-10\text{V}$ (Note 2)	I_{DSM}	-3.5		
Continuous Drain Current @ $T_A=70^{\circ}\text{C}$, $V_{GS}=-10\text{V}$ (Note 2)		-2.8		
Pulsed Drain Current (Note 3)	I_{DM}	-45		
Avalanche Current (Note 3)	I_{AS}	-12.5		
Avalanche Energy @ $L=1\text{mH}$, $I_D=-11\text{A}$, $V_{DD}=-50\text{V}$ (Note 2)	E_{AS}	60	mJ	
Total Power Dissipation	P_D	$T_C=25^{\circ}\text{C}$ (Note 1)	31	W
		$T_C=100^{\circ}\text{C}$ (Note 1)	12	
	P_{DSM}	$T_A=25^{\circ}\text{C}$ (Note 2)	2.5	
		$T_A=70^{\circ}\text{C}$ (Note 2)	1.6	
Operating Junction and Storage Temperature Range	T_j, T_{stg}	-55~+150	$^{\circ}\text{C}$	

* 100% UIS testing in condition of $V_D=-15\text{V}$, $L=1\text{mH}$, $V_G=-10\text{V}$, $I_{AS}=-9\text{A}$, Rated $V_{DS}=-60\text{V}$

Thermal Data

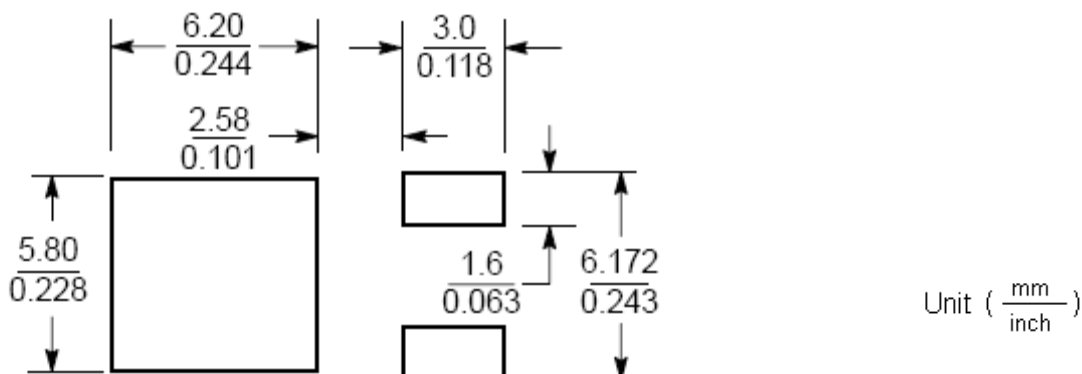
Parameter	Symbol	Typical	Maximum	Unit
Thermal Resistance, Junction-to-case	$R_{\theta JC}$	3.6	4	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-ambient, $t \leq 10\text{s}$ (Note 2)	$R_{\theta JA}$	15	18	
Thermal Resistance, Junction-to-ambient, steady state		40	50	

- Note : 1. The power dissipation P_D is based on $T_{J(MAX)}=150^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
2. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2 oz. copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.
3. Pulse width limited by junction temperature $T_{J(MAX)}=150^{\circ}\text{C}$. Ratings are based on low frequency and low duty cycles to keep initial $T_J=25^{\circ}\text{C}$.

Characteristics (Tc=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	-60	-	-	V	V _{GS} =0V, I _D =-250μA
V _{GS(th)}	-1.0	-	-2.5		V _{DS} =V _{GS} , I _D =-250μA
I _{GSS}	-	-	±100	nA	V _{GS} =±20V, V _{DS} =0V
I _{DSS}	-	-	-1	μA	V _{DS} =-48V, V _{GS} =0V
	-	-	-25		V _{DS} =-48V, V _{GS} =0V, T _J =85°C
R _{DS(ON)} *1	-	82.5	115	mΩ	V _{GS} =-10V, I _D =-10A
	-	104	150		V _{GS} =-5V, I _D =-8A
G _{FS} *1	-	11.5	-	S	V _{DS} =-10V, I _D =-10A
Dynamic					
Q _g *1, 2	-	11.5	17.5	nC	I _D =-10A, V _{DS} =-48V, V _{GS} =-10V
Q _{gs} *1, 2	-	2.4	-		
Q _{gd} *1, 2	-	2.9	-		
t _{d(ON)} *1, 2	-	6.6	9.9	ns	V _{DS} =-30V, I _D =-10A, V _{GS} =-10V, R _G =3Ω
t _r *1, 2	-	17.4	26.1		
t _{d(OFF)} *1, 2	-	26.2	39.3		
t _f *1, 2	-	7.6	11.4		
C _{iss}	-	542	-	pF	V _{GS} =0V, V _{DS} =-25V, f=1MHz
C _{oss}	-	57	-		
C _{rss}	-	40	-		
R _g	-	5.3	-	Ω	f=1MHz
Source-Drain Diode Ratings and Characteristics					
I _S *1	-	-	-12.5	A	
I _{SM} *1	-	-	-45		
V _{SD} *1	-	-0.97	-1.2	V	I _S =-10A, V _{GS} =0V
t _{rr}	-	13	19.5	ns	I _F =-10A, dI _F /dt=100A/μs
Q _{rr}	-	9.5	-	nC	

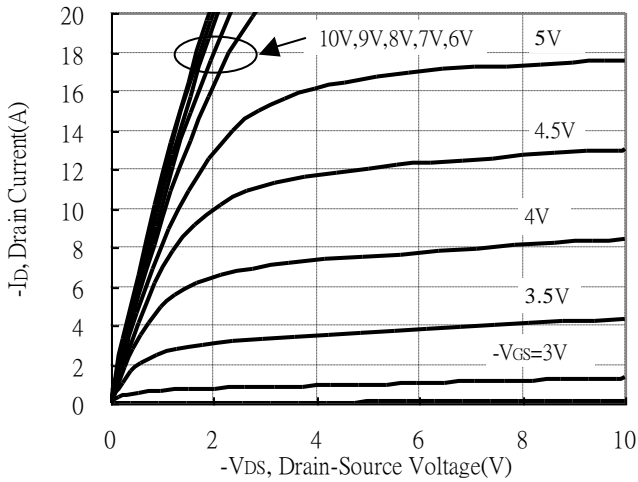
Note : *1.Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%
 *2.Independent of operating temperature
 *3.Pulse width limited by maximum junction temperature.

Recommended soldering footprint


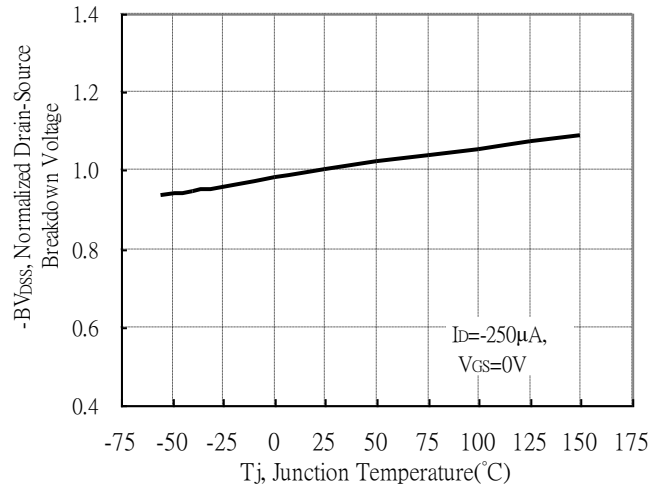


Typical Characteristics

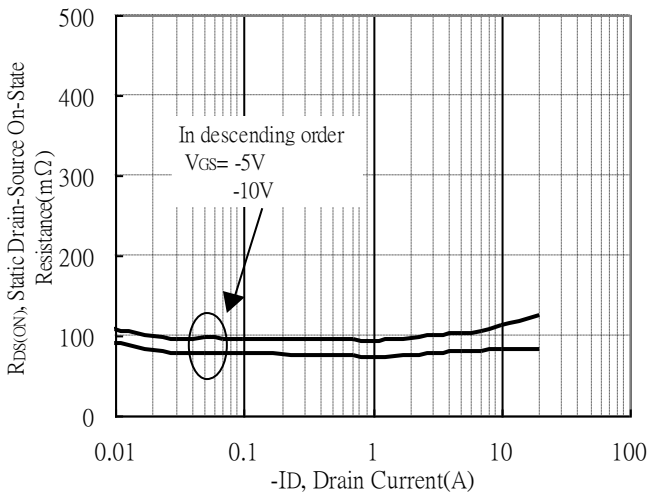
Typical Output Characteristics



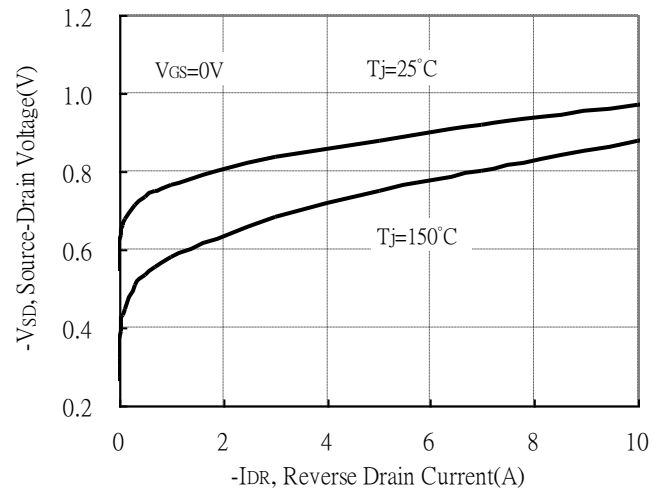
Brekdown Voltage vs Ambient Temperature



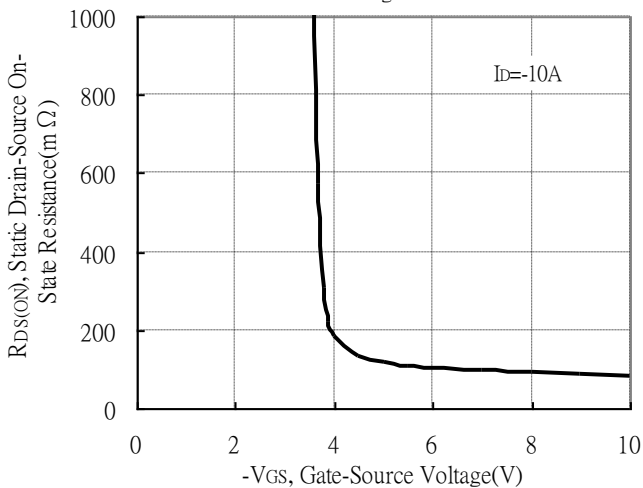
Static Drain-Source On-State resistance vs Drain Current



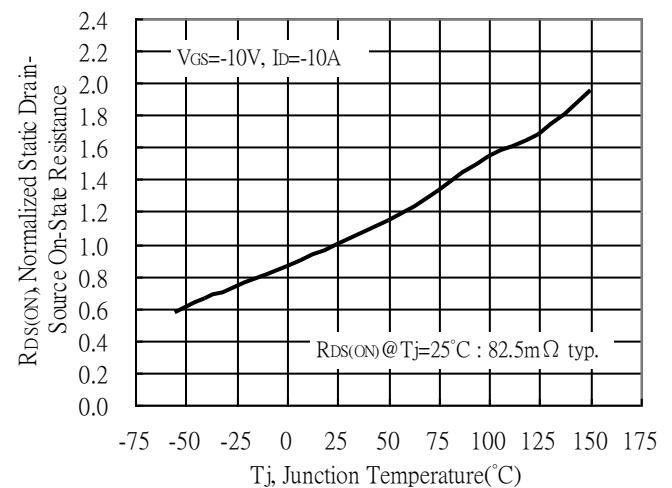
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

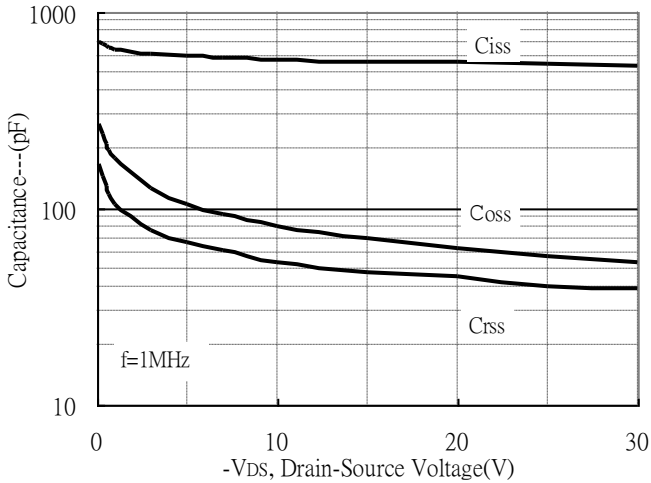


Drain-Source On-State Resistance vs Junction Temperature

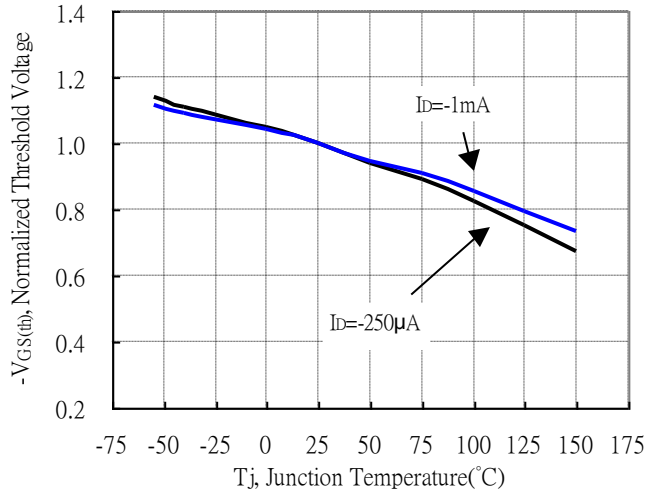


Typical Characteristics (Cont.)

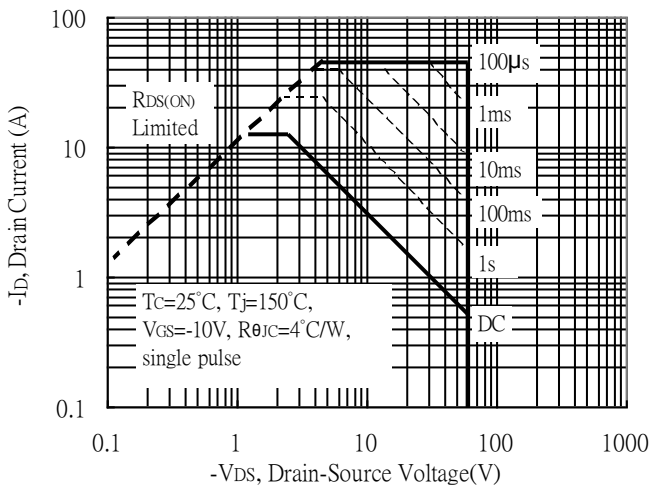
Capacitance vs Drain-to-Source Voltage



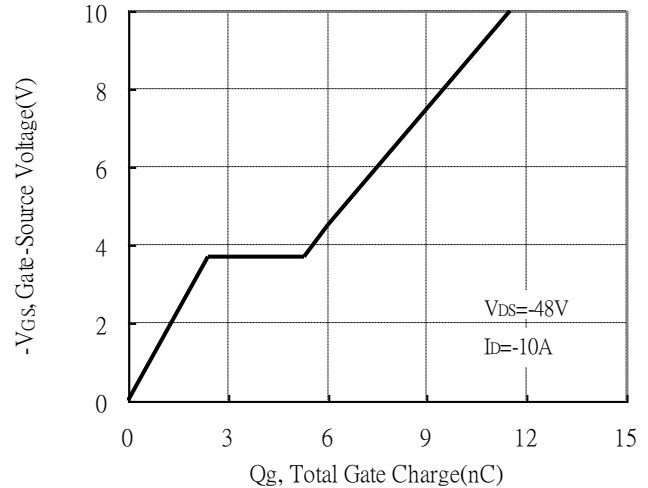
Threshold Voltage vs Junction Temperature



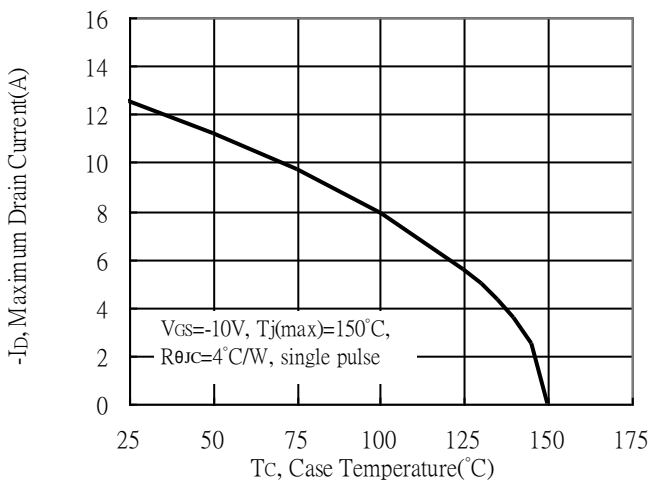
Maximum Safe Operating Area



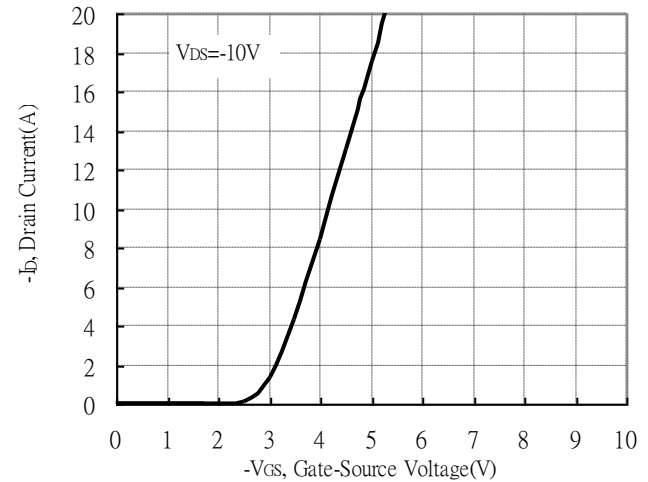
Gate Charge Characteristics



Maximum Drain Current vs Case Temperature



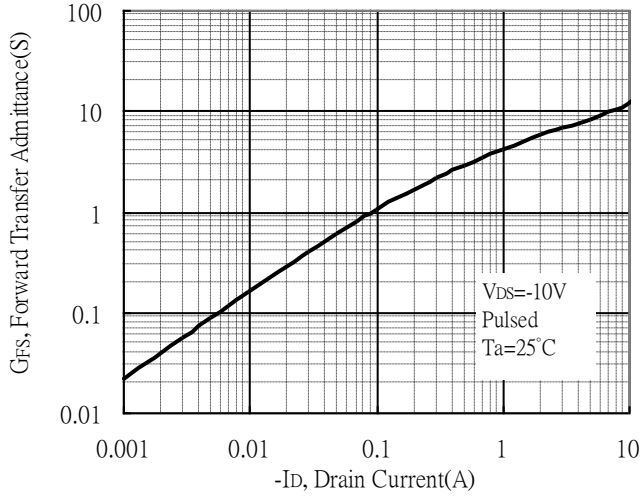
Typical Transfer Characteristics



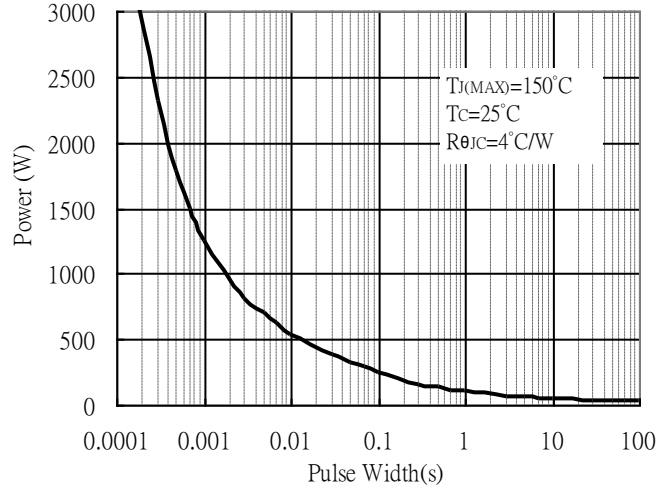


Typical Characteristics (Cont.)

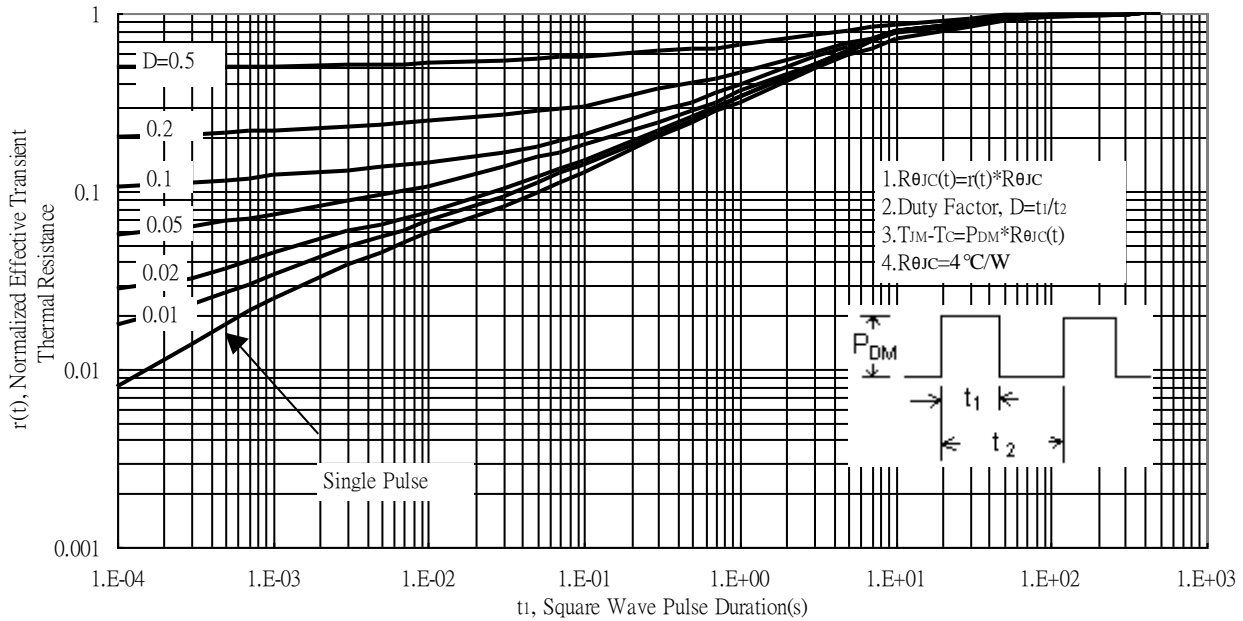
Forward Transfer Admittance vs Drain Current



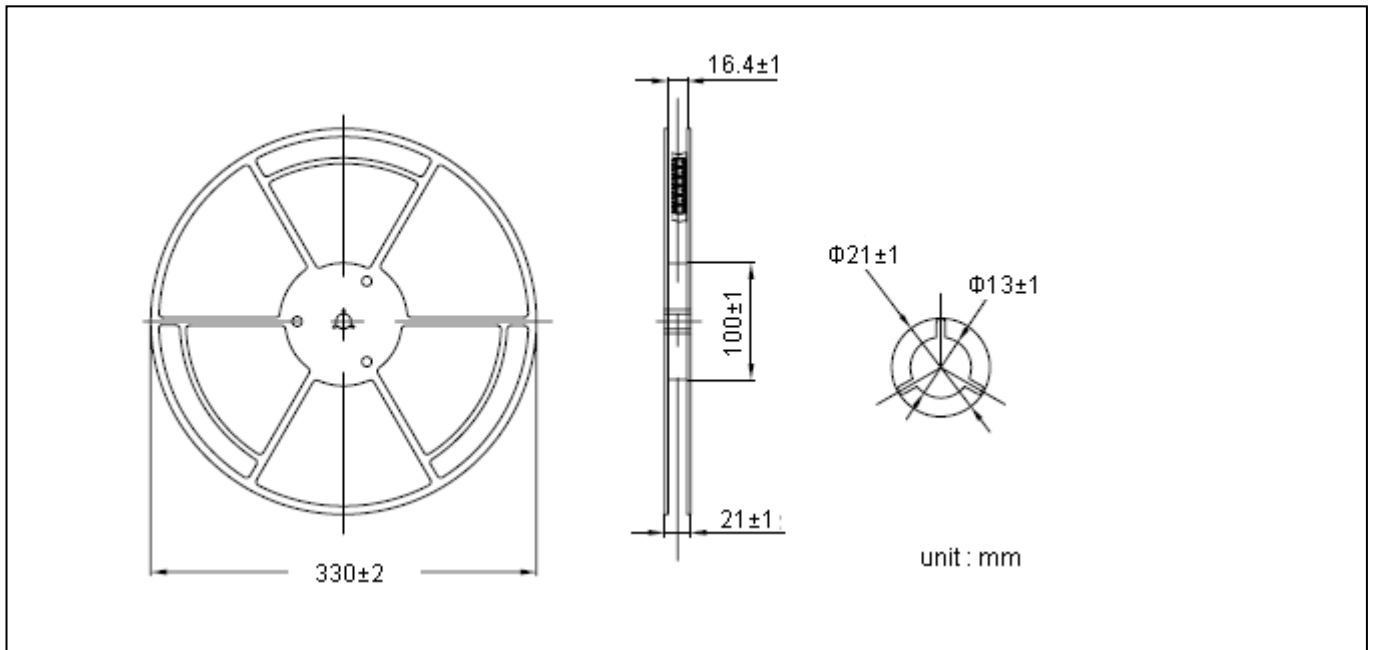
Single Pulse Power Rating, Junction to Case



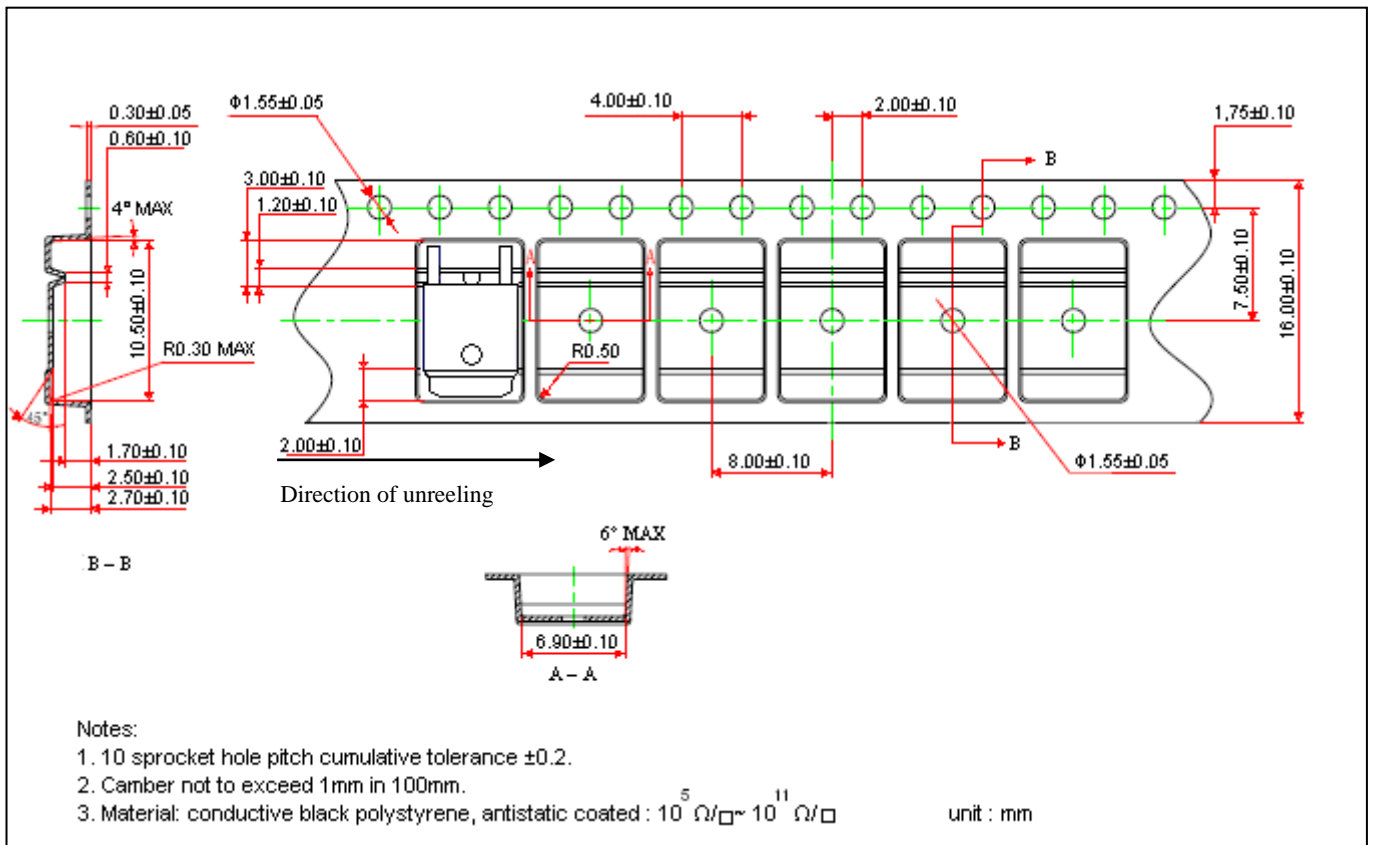
Transient Thermal Response Curves



Reel Dimension



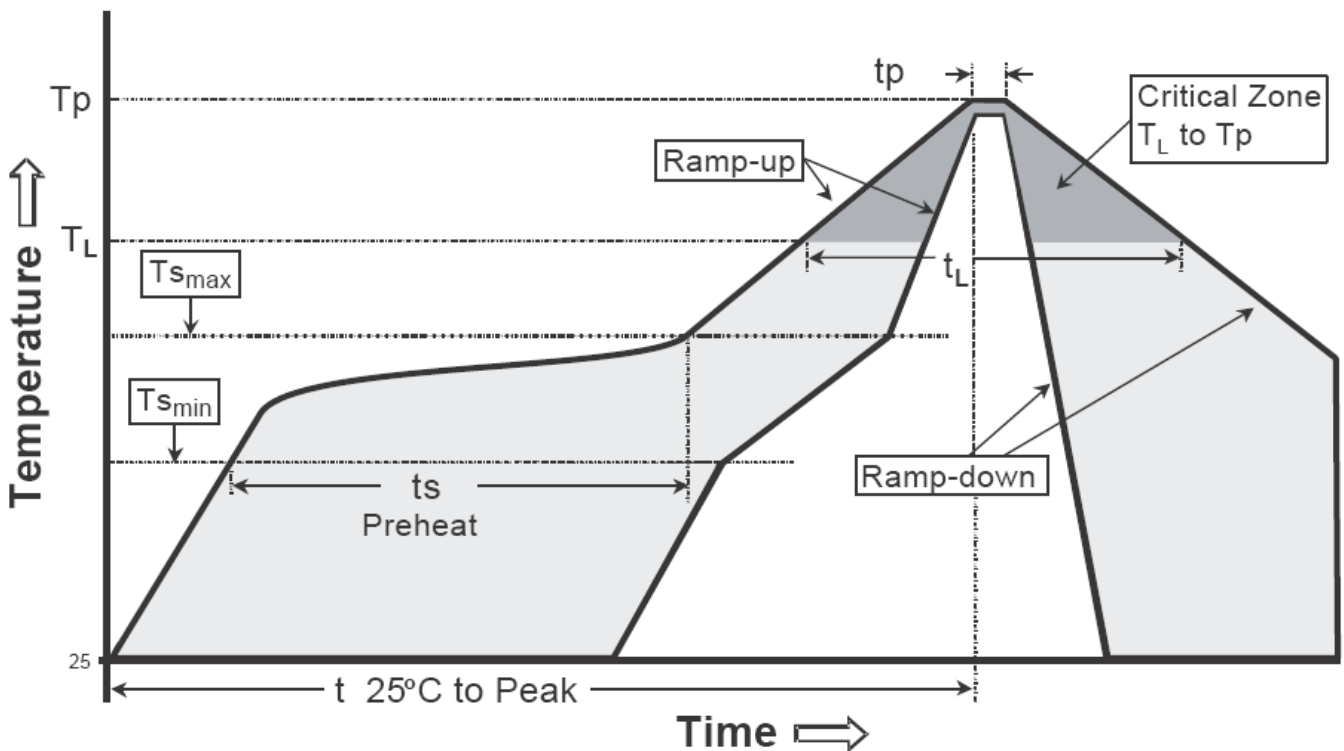
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

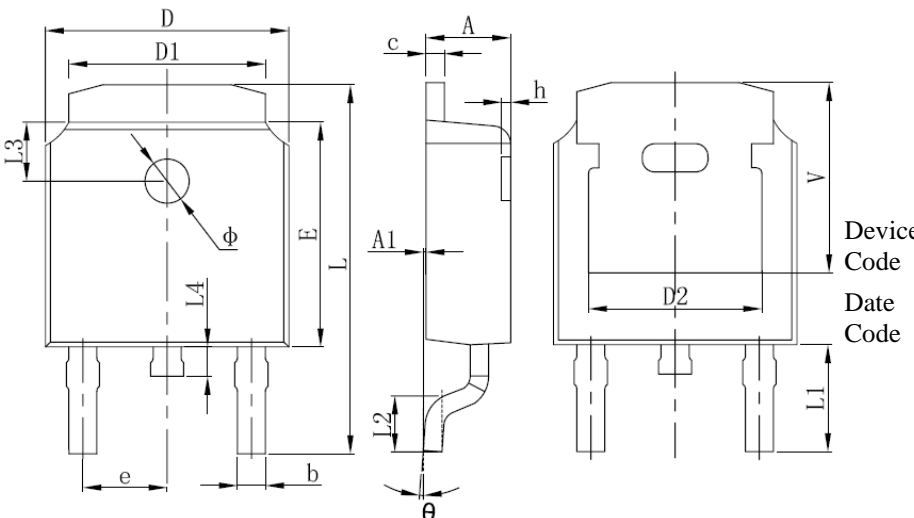
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

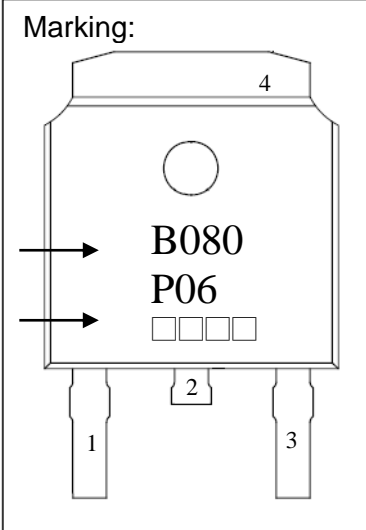
TO-252 Dimension



3-Lead TO-252 Plastic Surface Mount Package
 CYStek Package Code: J3

Date Code :
 First Code : Last digit of Christian Year
 Second Code : Month Code : Jan→A, Feb→B, Mar→C, Apr→D, May→E, Jun→F, Jul→G,
 Aug→H, Sep→J, Oct→K, Nov→L, Dec→M
 Last Two Codes : Production Serial Code, 01~99

Marking:



Device Code → B080
 Date Code → P06

Style: Pin 1.Gate 2.Drain 3.Source 4.Drain

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.087	0.094	2.200	2.400	L	0.382	0.406	9.712	10.312
A1	0.000	0.005	0.000	0.127	L1	0.114	REF	2.900	REF
b	0.025	0.030	0.635	0.770	L2	0.055	0.067	1.400	1.700
c	0.018	0.023	0.460	0.580	L3	0.063	REF	1.600	REF
D	0.256	0.264	6.500	6.700	L4	0.024	0.039	0.600	1.000
D1	0.201	0.215	5.100	5.460	Φ	0.043	0.051	1.100	1.300
D2	0.190	REF	4.830	REF	θ	0°	8°	0°	8°
E	0.236	0.244	6.000	6.200	h	0.000	0.012	0.000	0.300
e	0.086	0.094	2.186	2.386	v	0.207	REF	5.250	REF

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead : Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.