

P-Channel Enhancement Mode Power MOSFET

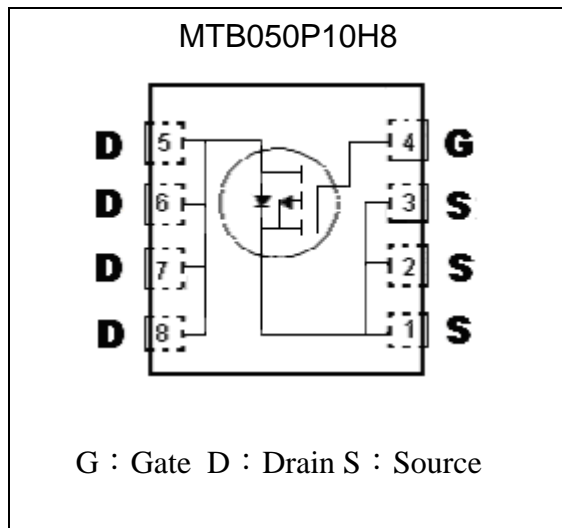
MTB050P10H8

BV _{DSS}		-100V
I _D @V _{GS} =-10V, T _C =25°C		-21.4A
I _D @V _{GS} =-10V, T _A =25°C		-4.8A
R _{DSON(TYP)}	V _{GS} =-10V, I _D =-15A	39.5mΩ
	V _{GS} =-4.5V, I _D =-12A	45.3mΩ

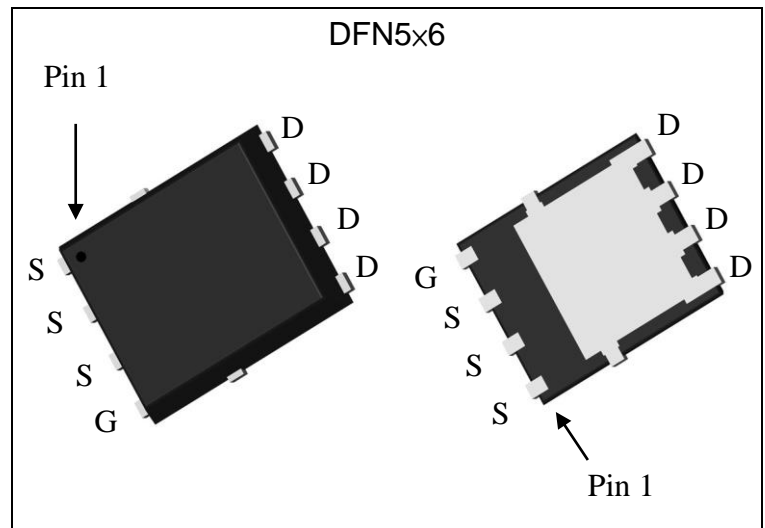
Features

- Single Drive Requirement
- Low On-resistance
- Fast Switching Characteristic
- Pb-free lead plating and Halogen-free package

Symbol

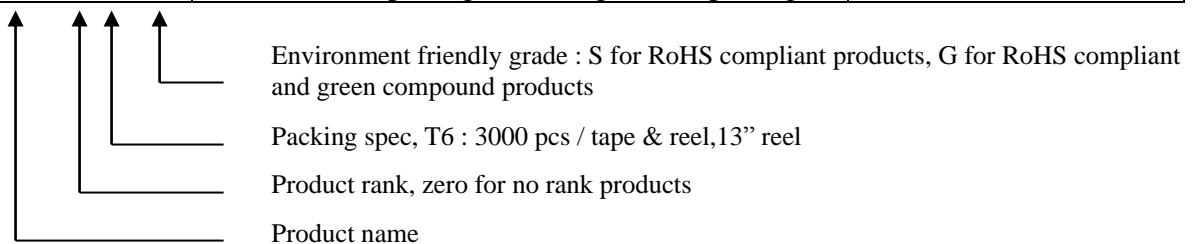


Outline



Ordering Information

Device	Package	Shipping
MTB050P10H8-0-T6-G	DFN5x6 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel





Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	10s	Steady State	Unit	
Drain-Source Voltage	V _{DS}	-100		V	
Gate-Source Voltage	V _{GS}	±20			
Continuous Drain Current @ T _C =25°C, V _{GS} =-10V (Note1)	I _D	-21.4		A	
Continuous Drain Current @ T _C =100°C, V _{GS} =-10V (Note1)		-15.1			
Continuous Drain Current @ T _A =25°C, V _{GS} =-10V (Note2)	I _{DSM}	-8.1	-4.8		
Continuous Drain Current @ T _A =70°C, V _{GS} =-10V (Note2)		-6.8	-4.0		
Pulsed Drain Current (Note3)	I _{DM}	-86			
Avalanche Current @ L=1mH (Note4)	I _{AS}	-20			
Avalanche Energy @ L=2mH, I _D =-20A, V _{DD} =-50V (Note4)	E _{AS}	400		mJ	
Total Power Dissipation	P _D	T _C =25°C (Note1)	50		W
		T _C =100°C (Note1)	25		
	P _{DSM}	T _A =25°C (Note2)	6.5	2.3	
		T _A =70°C (Note2)	4.5	1.6	
Operating Junction and Storage Temperature Range	T _j , T _{stg}	-55~+175		°C	

Thermal Data

Parameter	Symbol	Typical	Maximum	Unit
Thermal Resistance, Junction-to-case	R _{th,j-c}	2.5	3	°C/W
Thermal Resistance, Junction-to-ambient (Note2)	R _{th,j-a}	t≤10s	18	
		Steady State	50	65

- Note : 1. The power dissipation P_D is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
2. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2 oz. copper, in a still air environment with T_A=25°C. The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 175°C. The value in any given application depends on the user's specific board design.
3. Pulse width limited by junction temperature T_{J(MAX)}=175°C.
4. Ratings are based on low frequency and low duty cycles to keep initial T_J=25°C. 100% tested by conditions of L=1mH, I_{AS}=-20A, V_{GS}=-10V, V_{DD}=-50V.

Characteristics (Tc=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	-100	-	-	V	V _{GS} =0V, I _D =-250μA
V _{GS(th)}	-1	-	-2.5		V _{DS} = V _{GS} , I _D =-250μA
G _{FS} *1	-	23	-	S	V _{DS} = -15V, I _D =-10A
I _{GSS}	-	-	±100	nA	V _{GS} =±20V
I _{DSS}	-	-	-1	μA	V _{DS} = -80V, V _{GS} = 0V
	-	-	-10		V _{DS} = -80V, V _{GS} = 0, T _j =70°C
R _{DS(ON)} *1	-	39.5	50	mΩ	V _{GS} = -10V, I _D =-15A
	-	45.3	60		V _{GS} = -4.5V, I _D =-12A



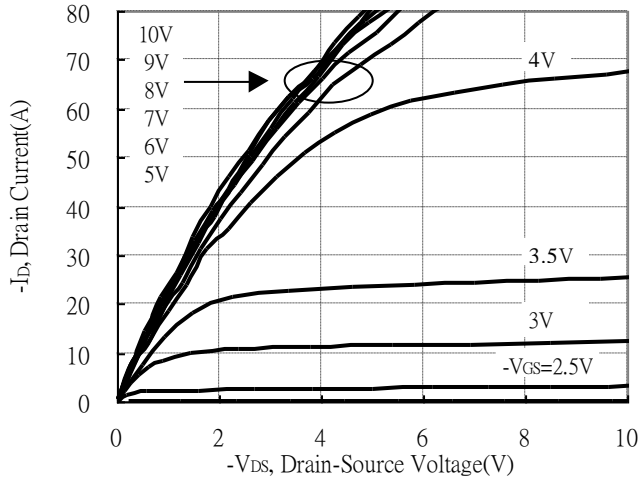
Dynamic *4					
Ciss	-	2191	-	pF	V _{DS} =-50V, V _{GS} =0V, f=1MHz
Coss	-	159	-		
Crss	-	65	-		
Qg *1, 2	-	40.7	-	nC	V _{DS} =-80V, V _{GS} =-10V, I _D =-15A
Qgs *1, 2	-	7.2	-		
Qgd *1, 2	-	4.0	-		
t _{d(ON)} *1, 2	-	13.4	-	ns	V _{DS} =-50V, I _D =-15A, V _{GS} =-10V R _G =2.7Ω
t _r *1, 2	-	23.6	-		
t _{d(OFF)} *1, 2	-	68.6	-		
t _f *1, 2	-	21.2	-		
R _g	-	4	-	Ω	f=1MHz
Source-Drain Diode					
I _S *1	-	-	-20	A	
I _{SM} *3	-	-	-80		
V _{SD} *1	-	-0.71	-1	V	I _S =-2A, V _{GS} =0V
t _{rr}	-	28.4	-	ns	I _F =-15A, dI _F /dt=100A/μs
Q _{rr}	-	40.9	-	nC	

Note : *1.Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%
 *2.Independent of operating temperature
 *3.Pulse width limited by maximum junction temperature.
 *4.Guaranteed by design, not subject to production testing.

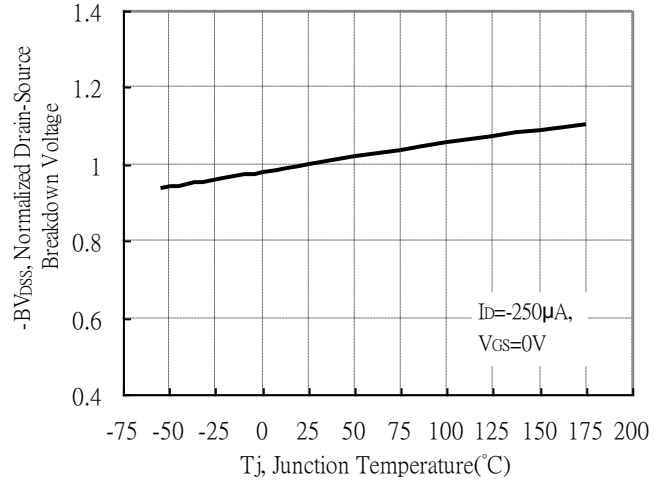


Typical Characteristics

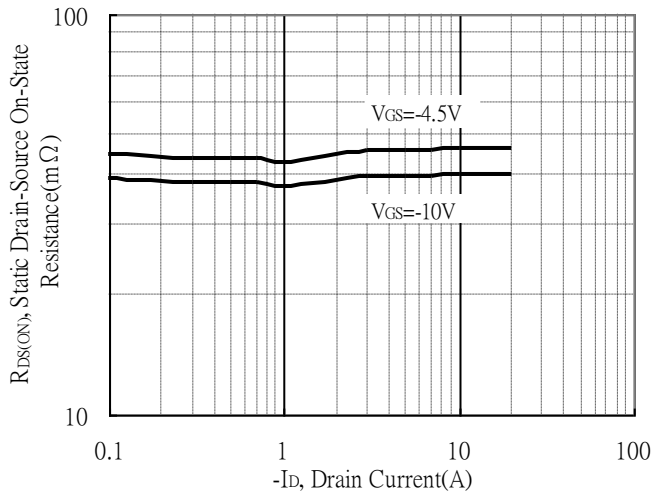
Typical Output Characteristics



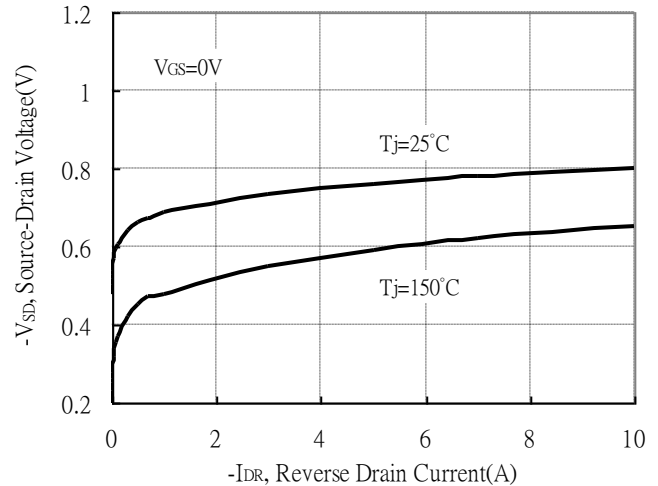
Brekdown Voltage vs Ambient Temperature



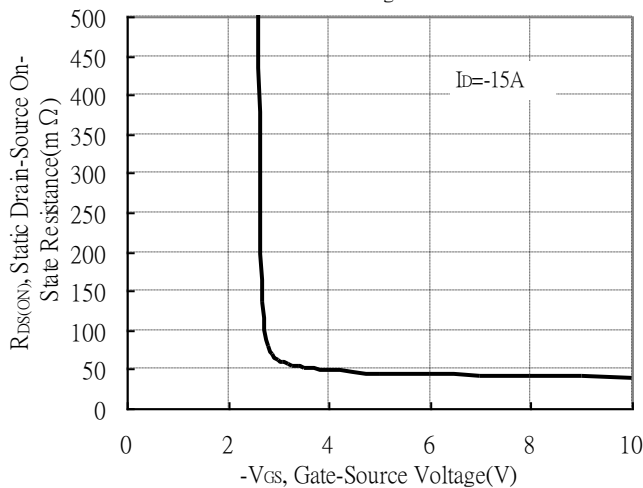
Static Drain-Source On-State resistance vs Drain Current



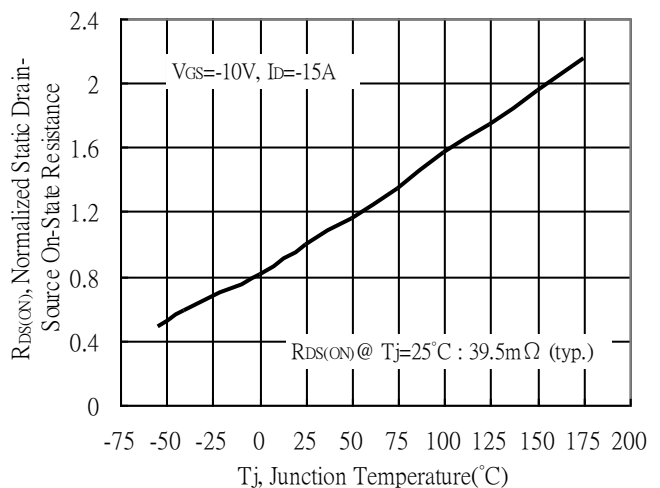
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

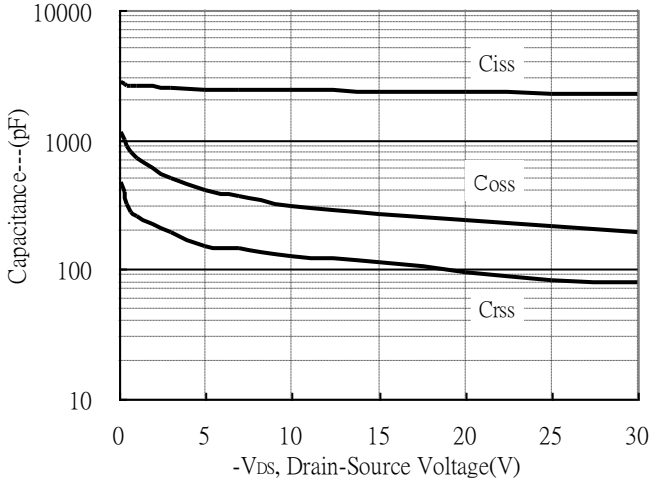


Drain-Source On-State Resistance vs Junction Temperature

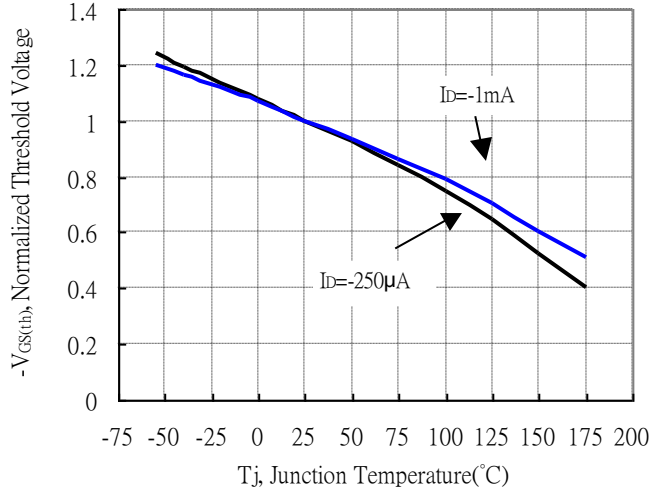


Typical Characteristics(Cont.)

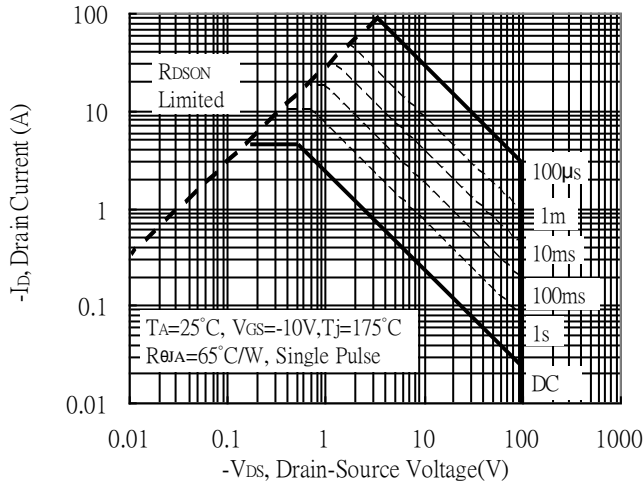
Capacitance vs Drain-to-Source Voltage



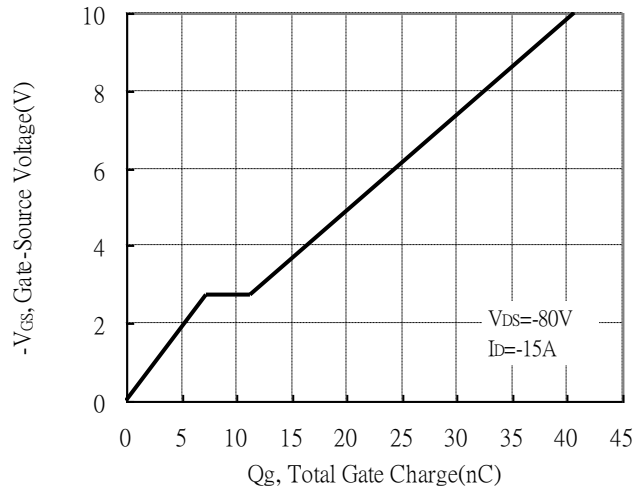
Threshold Voltage vs Junction Temperature



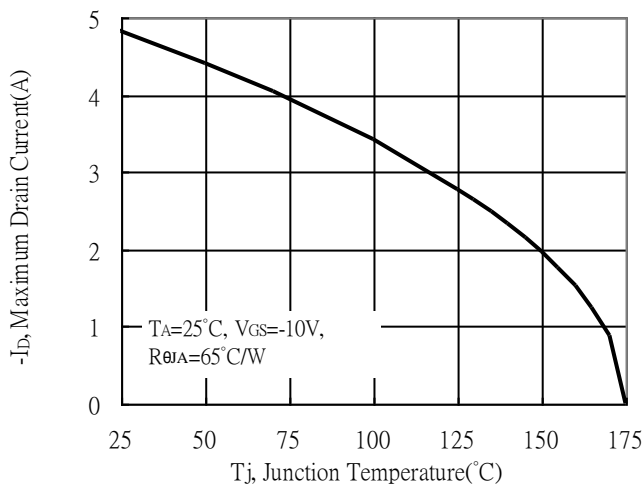
Maximum Safe Operating Area



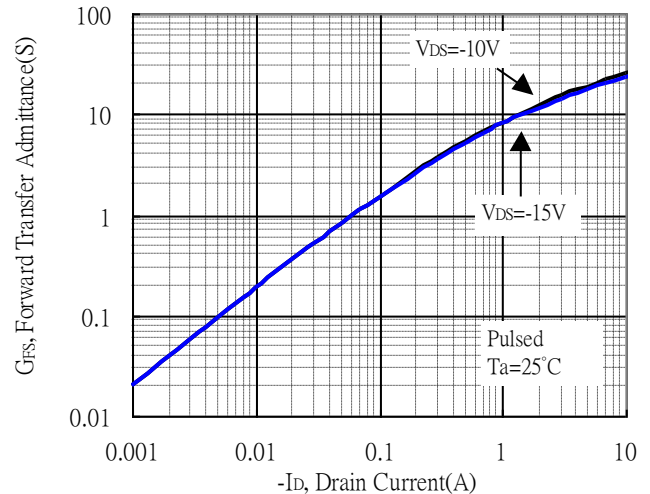
Gate Charge Characteristics



Maximum Drain Current vs Junction Temperature

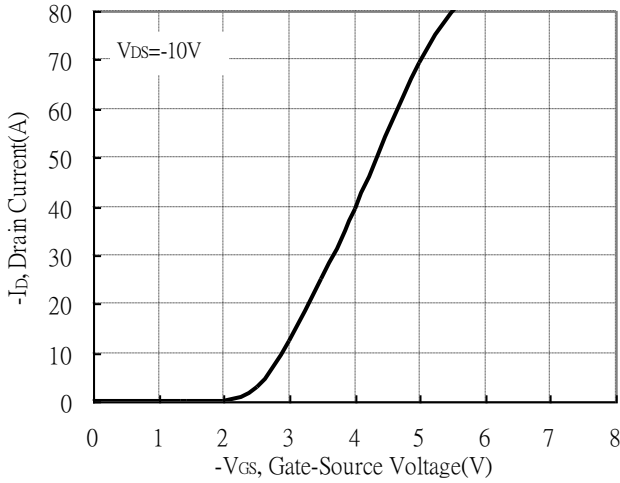


Forward Transfer Admittance vs Drain Current

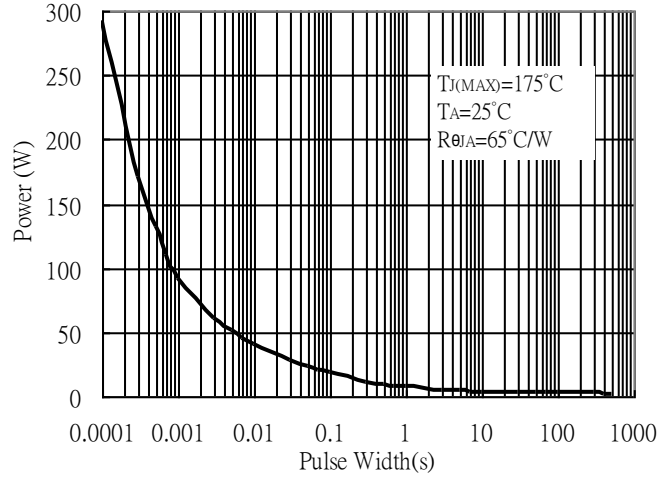


Typical Characteristics(Cont.)

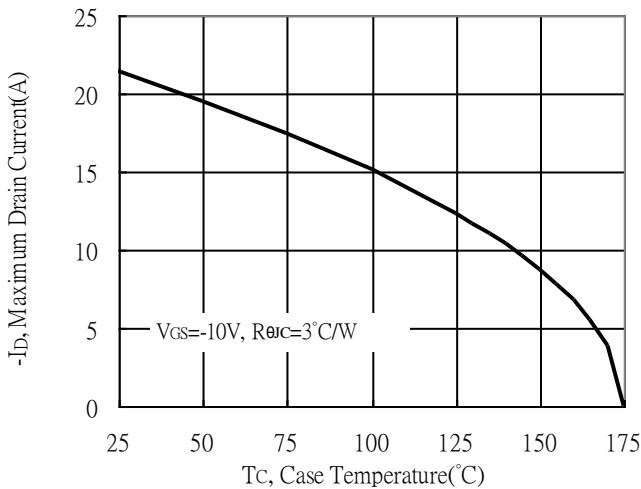
Typical Transfer Characteristics



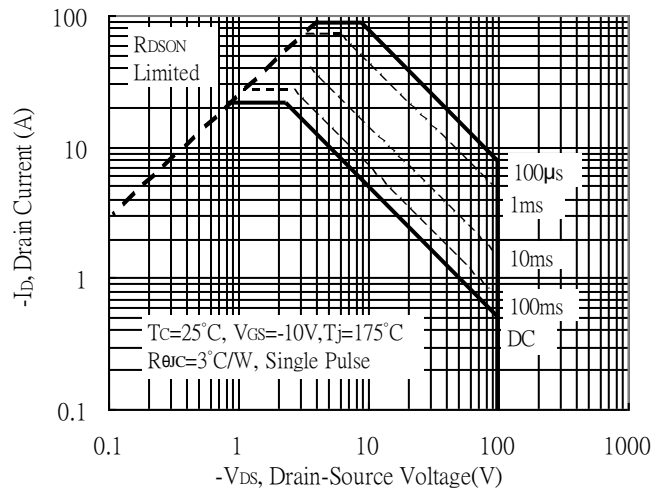
Single Pulse Maximum Power Dissipation



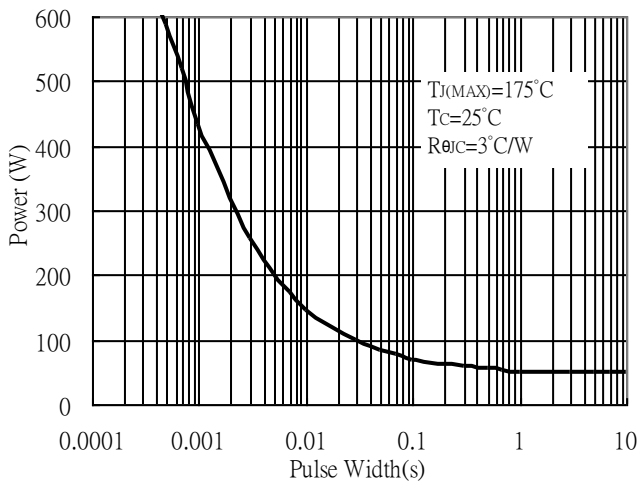
Maximum Drain Current vs Case Temperature



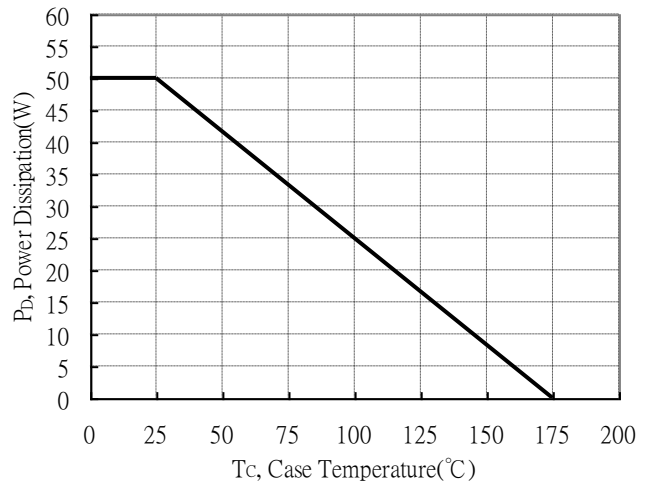
Maximum Safe Operating Area



Single Pulse Maximum Power Dissipation

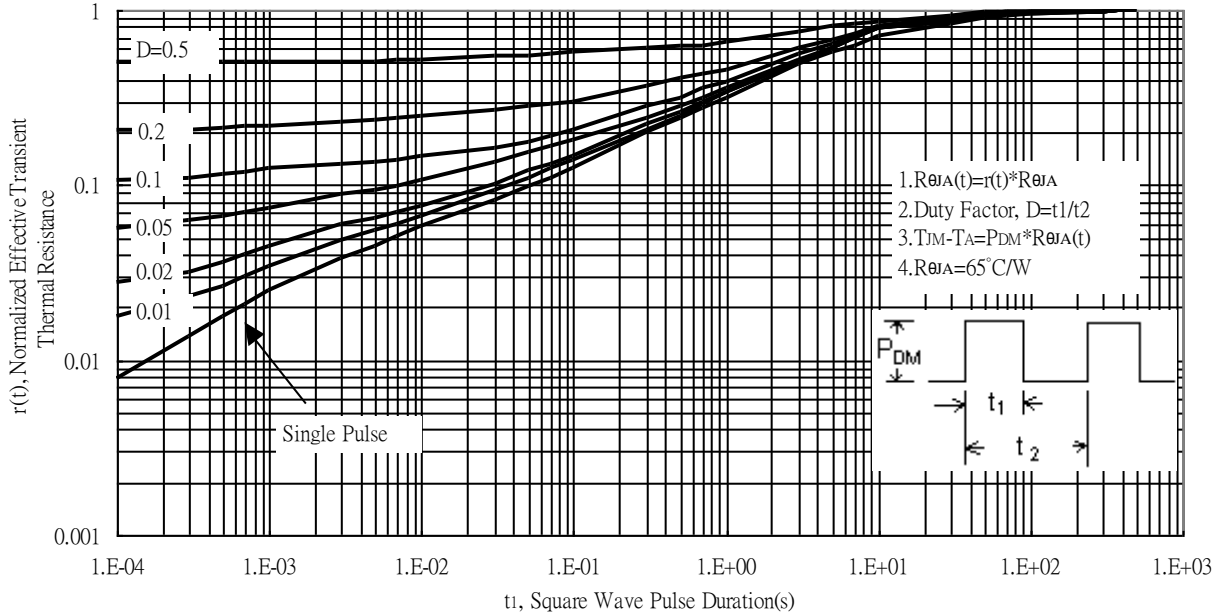


Power Derating Curve

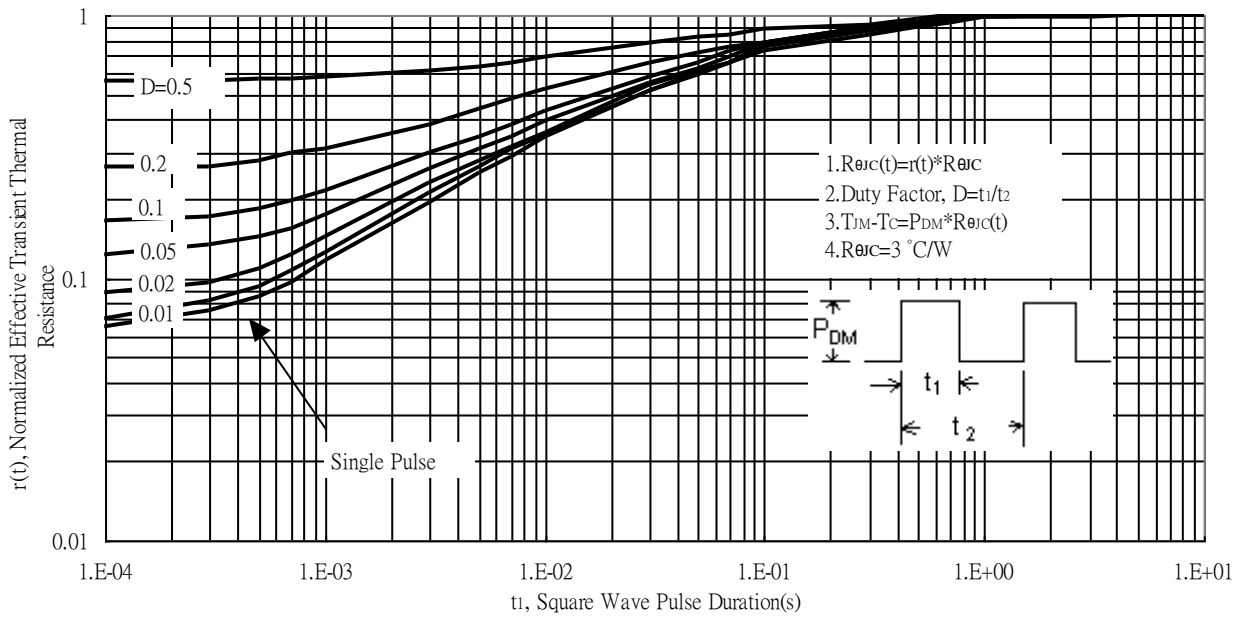


Typical Characteristics(Cont.)

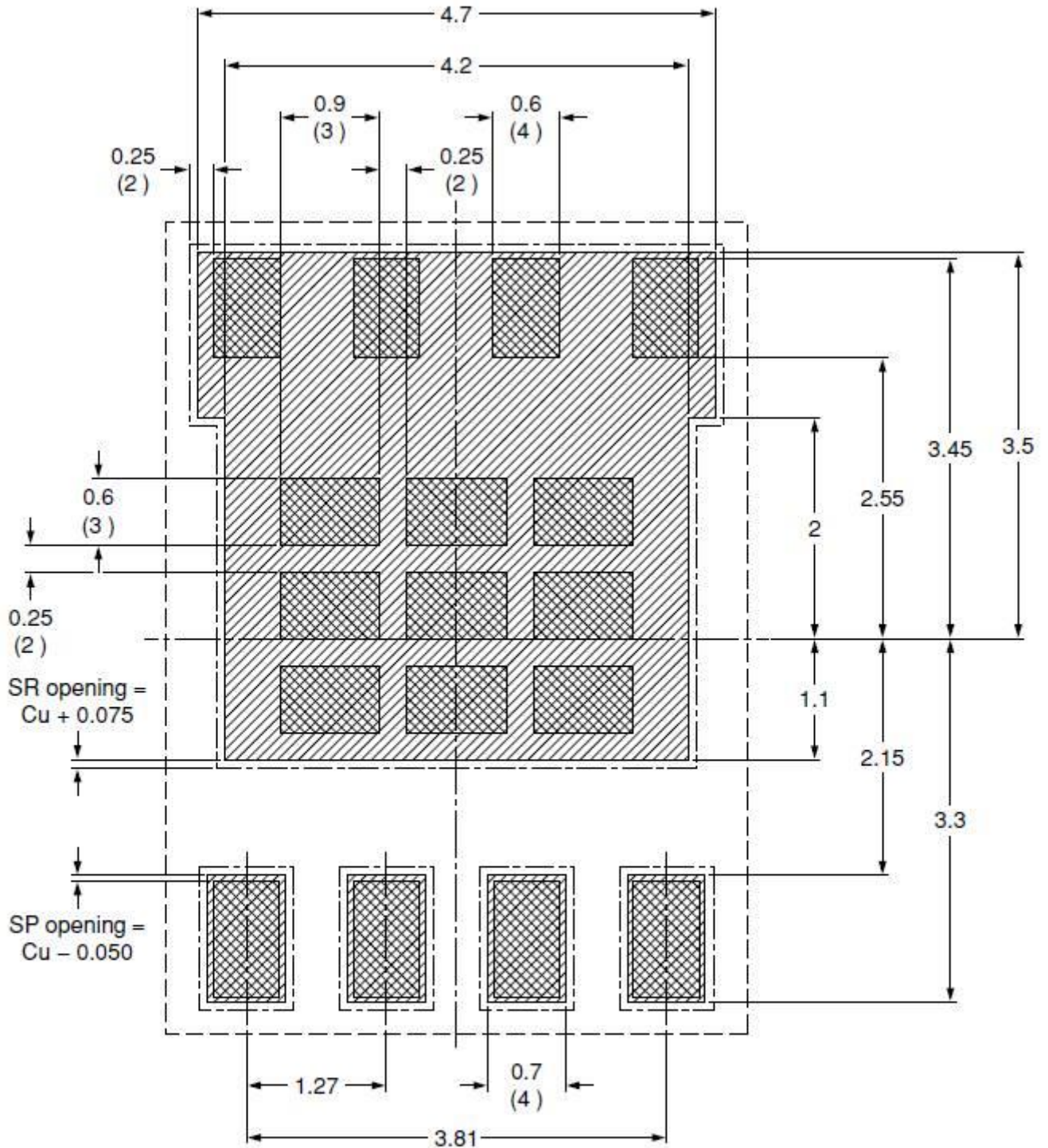
Transient Thermal Response Curves



Transient Thermal Response Curves

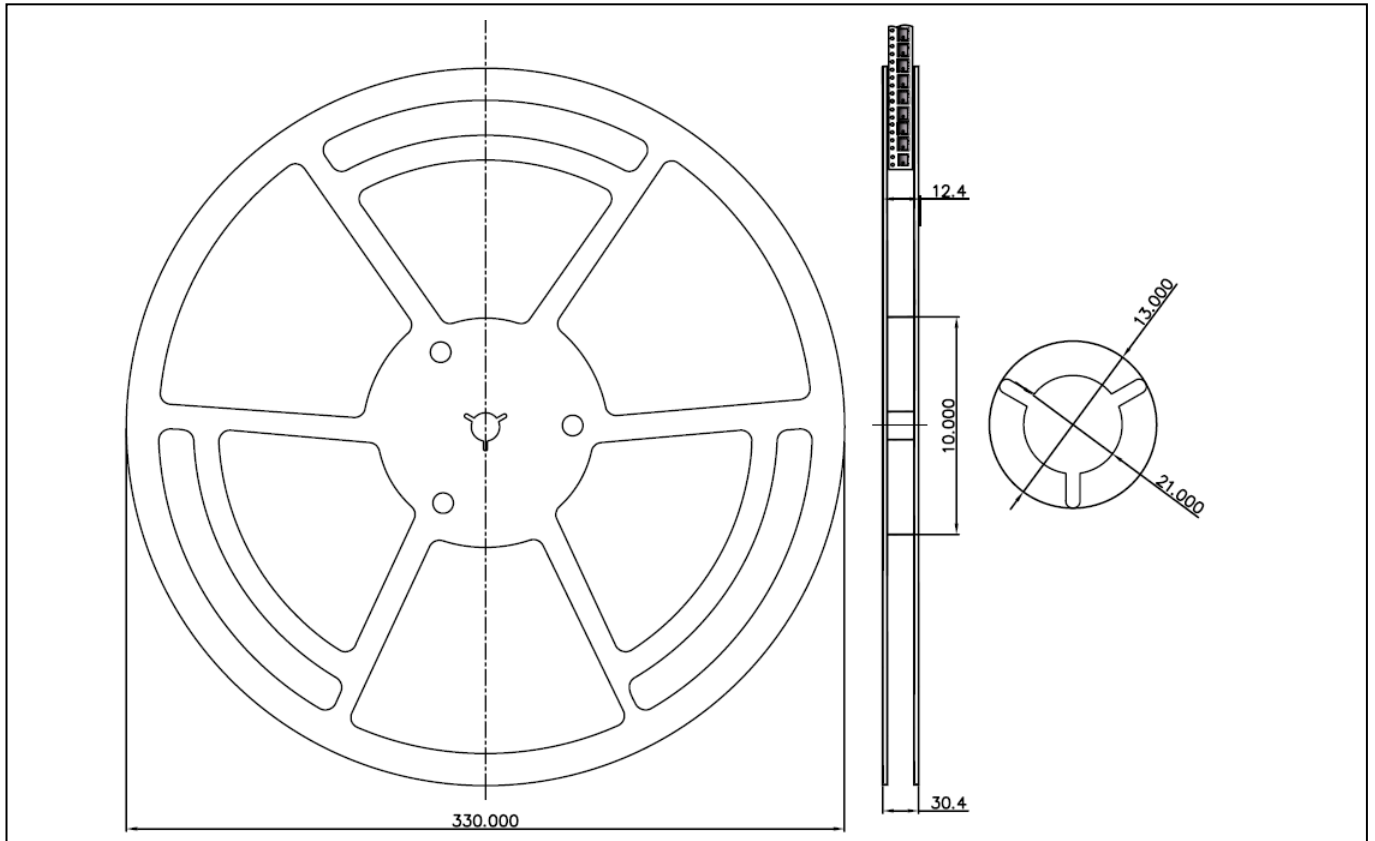


Recommended Soldering Footprint & Stencil Design

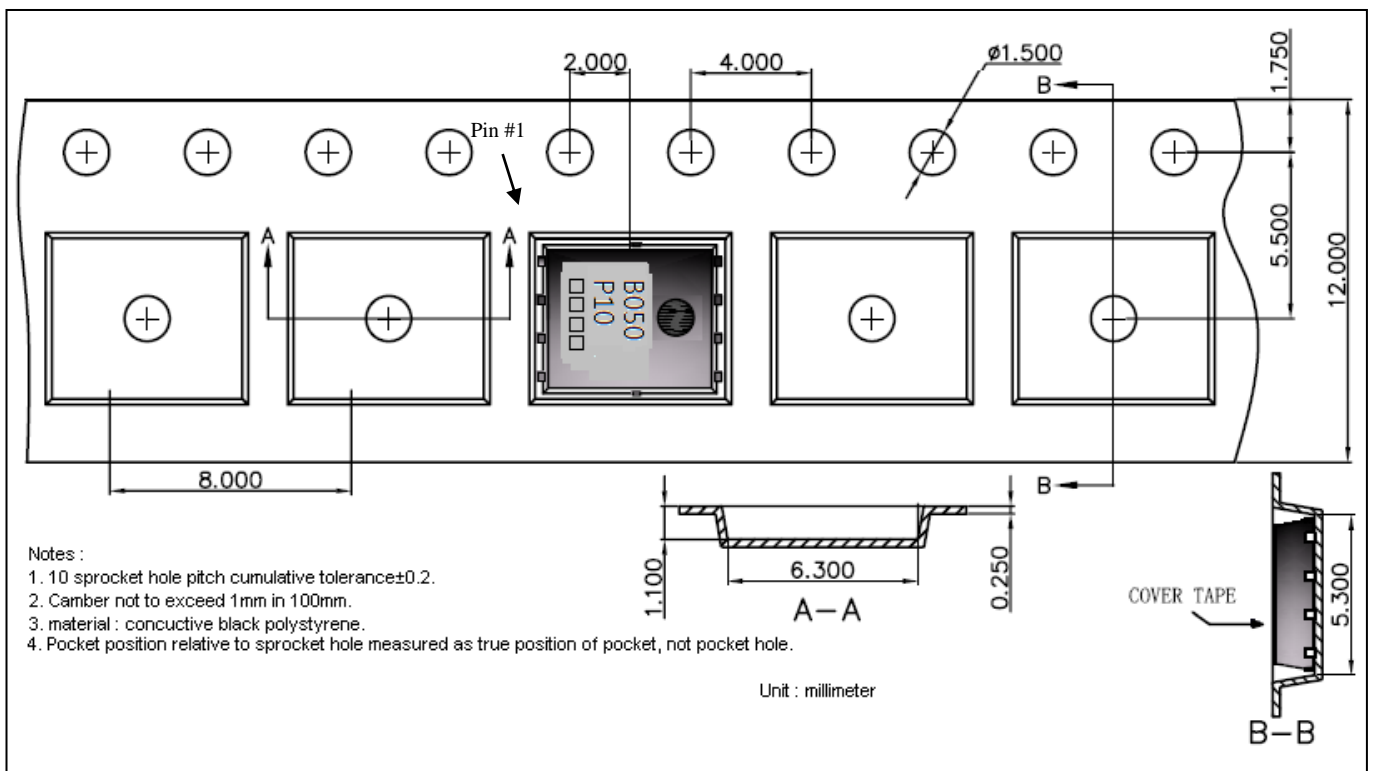


unit : mm

Reel Dimension



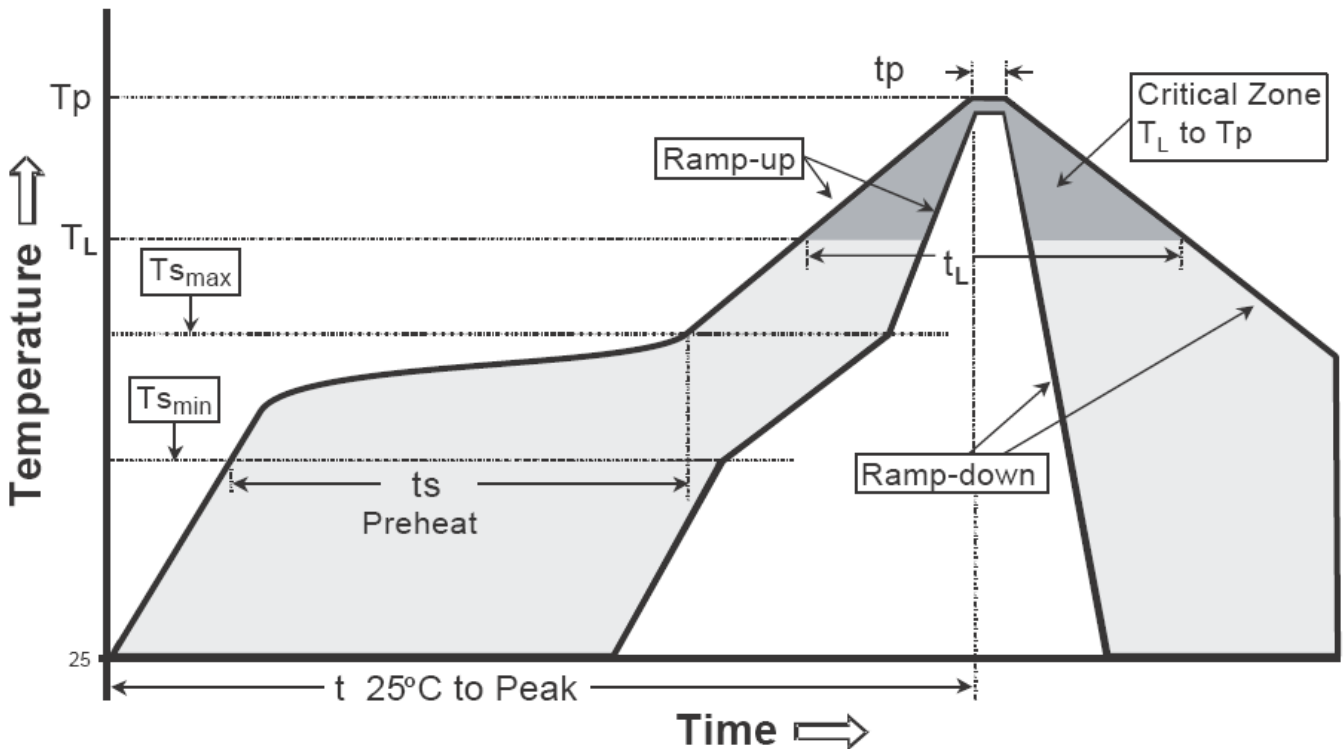
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

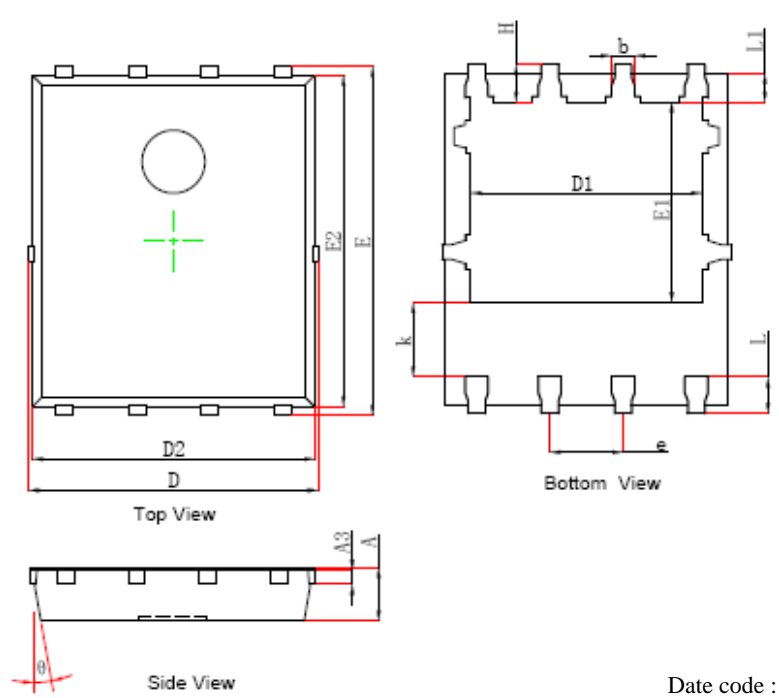
Recommended temperature profile for IR reflow



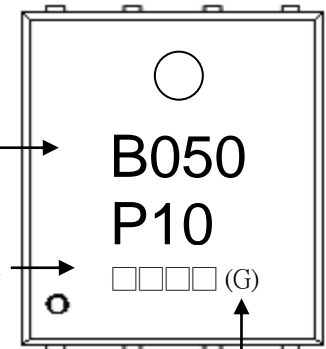
Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

DFN5x6 Dimension



Marking :



Device Name → **B050**
 P10

Date Code → □□□□ (G)

Assembly site code :
 Blank : JCET
 G : GEM

8-Lead DFN5x6 Plastic Package
 CYS Package Code : H8

Date code : (From left to right)
 First code : Year code, the last digit of Christine year.
 For example, 2017→7, 2018→8, 2019→9, ..., etc.
 Second code : Month code, Jan→A, Feb→B, Mar→C, Apr→D,
 May→E, Jun→F, Jul→G, Aug→H, Sep→J, Oct→K,
 Nov→L, Dec→M
 Third and fourth codes : production serial number, 01~99

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.900	1.100	0.035	0.043	k	1.100	-	0.043	-
A3	0.200	0.300	0.008	0.012	b	0.330	0.510	0.013	0.020
D	4.944	5.096	0.195	0.201	e	1.270 TYP.		0.050 TYP.	
E	5.900	6.126	0.232	0.241	L	0.510	0.711	0.020	0.028
D1	3.670	4.110	0.144	0.162	L1	0.310	0.576	0.012	0.023
E1	3.375	3.780	0.133	0.149	H	0.410	0.726	0.016	0.029
D2	4.800	5.000	0.189	0.197	θ	8°	12°	8°	12°
E2	5.674	5.826	0.223	0.229					

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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