

**P-Channel Enhancement Mode MOSFET**

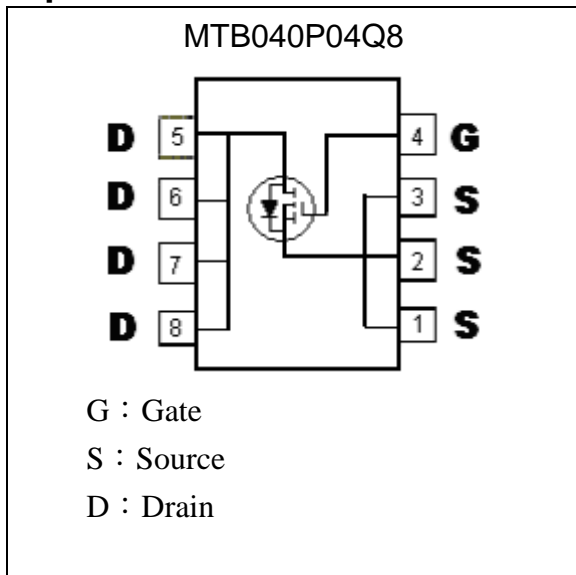
# MTB040P04Q8

BV <sub>DSS</sub>	-40V
I <sub>D</sub> @V <sub>GS</sub> =-10V, T <sub>A</sub> =25°C	-6.8A
I <sub>D</sub> @V <sub>GS</sub> =-10V, T <sub>A</sub> =70°C	-5.4A
R <sub>DSON</sub> @V <sub>GS</sub> =-10V, I <sub>D</sub> =-6A	31mΩ (typ)
R <sub>DSON</sub> @V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-5A	41mΩ (typ)

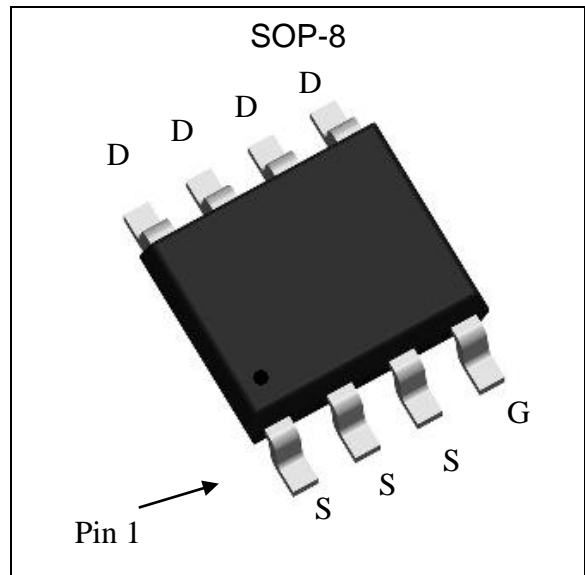
**Features**

- Simple drive requirement
- Low on-resistance
- Fast switching speed
- Pb-free lead plating and halogen-free package

**Equivalent Circuit**

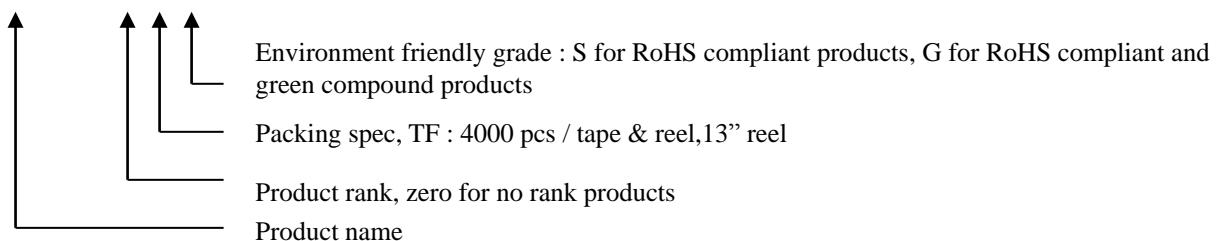


**Outline**



**Ordering Information**

Device	Package	Shipping
MTB040P04Q8-0-TF-G	SOP-8 (Pb-free lead plating and halogen-free package)	4000 pcs/ Tape & Reel





**Absolute Maximum Ratings** (Ta=25°C)

Parameter	Symbol	Limits	Unit	
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-40	V	
Gate-Source Voltage	V <sub>GS</sub>	±20		
Continuous Drain Current @ V <sub>GS</sub> =-10V, T <sub>A</sub> =25°C (Note 1)	I <sub>D</sub>	-6.8	A	
Continuous Drain Current @ V <sub>GS</sub> =-10V, T <sub>A</sub> =70°C (Note 1)		-5.4		
Pulsed Drain Current (Note 2)	I <sub>DM</sub>	-38		
Avalanche Current @ L=0.1mH	I <sub>AS</sub>	-28		
Avalanche Energy @ L=2mH, I <sub>D</sub> =-12A, V <sub>DD</sub> =-15V (Note 3)	E <sub>AS</sub>	144	mJ	
Total Power Dissipation (Note 1)	P <sub>D</sub>	T <sub>A</sub> =25 °C	3.1	W
		T <sub>A</sub> =70 °C	2	
Operating Junction and Storage Temperature	T <sub>j</sub> , T <sub>stg</sub>	-55~+150	°C	

Note : 1.Surface mounted on FR-4 board, t≤10sec.  
 2.Pulse width ≤300µs, Duty Cycle≤2%  
 3.100% tested by conditions of V<sub>DD</sub>=-15V, V<sub>GS</sub>=-10V, L=0.5mH, I<sub>AS</sub>=-12A

**Thermal Data**

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	R <sub>θJC</sub>	25	°C/W
Thermal Resistance, Junction-to-ambient, max	R <sub>θJA</sub>	40 (Note )	

Note : Surface mounted on 1 in<sup>2</sup>copper pad of FR-4 board, pulse width≤10s.

**Electrical Characteristics** (T<sub>j</sub>=25°C, unless otherwise specified)

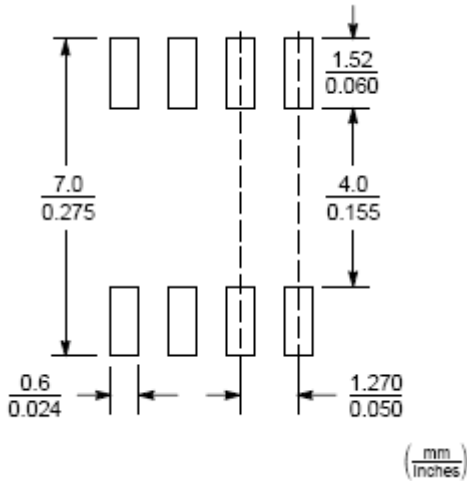
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
<b>Static</b>					
BV <sub>DSS</sub>	-40	-	-	V	V <sub>GS</sub> =0V, I <sub>D</sub> =-250µA
V <sub>GS(th)</sub>	-1	-	-2.5		V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250µA
I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V
I <sub>DSS</sub>	-	-	-1	µA	V <sub>DS</sub> =-32V, V <sub>GS</sub> =0V
	-	-	-5		V <sub>DS</sub> =-32V, V <sub>GS</sub> =0V, T <sub>j</sub> =55°C
*R <sub>DS(ON)</sub>	-	31	41	mΩ	I <sub>D</sub> =-6A, V <sub>GS</sub> =-10V
	-	41	55		I <sub>D</sub> =-5A, V <sub>GS</sub> =-4.5V
*G <sub>FS</sub>	-	8.6	-	S	V <sub>DS</sub> =-10V, I <sub>D</sub> =-5A
<b>Dynamic</b>					
C <sub>iss</sub>	-	914	-	pF	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V, f=1MHz
C <sub>oss</sub>	-	69	-		
C <sub>rss</sub>	-	56	-		
*t <sub>d(ON)</sub>	-	6.8	-	ns	V <sub>DD</sub> =-20V, I <sub>D</sub> =-6A, V <sub>GS</sub> =-10V, R <sub>G</sub> =1Ω
*t <sub>r</sub>	-	20	-		
*t <sub>d(OFF)</sub>	-	66.6	-		
*t <sub>f</sub>	-	32.8	-		



*Qg	-	19.5	-	nC	V <sub>DS</sub> =-32V, V <sub>GS</sub> =-10V, I <sub>D</sub> =-6A
*Qgs	-	2.8	-		
*Qgd	-	4.1	-		
<b>Source Drain Diode</b>					
*V <sub>SD</sub>	-	-0.85	-1.2	V	V <sub>GS</sub> =0V, I <sub>S</sub> =-6A
trr	-	9.6	-	ns	I <sub>F</sub> =-6A, dI <sub>F</sub> /dt=100A/μs
Qrr	-	5	-	nC	

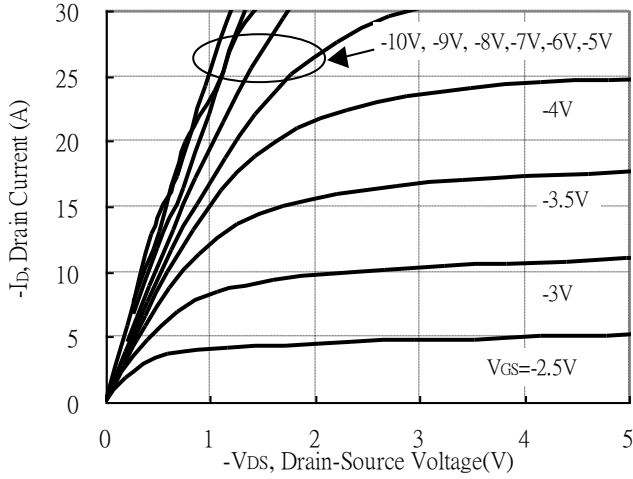
\*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

### Recommended Soldering Footprint

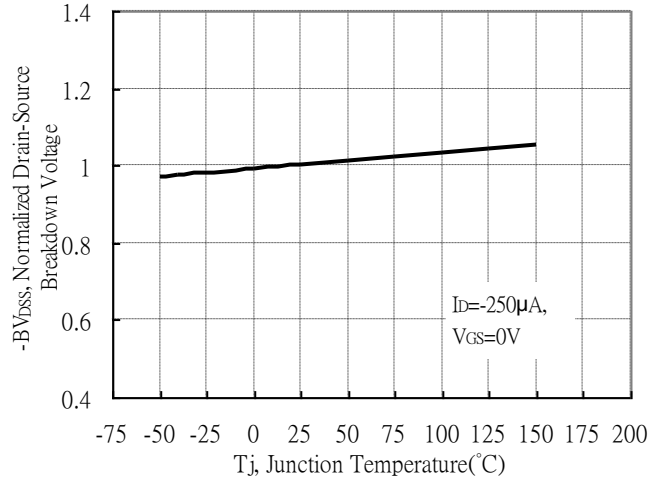


## Typical Characteristics

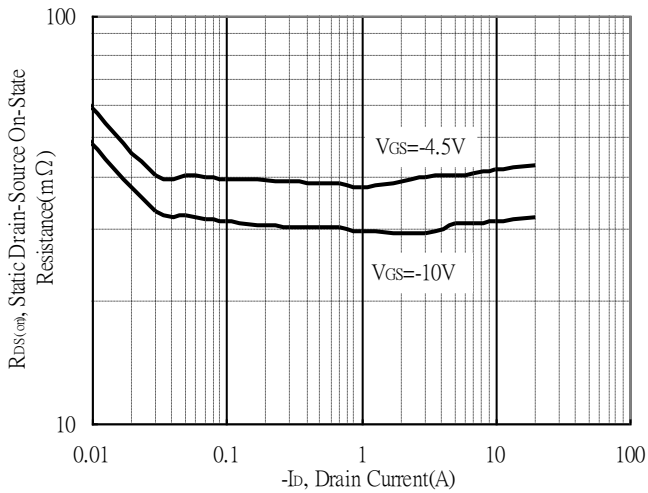
Typical Output Characteristics



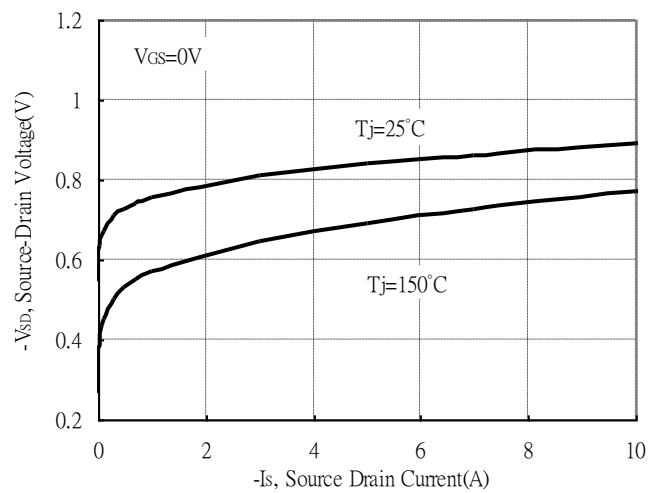
Breakdown Voltage vs Ambient Temperature



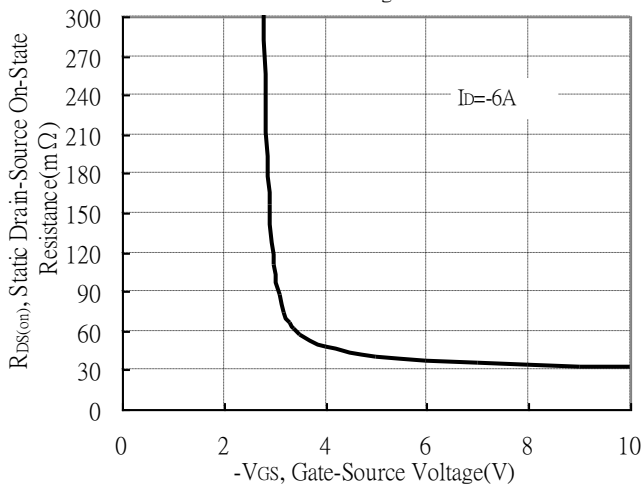
Static Drain-Source On-State resistance vs Drain Current



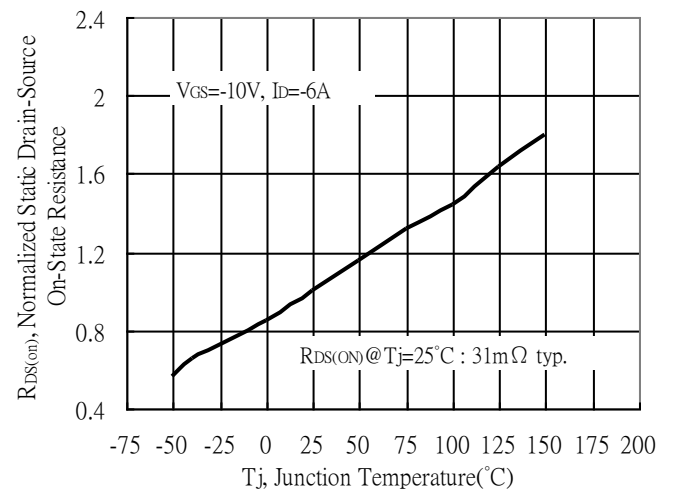
Source Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

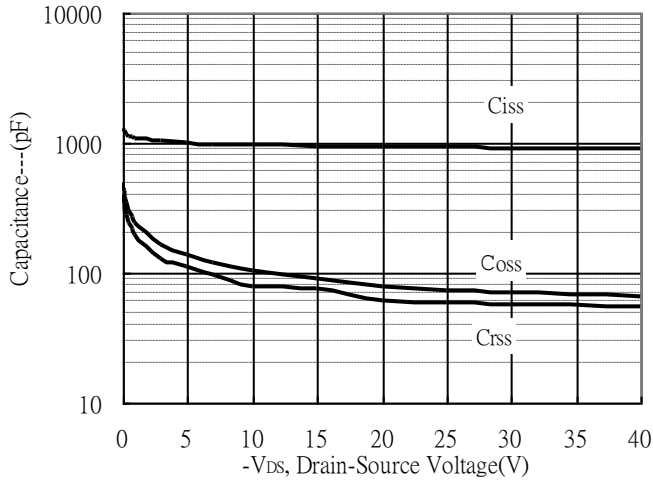


Drain-Source On-State Resistance vs Junction Temperature

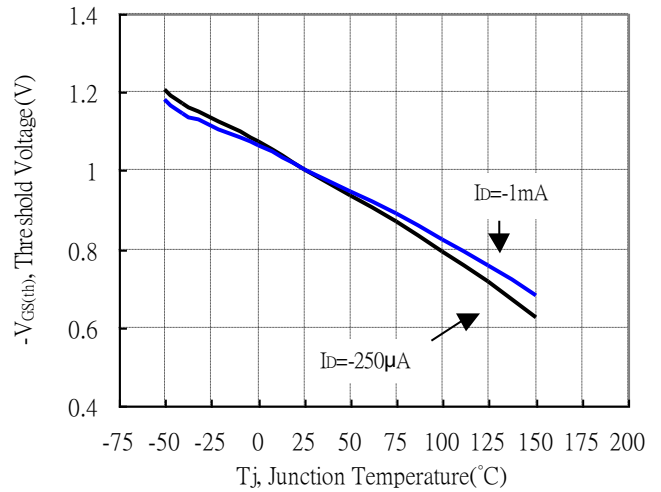


**Typical Characteristics(Cont.)**

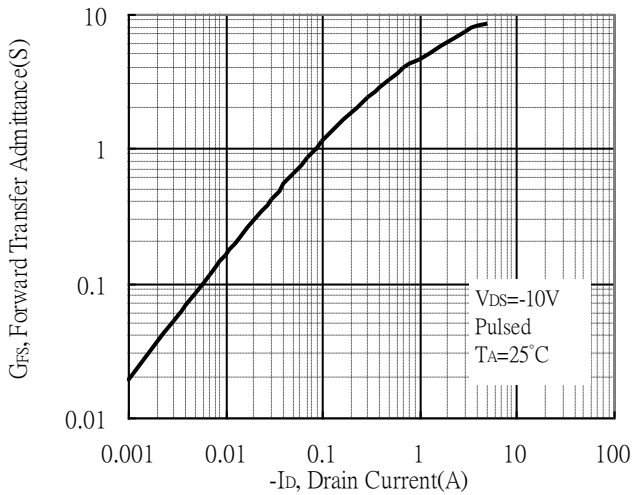
Capacitance vs Drain-to-Source Voltage



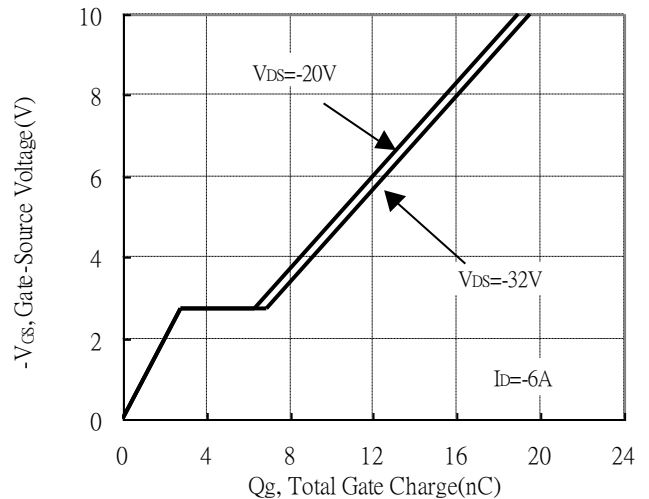
Threshold Voltage vs Junction Temperature



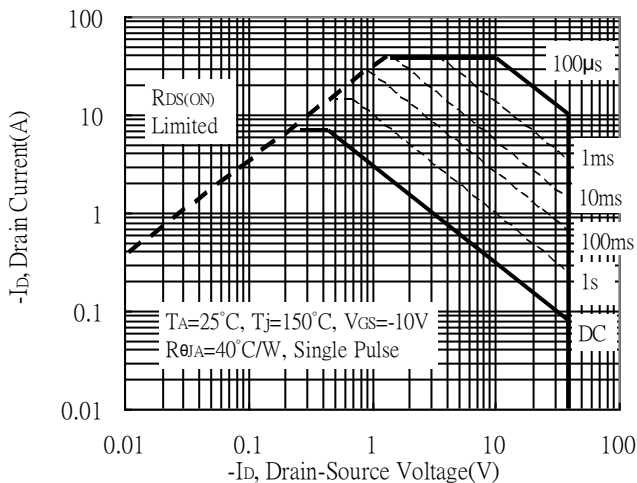
Forward Transfer Admittance vs Drain Current



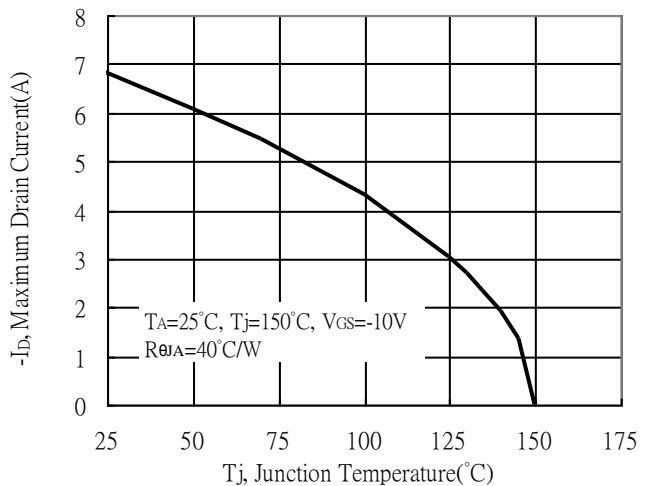
Gate Charge Characteristics



Maximum Safe Operating Area



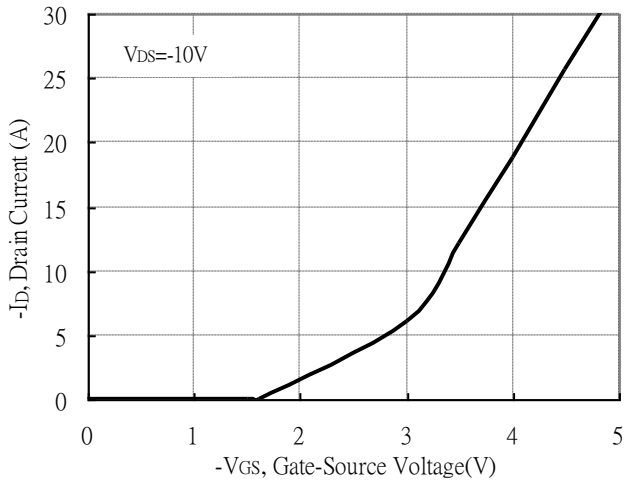
Maximum Drain Current vs Junction Temperature



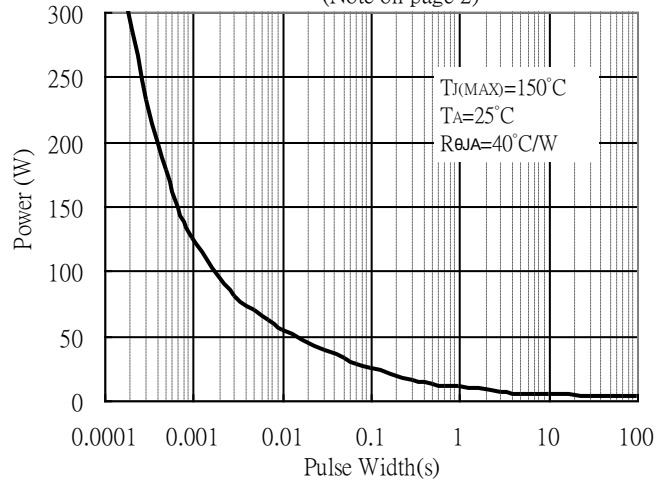


**Typical Characteristics(Cont.)**

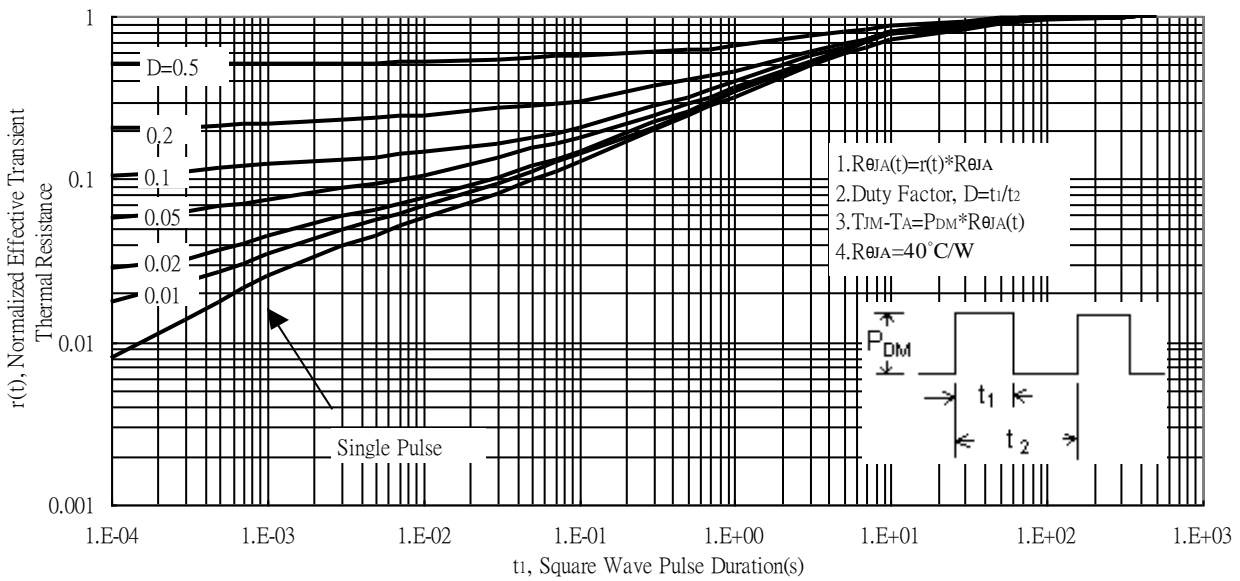
Typical Transfer Characteristics



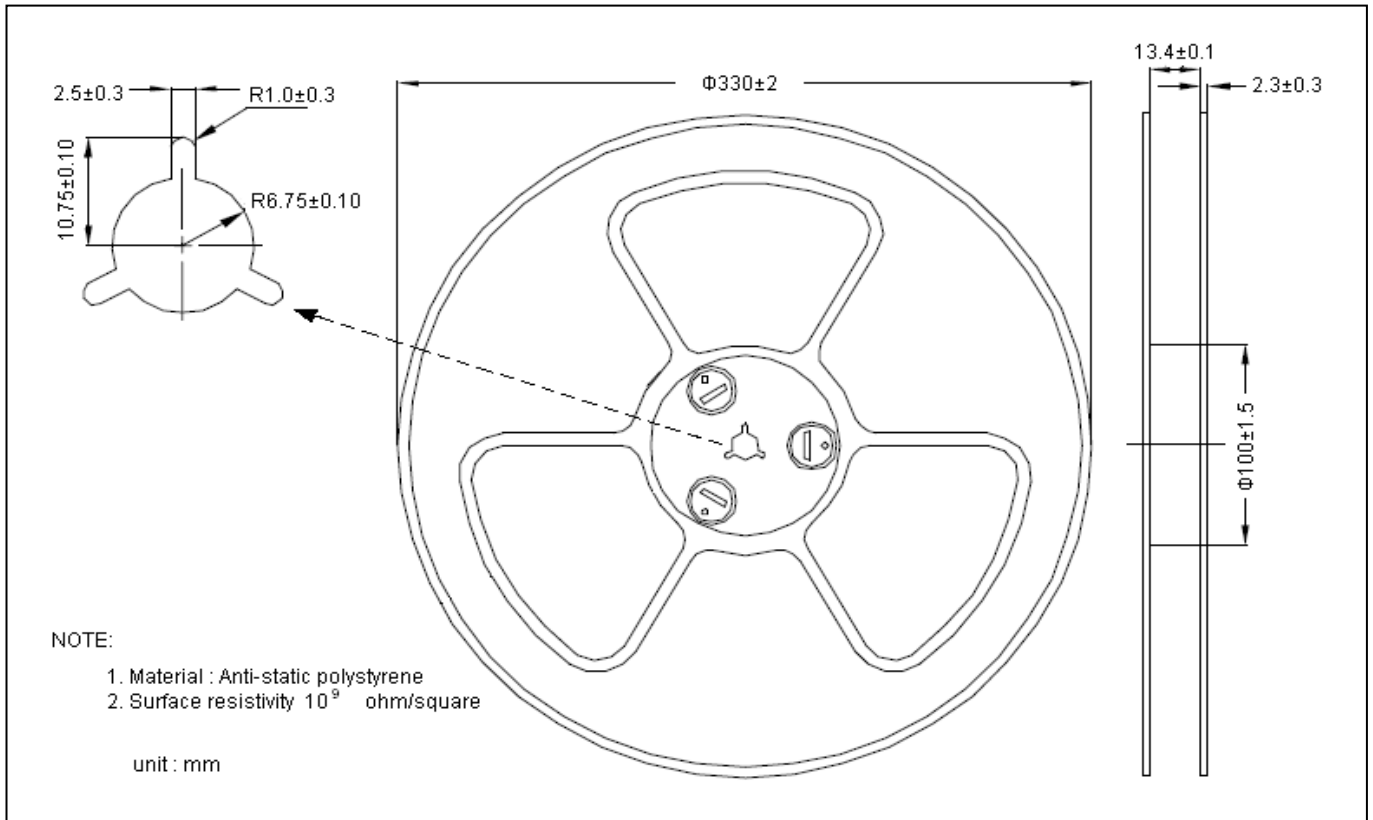
Single Pulse Power Rating, Junction to Ambient  
 (Note on page 2)



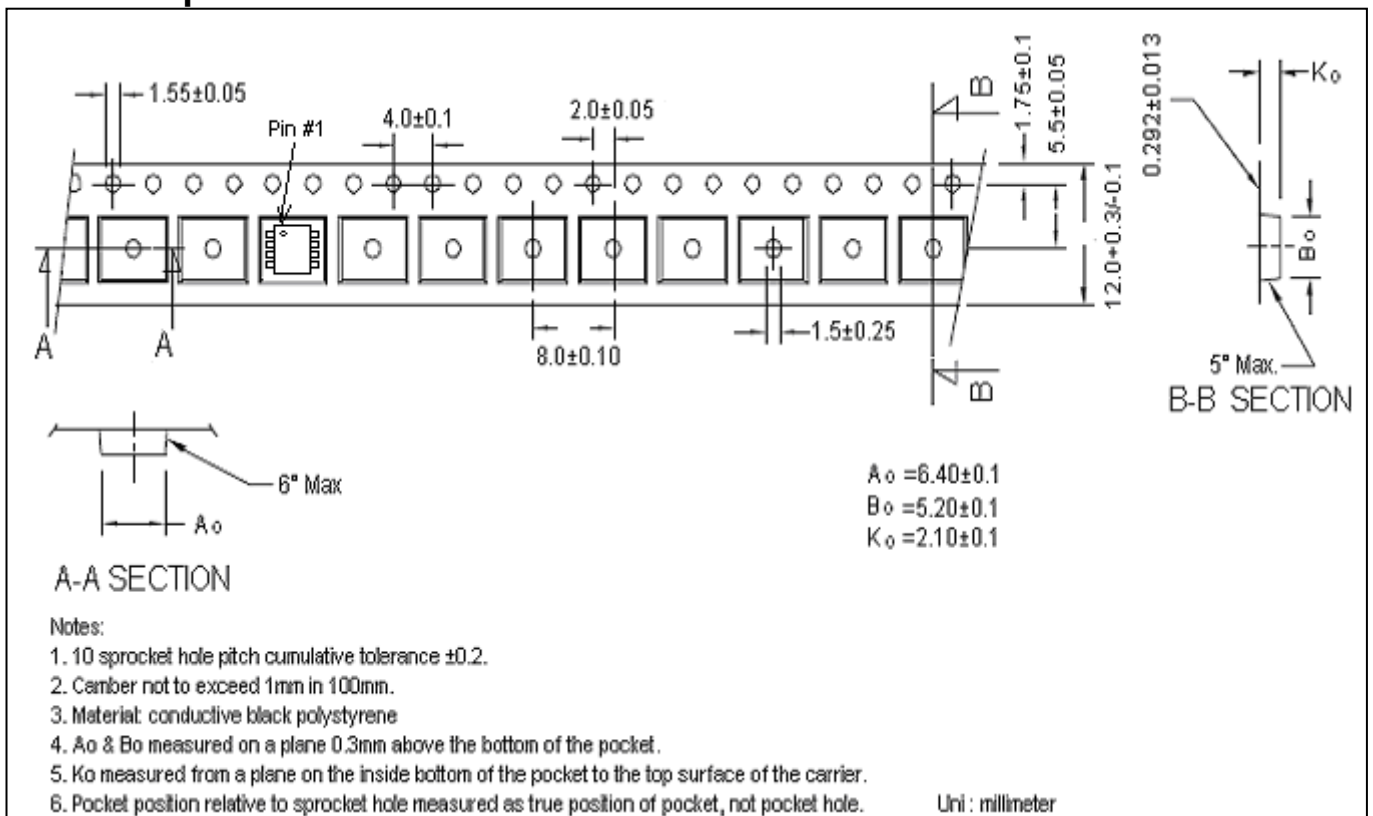
Transient Thermal Response Curves



**Reel Dimension**



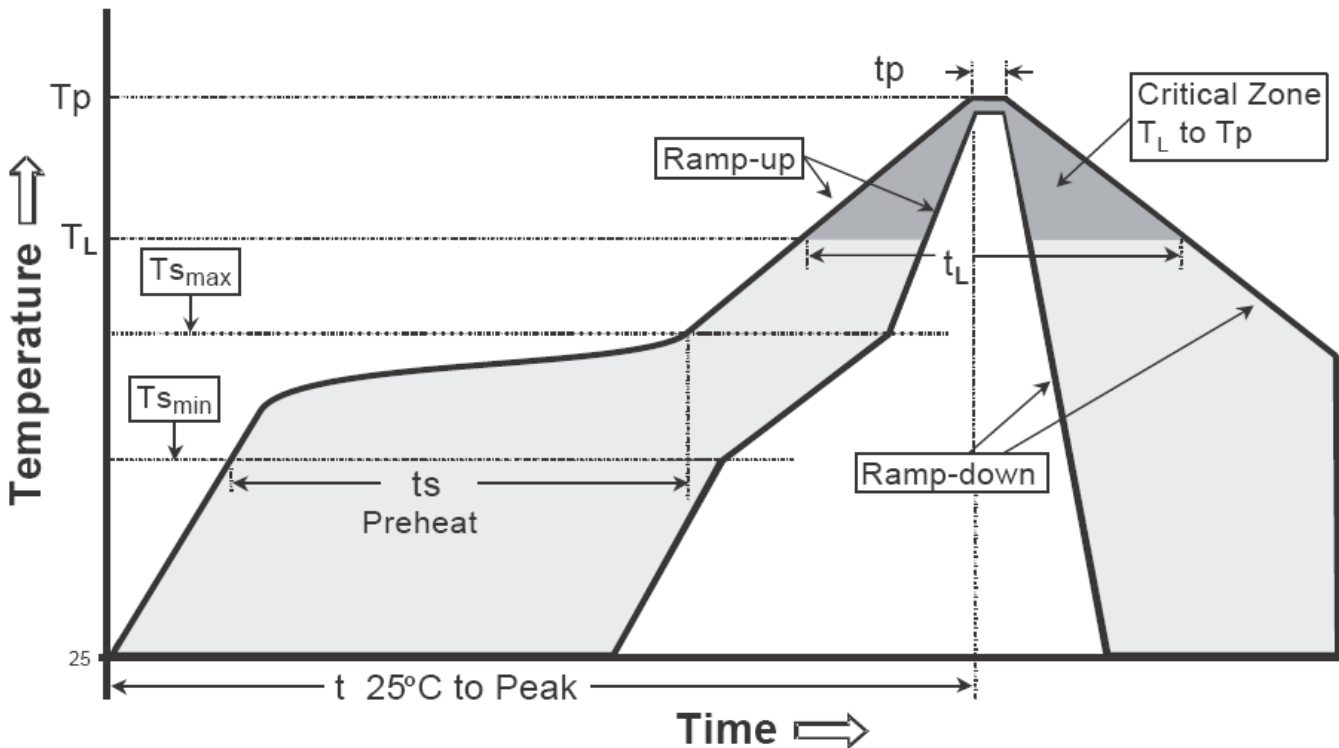
**Carrier Tape Dimension**



**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

**Recommended temperature profile for IR reflow**

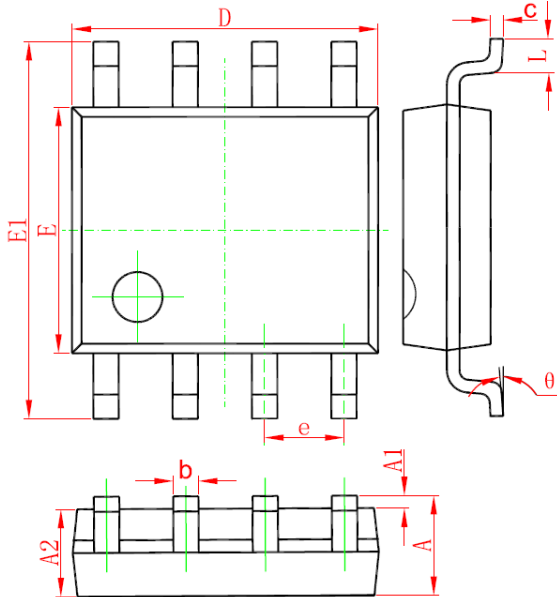


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

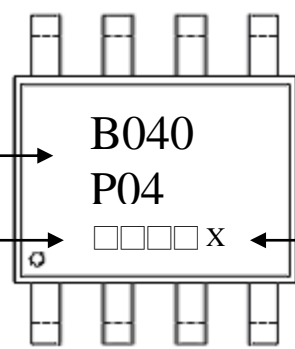
Note : All temperatures refer to topside of the package, measured on the package body surface.



**SOP-8 Dimension**



**Marking:**



Device Code → **B040**

Date Code →     X ← Assembly site code

Date Code(counting from left to right) :

1<sup>st</sup> code: year code, the last digit of Christian year

2<sup>nd</sup> code : month code, Jan→A, Feb→B, Mar→C, Apr→D  
 May→E, Jun→F, Jul→G, Aug→H, Sep→J,  
 Oct→K, Nov→L, Dec→M

3<sup>rd</sup> and 4<sup>th</sup> codes : production serial number, 01~99

Production site code : blank→ site 1, G →site 2

**8-Lead SOP-8 Plastic Package**  
 CYStek Package Code: Q8

\*: Typical

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069	E	3.800	4.000	0.150	0.157
A1	0.100	0.250	0.004	0.010	E1	5.800	6.200	0.228	0.244
A2	1.350	1.550	0.053	0.061	e	*1.270		*0.050	
b	0.330	0.510	0.013	0.020	L	0.400	1.270	0.016	0.050
c	0.170	0.250	0.006	0.010	θ	0°	8°	0°	8°
D	4.700	5.100	0.185	0.200					

**Notes:** 1.Controlling dimension: millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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