

P-Channel Enhancement Mode Power MOSFET

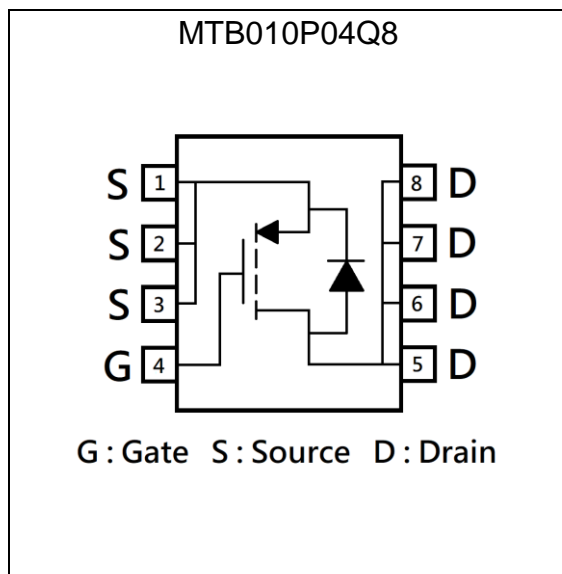
MTB010P04Q8

BV_{DSS}	-40V
I_D @ T_A=25°C, V_{GS}=-10V	-12.5A
I_D @ T_A=70°C, V_{GS}=-10V	-10A
R_{DS(ON)}@ V_{GS}=-10V, I_D=-15A	8.5 mΩ (typ)
R_{DS(ON)}@ V_{GS}=-4.5V, I_D=-10A	12.5mΩ (typ)

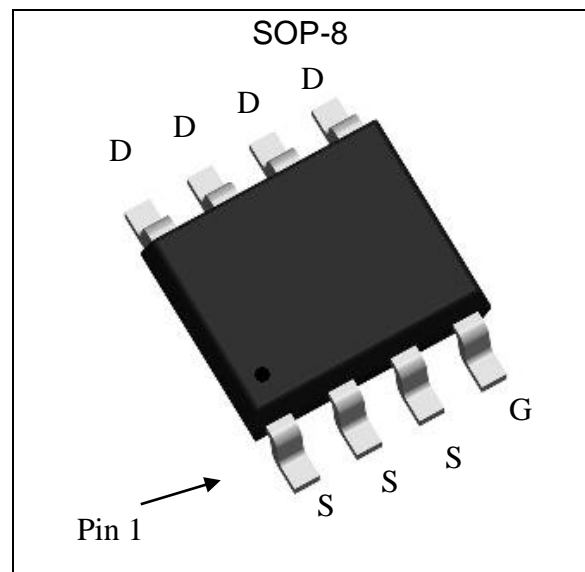
Features

- Simple drive requirement
- Low on-resistance
- Fast switching characteristic
- Pb-free & halogen-free package

Symbol

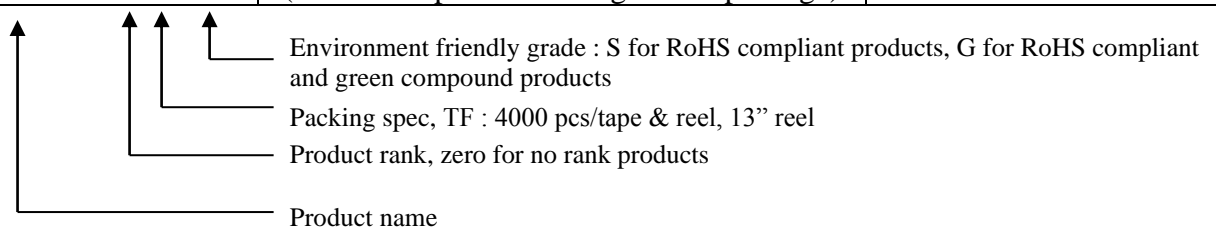


Outline



Ordering Information

Device	Package	Shipping
MTB010P04Q8-0-TF-G	SOP-8 (RoHS compliant & Halogen-free package)	4000 pcs / Tape & Reel





Absolute Maximum Ratings (Tc=25°C, unless otherwise noted)

Parameter	Symbol	Limits	Unit	
Drain-Source Voltage	V _{DS}	-40	V	
Gate-Source Voltage	V _{GS}	±20		
Continuous Drain Current @ V _{GS} =-10V, T _A =25°C	I _D	-12.5	A	
Continuous Drain Current @ V _{GS} =-10V, T _A =70°C		-10		
Pulsed Drain Current	I _{DM}	-104 *1		
Avalanche Current @ L=0.1mH	I _{AS}	-50		
Avalanche Energy @ L=1mH, I _D =-24A, V _{DD} =-15V	E _{AS}	288 *2	mJ	
Repetitive Avalanche Energy @ L=0.05mH	E _{AR}	2.5		
Total Power Dissipation	P _D	T _A =25 °C	3.1 *3	W
		T _A =70 °C	2.0 *3	
Operating Junction and Storage Temperature	T _j , T _{stg}	-55~+150	°C	

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	R _{θJC}	20	°C/W
Thermal Resistance, Junction-to-ambient, max	R _{θJA}	40 *3	

Note : *1. Duty cycle ≤ 1%, pulse width ≤ 100μs.

*2. 100% tested by conditions of L=0.1mH, I_{AS}=-10A, V_{GS}=-10V, V_{DD}=-15V

*3. Surface mounted on 1 in² copper pad of FR-4 board, t ≤ 10s; 125 °C/W when mounted on minimum copper pad.

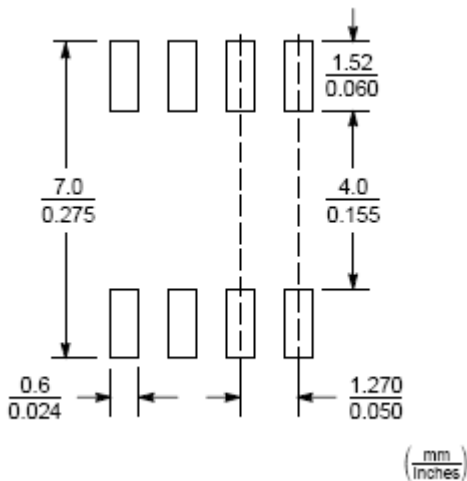
Characteristics (Tc=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	-40	-	-	V	V _{GS} =0V, I _D =-250μA
V _{GS(th)}	-1	-	-2.5		V _{DS} = V _{GS} , I _D =-250μA
I _{GSS}	-	-	±100	nA	V _{GS} =±20V, V _{DS} =0V
I _{DSS}	-	-	-1	μA	V _{DS} =-32V, V _{GS} =0V
	-	-	-10		V _{DS} =-32V, V _{GS} =0V, T _j =125°C
*R _{DS(ON)}	-	8.5	12	mΩ	V _{GS} =-10V, I _D =-15A
	-	12.5	20		V _{GS} =-4.5V, I _D =-10A
G _{FS}	-	24.1	-	S	V _{DS} =-10V, I _D =-10A
Dynamic					
C _{iss}	-	3384	-	pF	V _{DS} =-20V, V _{GS} =0V, f=1MHz
C _{oss}	-	276	-		
C _{rss}	-	203	-		

Characteristics (Cont. Tc=25°C, unless otherwise specified)

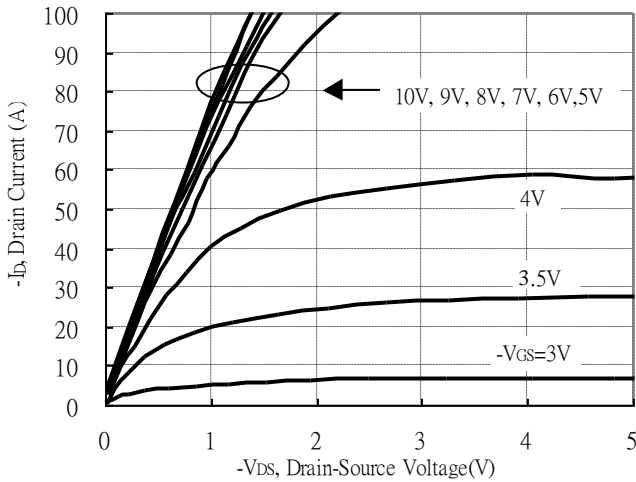
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Dynamic					
$t_{d(ON)}$ *1, 2	-	17.4	-	ns	$V_{DS}=-20V, I_D=-15A, V_{GS}=-10V,$ $R_G=1\Omega$
t_r *1, 2	-	20.6	-		
$t_{d(OFF)}$ *1, 2	-	96.4	-		
t_f *1, 2	-	16.4	-	nC	$V_{DS}=-20V, I_D=-4A, V_{GS}=-10V$
Q_g *1, 2	-	67.6	-		
Q_{gs} *1, 2	-	10.5	-		
Q_{gd} *1, 2	-	14.3	-		
R_g	-	5.3	-	Ω	$f=1MHz$
Source-Drain Diode Ratings and Characteristics					
I_S *1	-	-	-2.6	A	
I_{SM} *3	-	-	-10		
V_{SD} *1	-	-0.82	-1.2	V	$I_S=-10A, V_{GS}=0V$
t_{rr}	-	16.4	-	ns	$I_F=-10A, dI_F/dt=100A/\mu s$
Q_{rr}	-	11.0	-	nC	

Note : *1.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
 *2.Independent of operating temperature
 *3.Pulse width limited by maximum junction temperature.

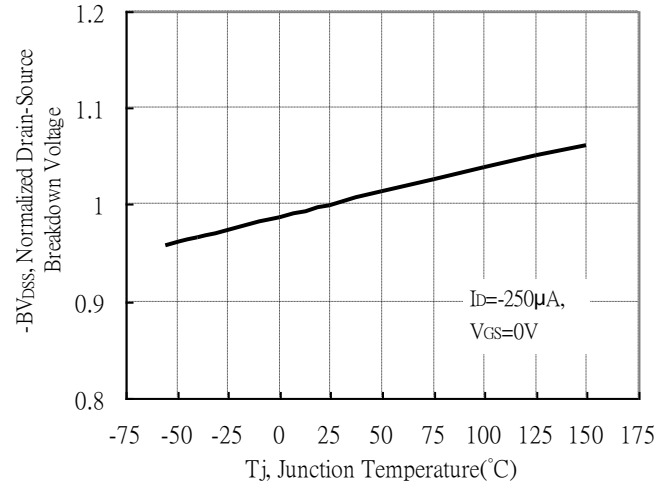
Recommended Soldering Footprint


Typical Characteristics

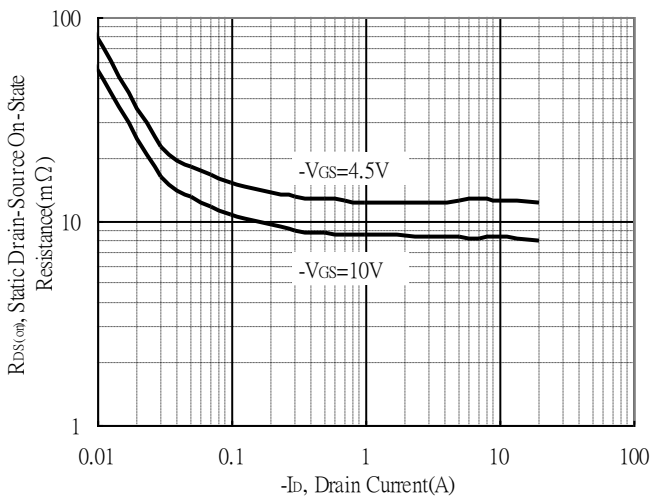
Typical Output Characteristics



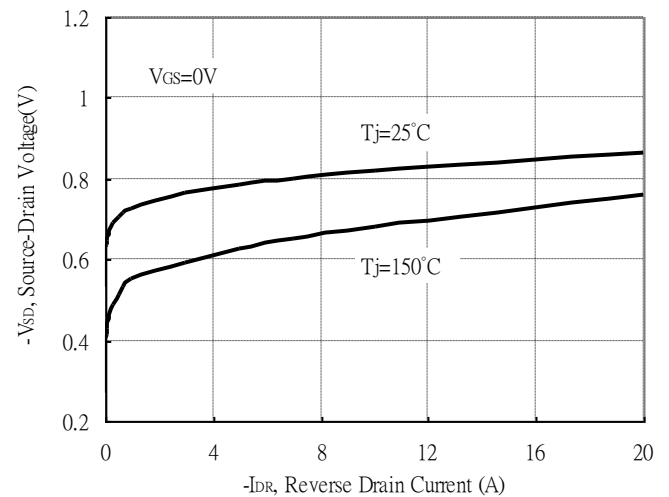
Brekdown Voltage vs Ambient Temperature



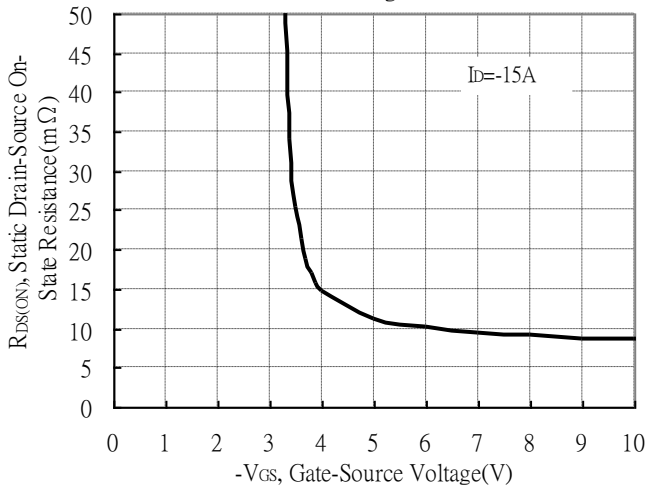
Static Drain-Source On-State resistance vs Drain Current



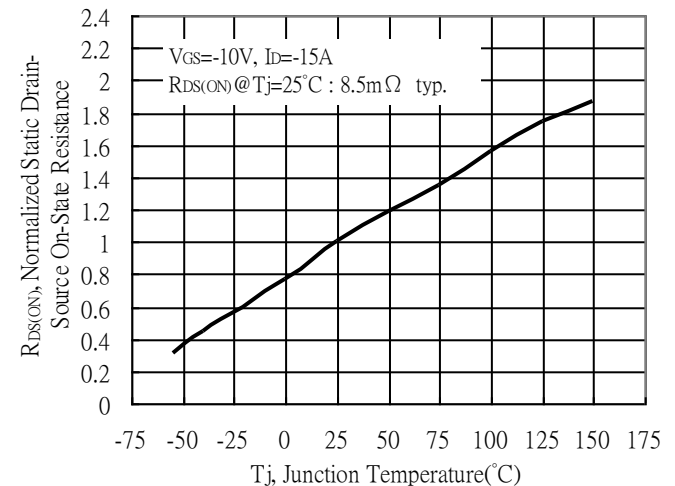
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

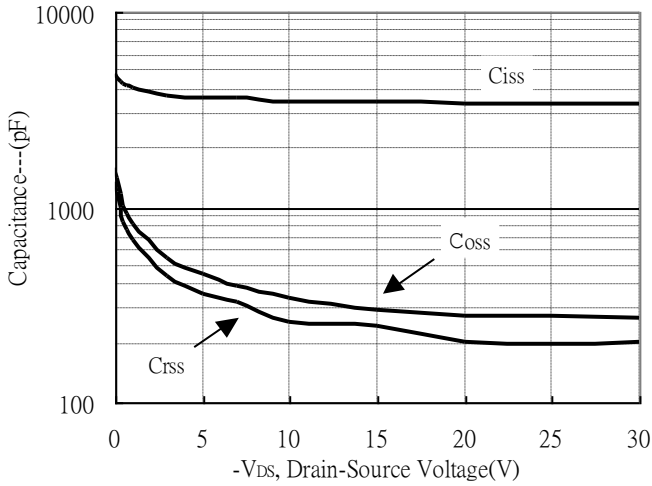


Drain-Source On-State Resistance vs Junction Temperature

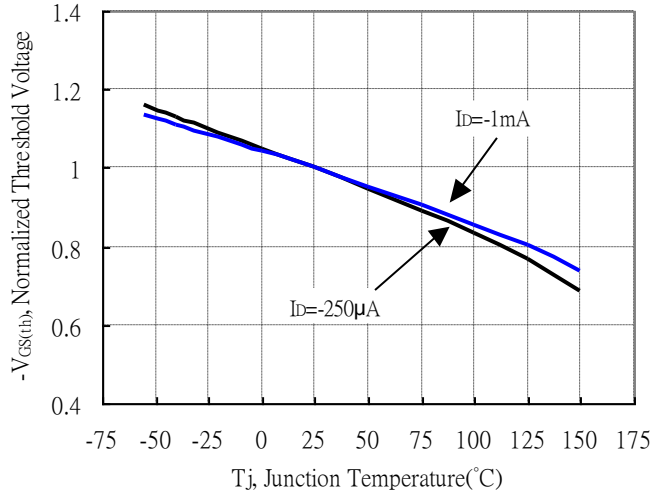


Typical Characteristics(Cont.)

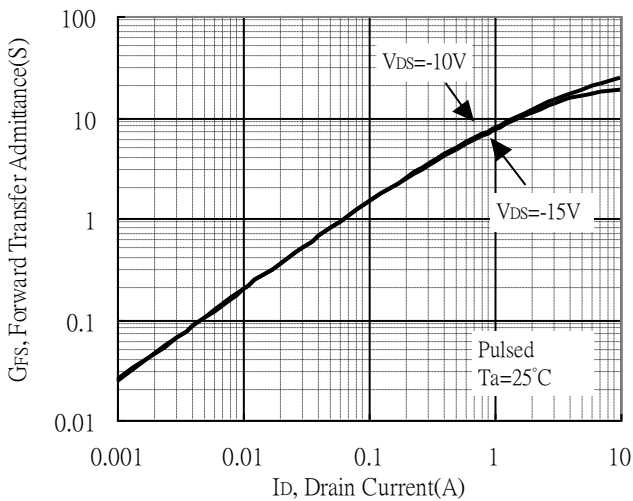
Capacitance vs Drain-to-Source Voltage



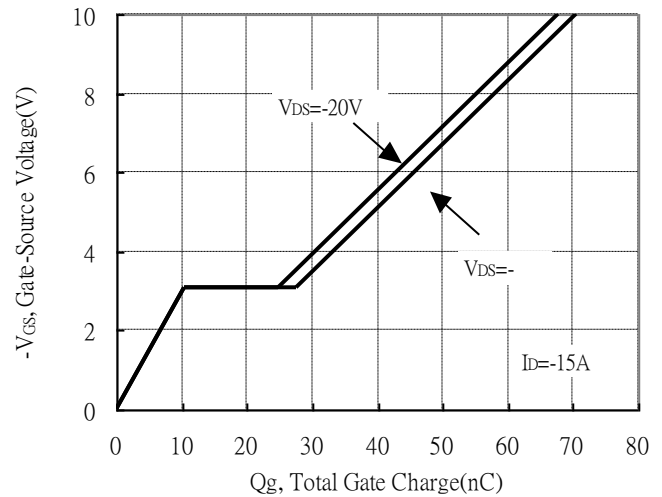
Threshold Voltage vs Junction Temperature



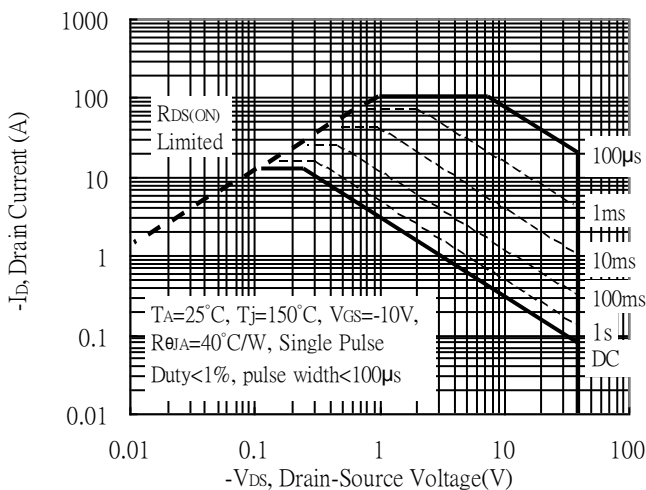
Forward Transfer Admittance vs Drain Current



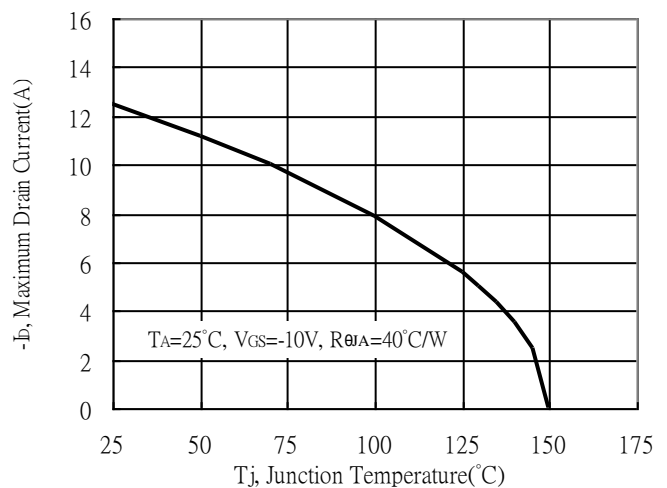
Gate Charge Characteristics



Maximum Safe Operating Area

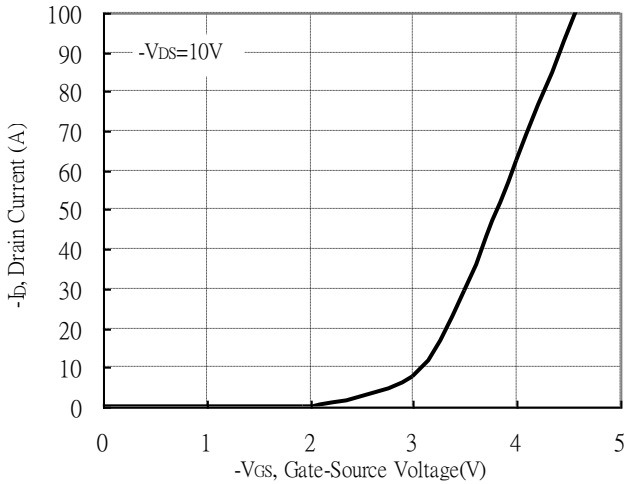


Maximum Drain Current vs Junction Temperature

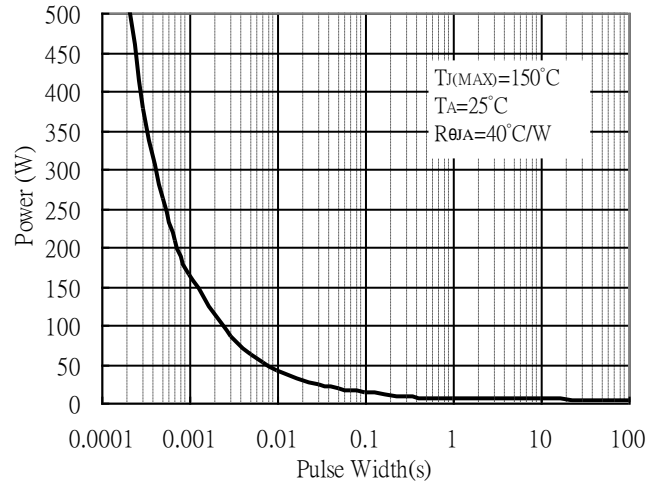


Typical Characteristics(Cont.)

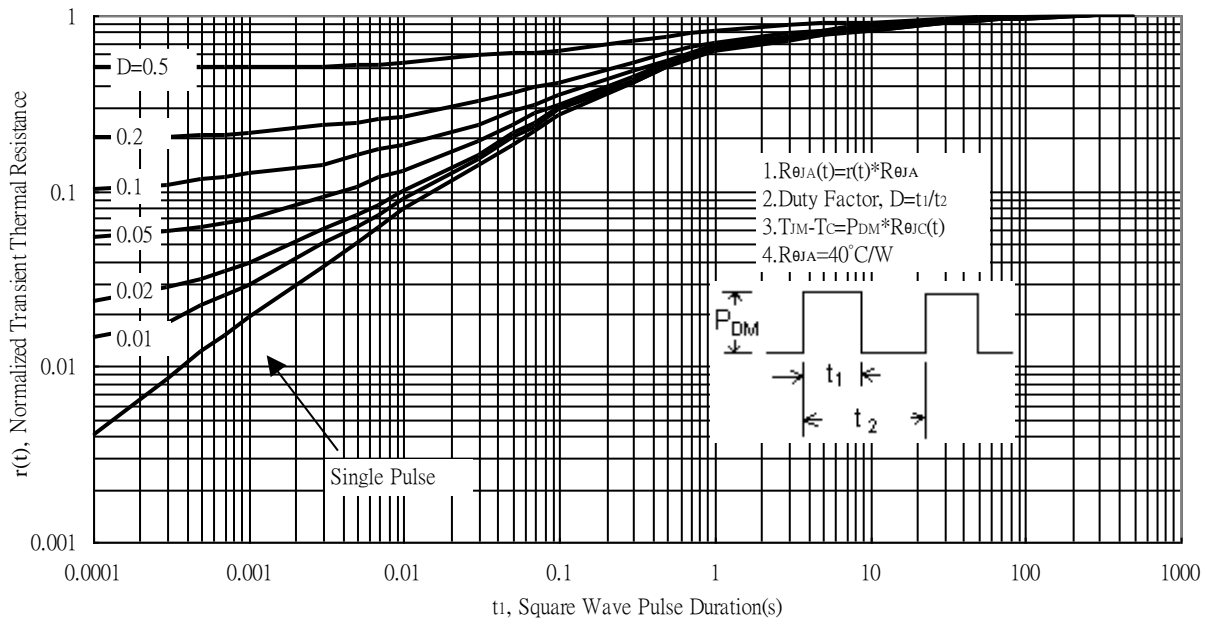
Typical Transfer Characteristics



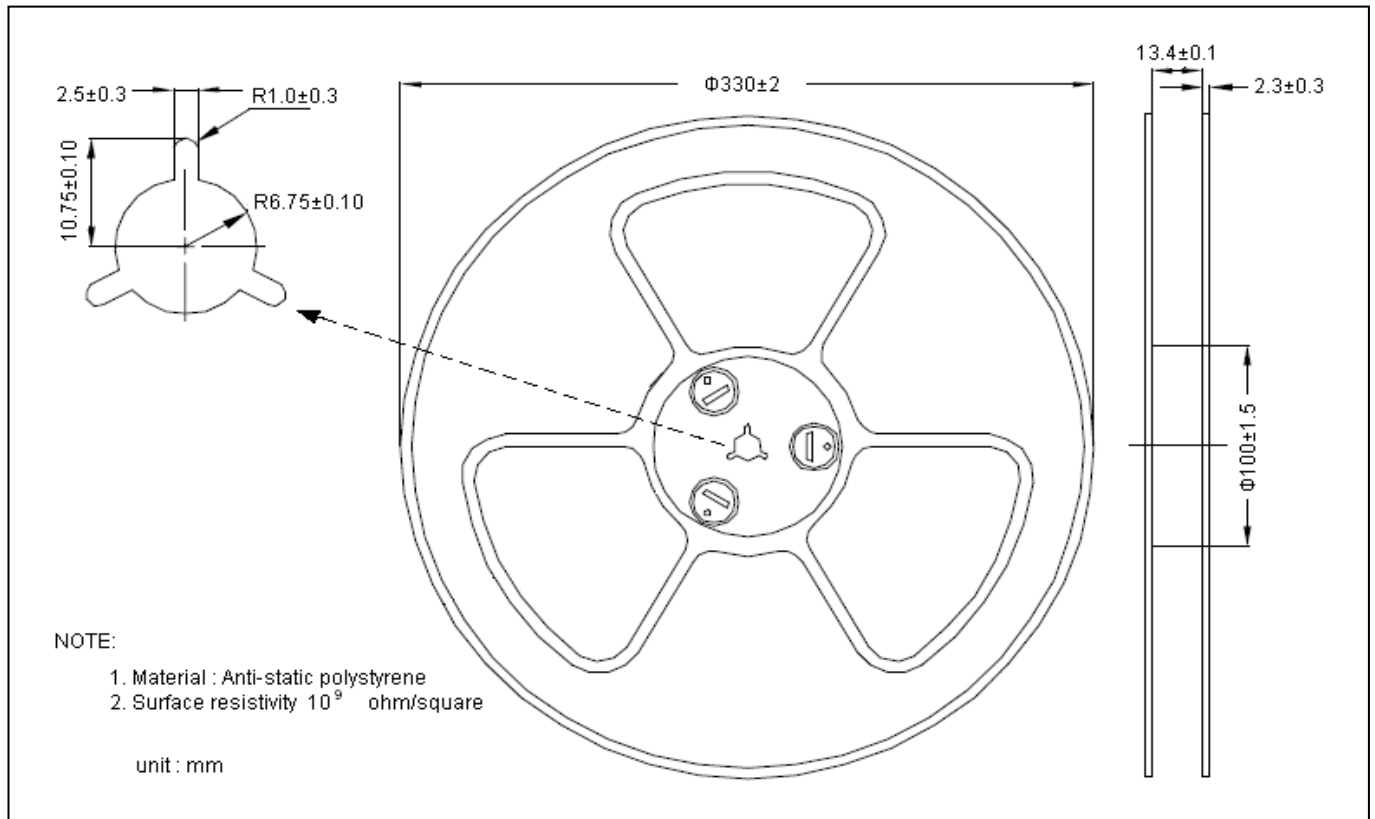
Single Pulse Power Rating, Junction to Ambient
 (Note on page 2)



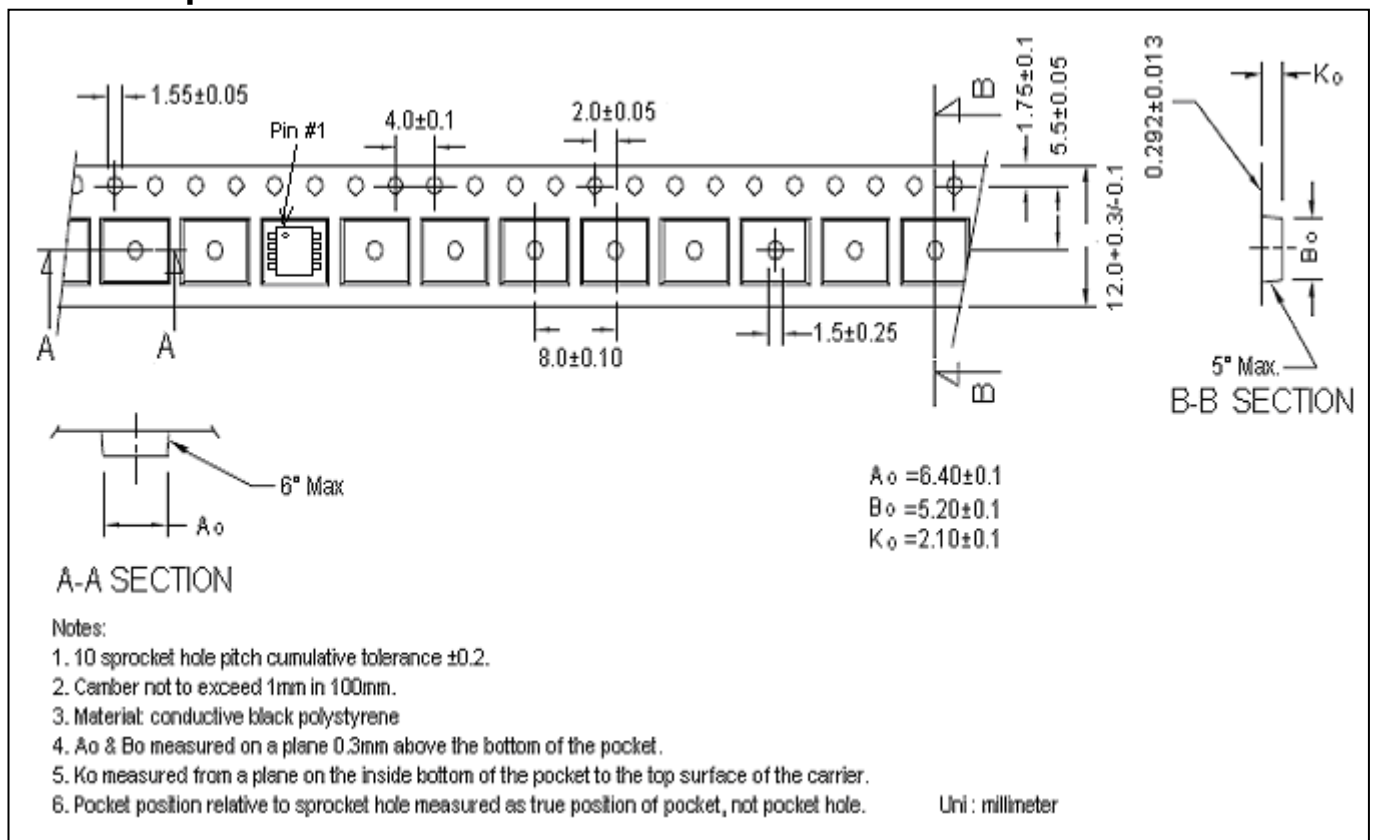
Transient Thermal Response Curves



Reel Dimension



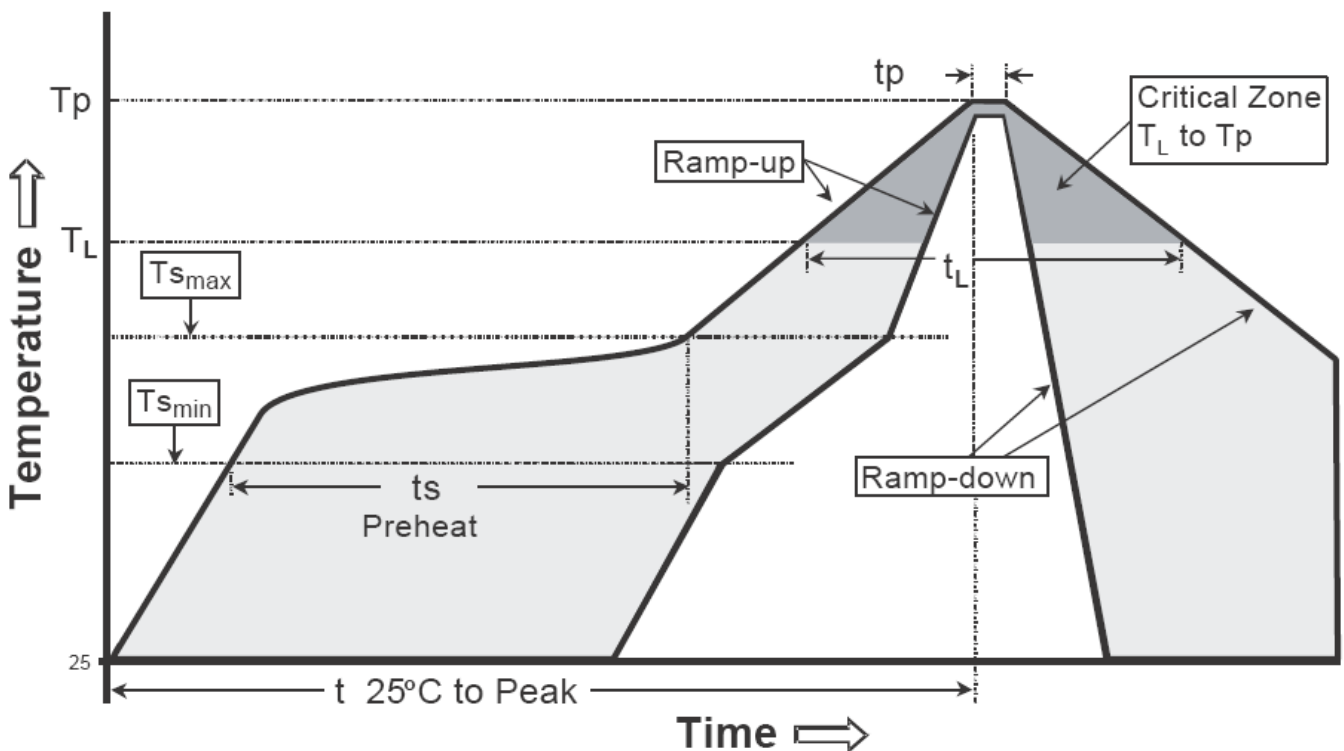
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

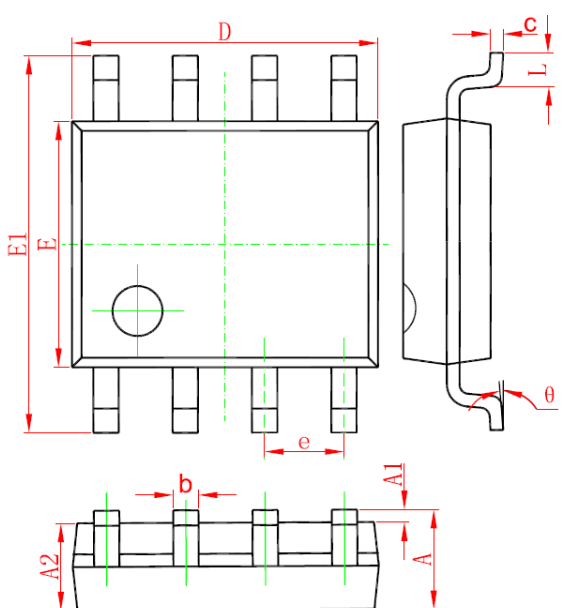
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

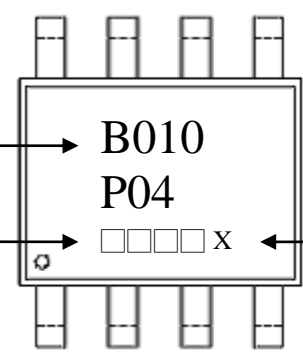
Note : All temperatures refer to topside of the package, measured on the package body surface.

SOP-8 Dimension



The diagram shows three views of an 8-lead SOP-8 package: a top view with dimensions D, E, E1, and e; a side view with dimensions c, L, and θ ; and a bottom view with dimensions A, A1, A2, and b.

Marking:



Device Code → **B010**
 P04
 Date Code → □□□□ X ← Assembly site code

Date Code(counting from left to right) :
 1st code : year code, the last digit of Christian year
 2nd code : month code, Jan→A, Feb→B, Mar→C, Apr→D,
 May→E, Jun→F, Jul→G, Aug→H, Sep→J, Oct→K,
 Nov→L, Dec→M
 3rd and 4th codes : production serial number, 01~99

Assembly site code : blank→ site 1, G→site 2

8-Lead SOP-8 Plastic Package
 CYStek Package Code: Q8

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069	E	3.800	4.000	0.150	0.157
A1	0.100	0.250	0.004	0.010	E1	5.800	6.200	0.228	0.244
A2	1.350	1.550	0.053	0.061	e	*1.270		*0.050	
b	0.330	0.510	0.013	0.020	L	0.400	1.270	0.016	0.050
c	0.170	0.250	0.006	0.010	θ	0°	8°	0°	8°
D	4.700	5.100	0.185	0.200					

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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