

N-Channel Enhancement Mode MOSFET

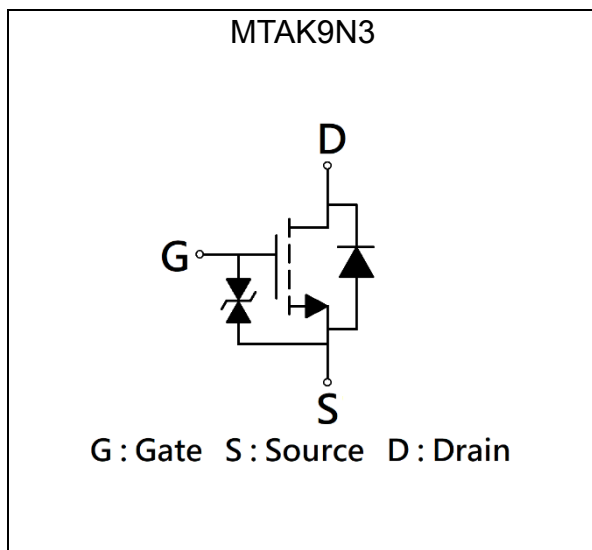
MTAK9N3

Features

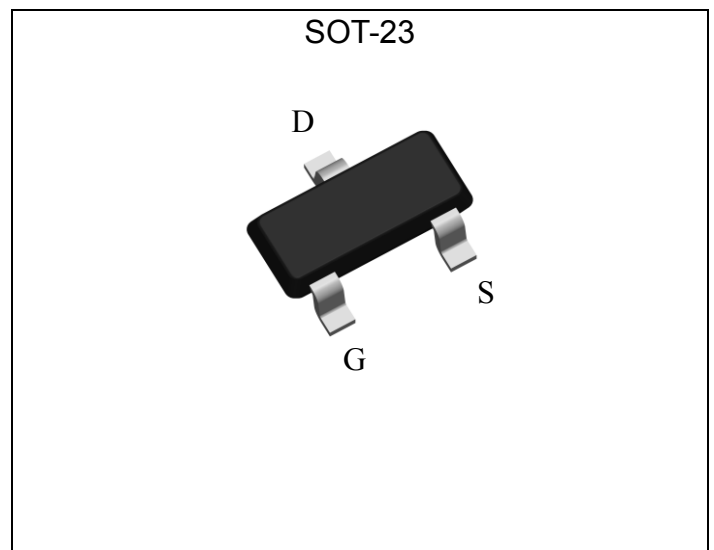
- ESD protected gate, typical 3kV (HBM)
- High speed switching
- Easily designed drive circuits
- Low-voltage drive
- Easy to use in parallel
- RoHS compliant package

BV_{DSS}	20V
$I_D @ V_{GS}=4.5V, T_A=25^\circ C$	0.45A
$R_{DS(ON) \text{ typ.}} @ V_{GS}=4.5V, I_D=0.2A$	0.65 Ω
$R_{DS(ON) \text{ typ.}} @ V_{GS}=2.5V, I_D=0.2A$	0.8 Ω
$R_{DS(ON) \text{ typ.}} @ V_{GS}=1.8V, I_D=0.2A$	1 Ω

Equivalent Circuit

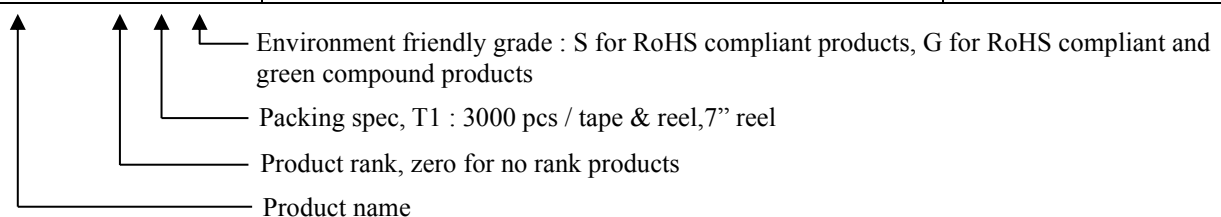


Outline



Ordering Information

Device	Package	Shipping
MTAK9N3-0-T1-G	SOT-23 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel



**Absolute Maximum Ratings (T_A=25°C)**

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	±8	
Continuous Drain Current @ V _{GS} =4.5V, T _A =25°C	I _D	0.45	A
Continuous Drain Current @ V _{GS} =4.5V, T _A =70°C		0.36	
Pulsed Drain Current *a	I _{DM}	1.8	
Continuous Body Diode Forward Current @ T _A =25°C	I _S	0.3	
ESD susceptibility *b	V _{ESD}	3000	V
Total Power Dissipation @ T _A =25°C	P _D	0.3	W
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55~+150	°C

Thermal Data

Parameter	Symbol	Steady State	Unit
Thermal Resistance, Junction-to-ambient	R _{θJA}	357	°C/W

Note:

*a. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and low duty cycles to keep initial T_J=25°C.

*b. Human body model, 1.5kΩ in series with 100pF.



Electrical Characteristics (T_A=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	20	-	-	V	V _{GS} =0V, I _D =250μA
V _{GS(th)}	0.3	-	1		V _{DS} =V _{GS} , I _D =250μA
G _{FS}	-	1	-	S	V _{DS} =5V, I _D =0.2A
I _{GSS}	-	-	±10	μA	V _{GS} =±8V, V _{DS} =0V
I _{DSS}	-	-	1		V _{DS} =16V, V _{GS} =0V
R _{DS(ON)}	-	0.65	1	Ω	V _{GS} =4.5V, I _D =0.2A
	-	0.8	1.8		V _{GS} =2.5V, I _D =0.2A
	-	1	3		V _{GS} =1.8V, I _D =0.2A
Dynamic					
C _{iss}	-	32	-	pF	V _{DS} =10V, V _{GS} =0V, f=1MHz
C _{oss}	-	19	-		
C _{rss}	-	17	-		
Q _g *1, 2	-	0.8	-	nC	V _{DS} =10V, I _D =0.2A, V _{GS} =4.5V
Q _{gs} *1, 2	-	0.2	-		
Q _{gd} *1, 2	-	0.15	-		
t _{d(ON)} *1, 2	-	4.8	-	ns	V _{DS} =10V, I _D =0.2A, V _{GS} =4.5V, R _{GS} =10Ω
t _r *1, 2	-	16	-		
t _{d(OFF)} *1, 2	-	20	-		
t _f *1, 2	-	15.6	-		
Source-Drain Diode					
V _{SD} *1	-	0.8	1.2	V	I _S =0.2A, V _{GS} =0V
t _{rr}	-	7	-	ns	I _F =0.2A, dI _F /dt=100A/μs
Q _{rr}	-	1	-	nC	

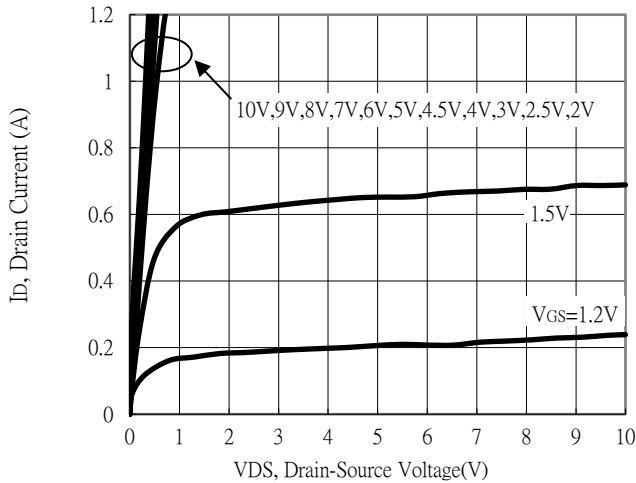
Note:

*1. Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

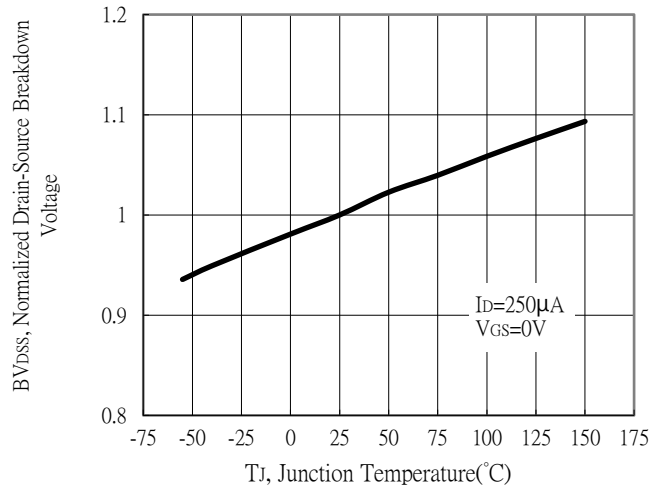
*2. Independent of operating temperature

Typical Characteristics

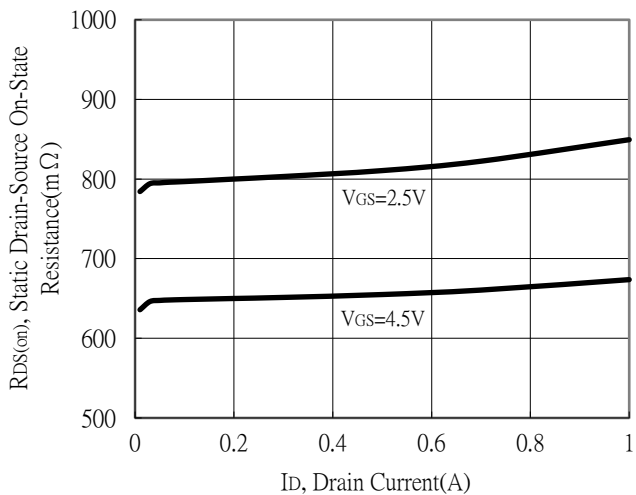
Typical Output Characteristics



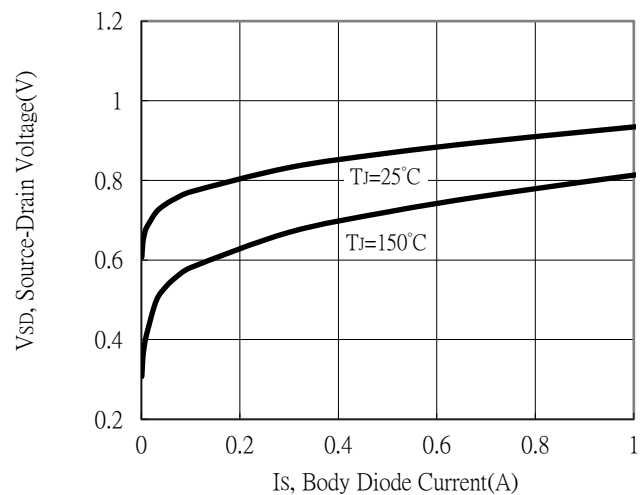
Breakdown Voltage vs Junction Temperature



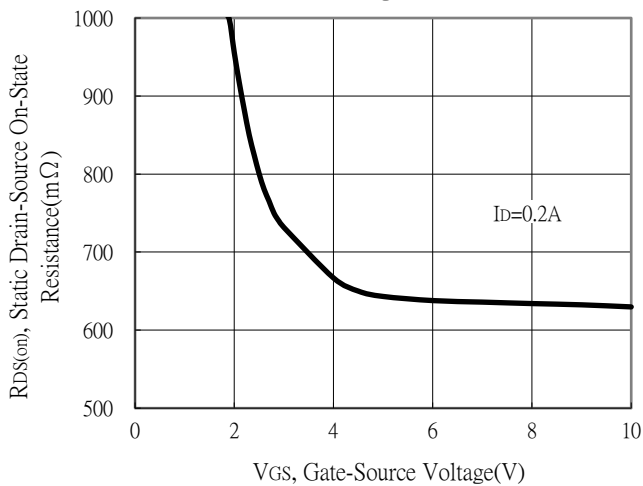
Static Drain-Source On-State resistance vs Drain Current



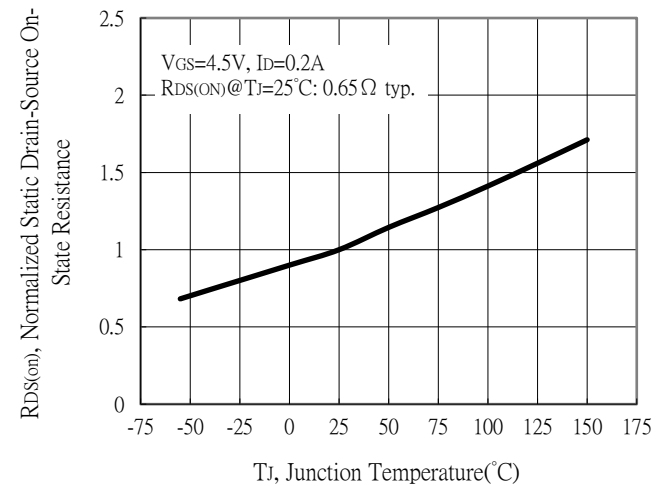
Body Diode Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

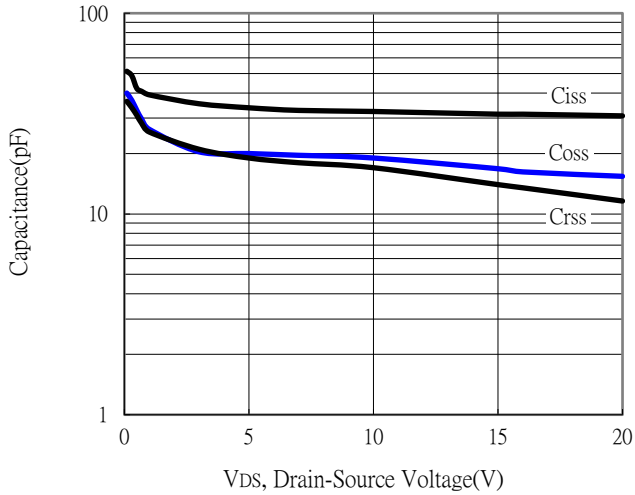


Drain-Source On-State Resistance vs Junction Temperature

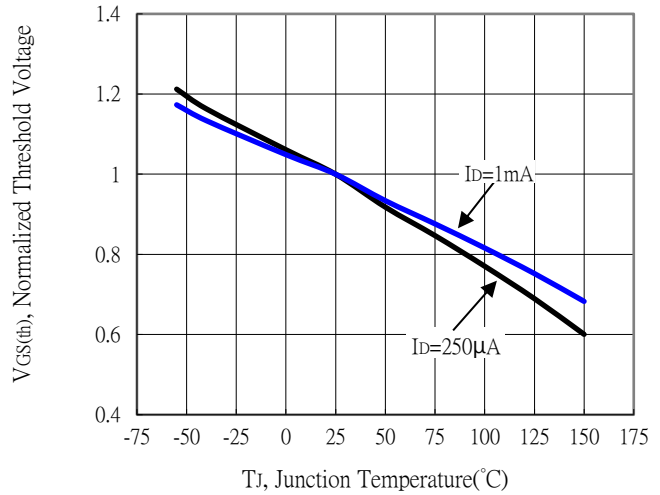


Typical Characteristics (Cont.)

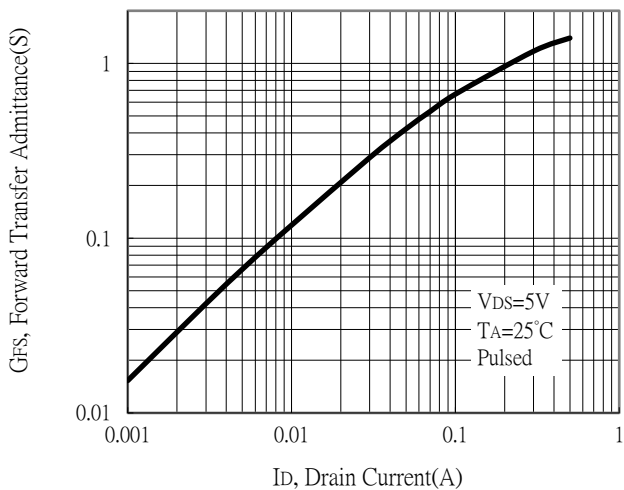
Capacitance vs Drain-to-Source Voltage



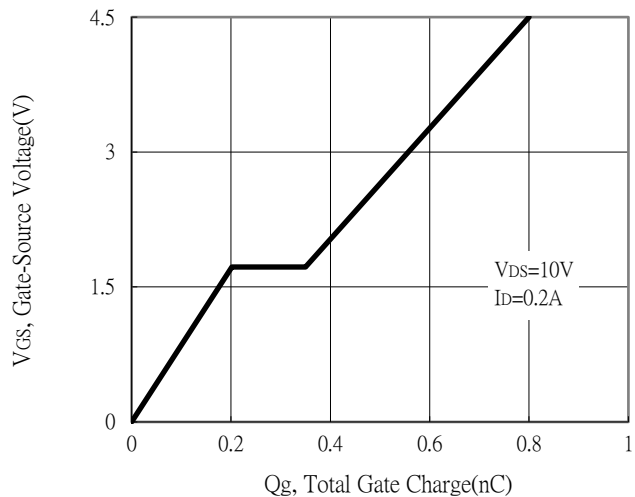
Threshold Voltage vs Junction Temperature



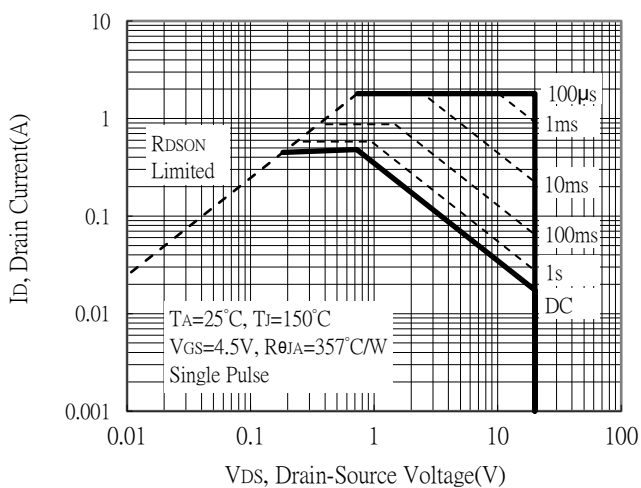
Forward Transfer Admittance vs Drain Current



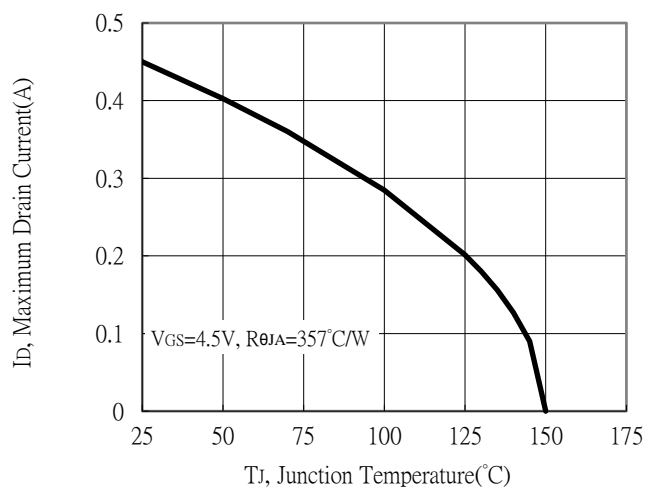
Gate Charge Characteristics



Maximum Safe Operating Area

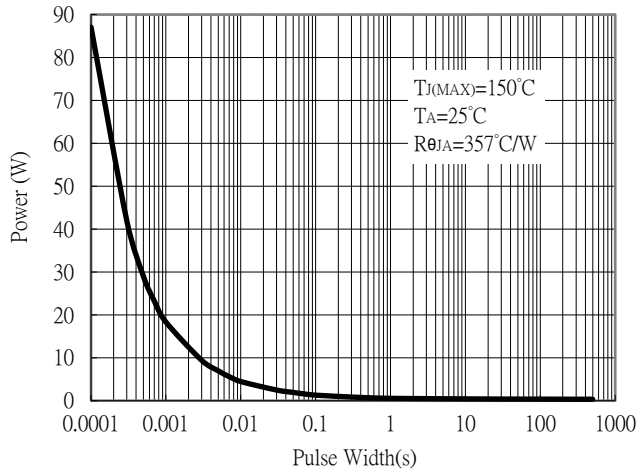


Maximum Drain Current vs Junction Temperature

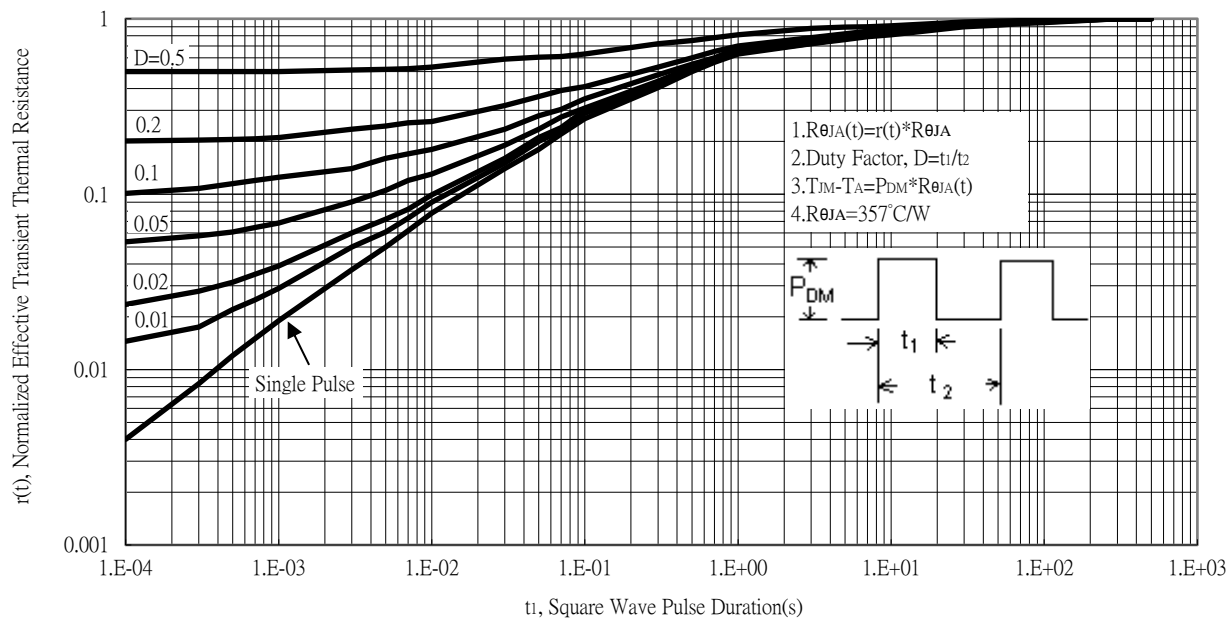


Typical Characteristics (Cont.)

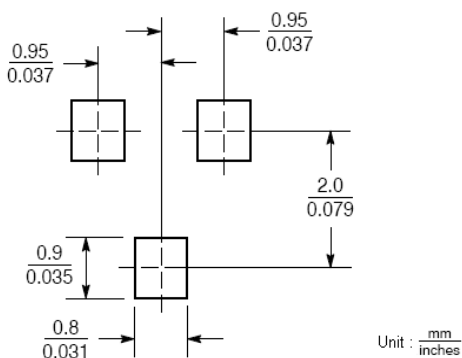
Single Pulse Power Rating, Junction to Ambient



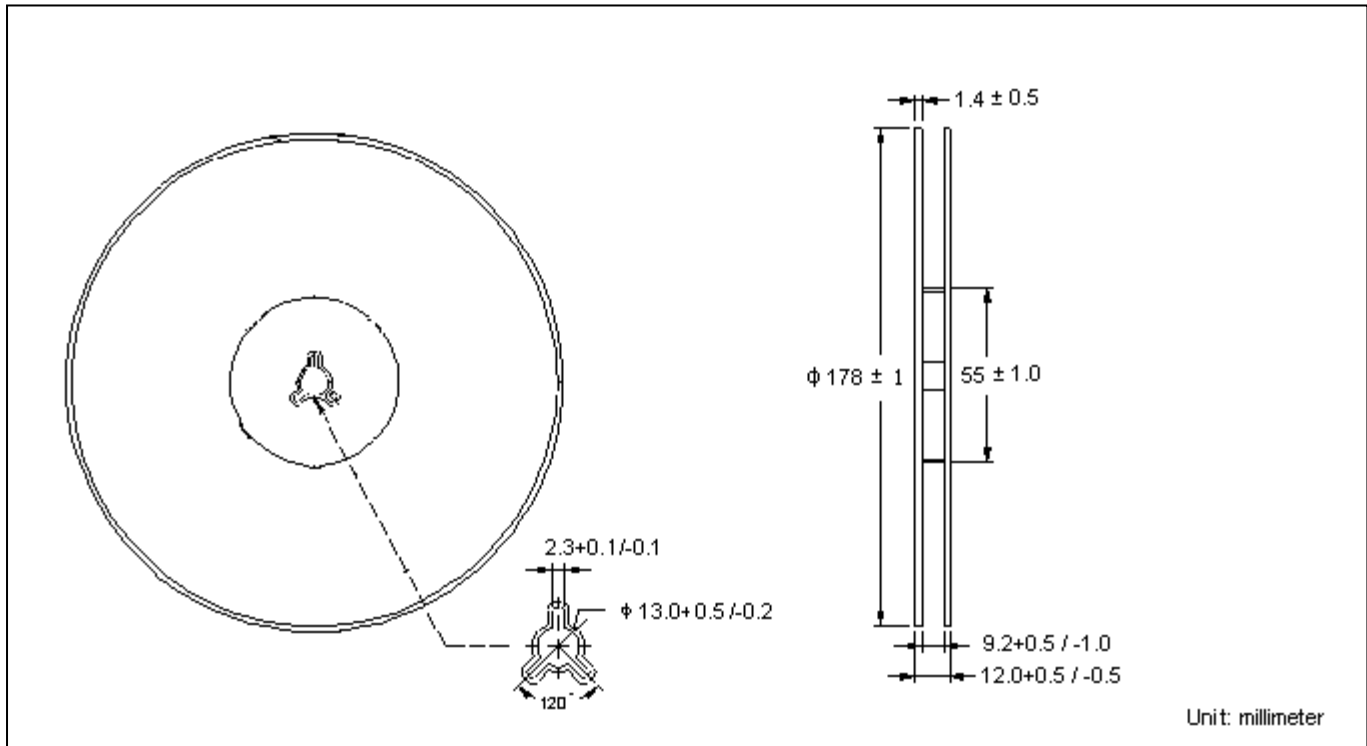
Transient Thermal Response Curves



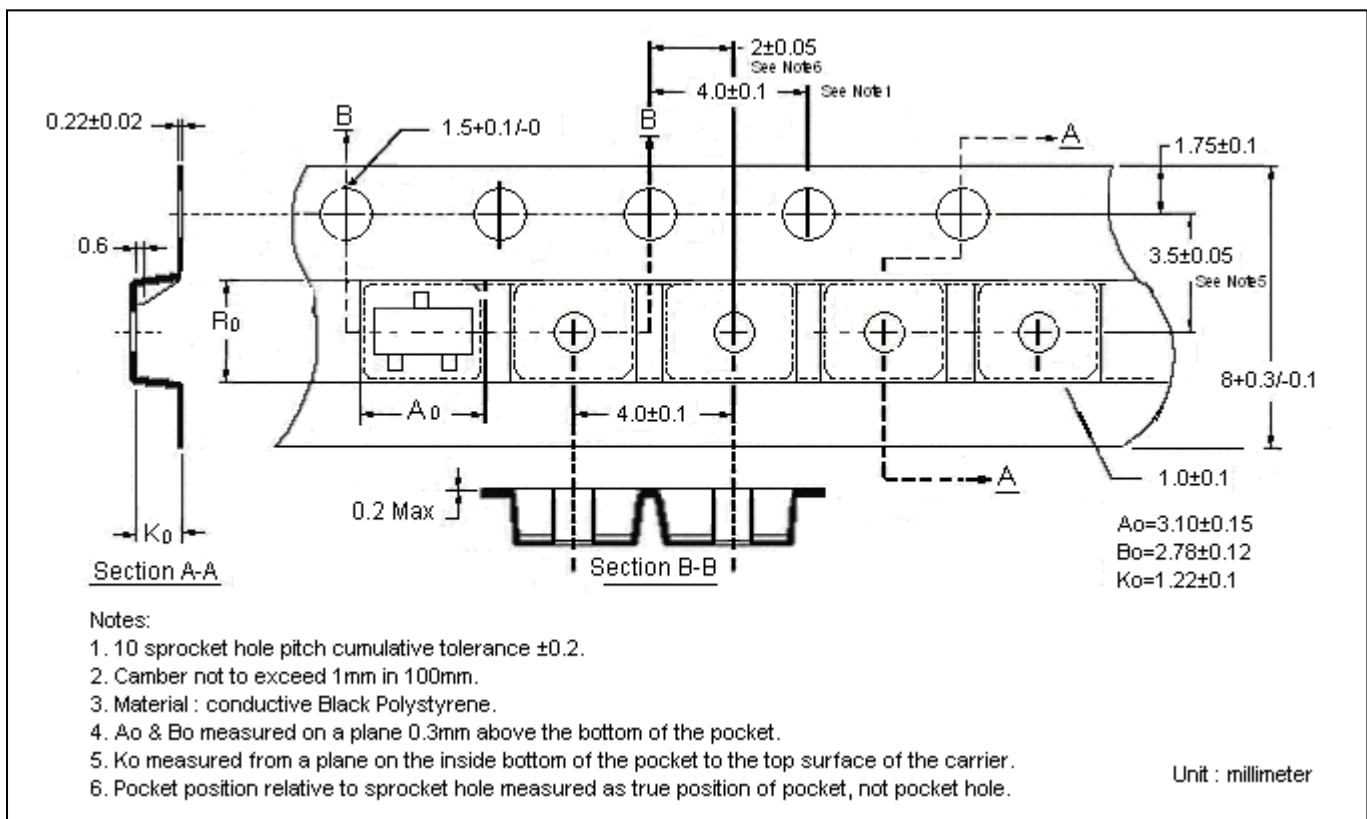
Recommended Soldering Footprint



Reel Dimension



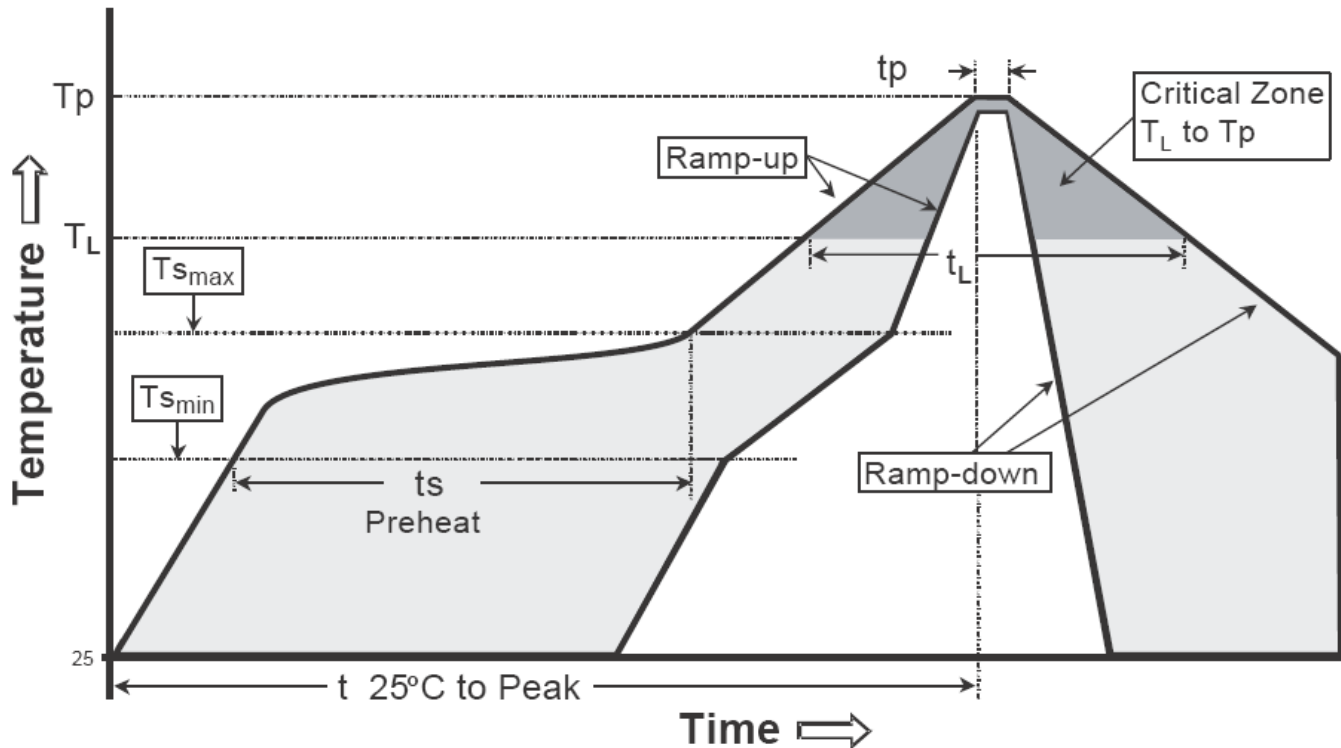
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

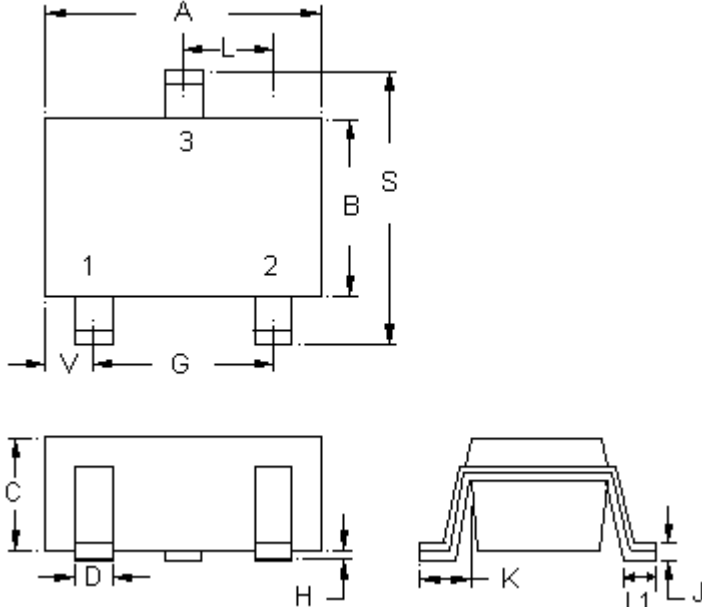
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (Tl)	183°C	217°C
- Time (tl)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

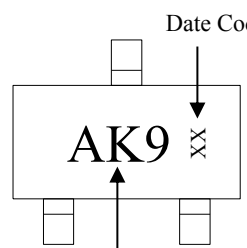
Note : 1. All temperatures refer to topside of the package, measured on the package body surface.
 2. For devices mounted on FR-4 PCB of 1.6mm or equivalent grade PCB. If other grade PCB is used, care should be taken to match the coefficients of thermal expansion between components and PCB. If they are not matched well, the solder joints may crack or the bodies of the parts may crack or shatter as the assembly cools.

SOT-23 Dimension



The diagram shows three views of the SOT-23 package: a top view with dimensions A, L, B, S, 1, 2, 3, V, and G; a side view with dimensions C, D, H, and J; and a perspective view of the leads with dimensions K, L1, and L2.

Marking:



The marking diagram shows a rectangular package with three leads. The top lead is labeled 'Date Code' with a downward arrow. The bottom-left lead is labeled 'Device Code' with an upward arrow. The center of the package is marked with 'AK9' and 'XX'.

3-Lead SOT-23 Plastic Surface Mounted Package
 CYStek Package Code: N3

Style: Pin 1.Gate 2.Source 3.Drain

Date Code : Year + Month
 Year : 9→2019,0→2020, ..., etc
 Month : 1→Jan,2→Feb, ..., 9→Sep, A→Oct, B→Nov, C→Dec

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1102	0.1181	2.80	3.00	J	0.0032	0.0059	0.08	0.15
B	0.0472	0.0551	1.20	1.40	K	0.0217	REF	0.55	REF
C	0.0354	0.0413	0.90	1.05	L	0.0374	TYP	0.95	TYP
D	0.0118	0.0197	0.30	0.50	S	0.0886	0.1004	2.25	2.55
G	0.0709	0.0787	1.80	2.00	V	0.0098	0.0256	0.25	0.65
H	0.0000	0.0040	0.00	0.10	L1	0.0118	0.0197	0.30	0.50

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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