

ESD protected Dual N-channel MOSFET

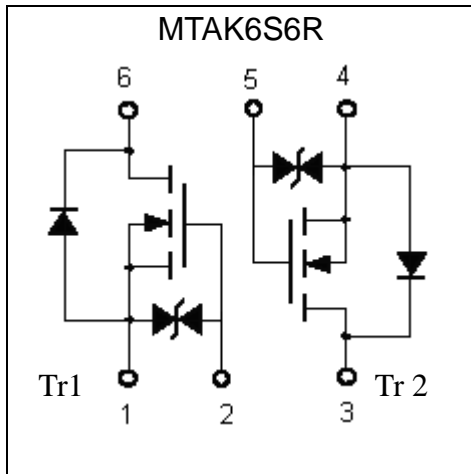
MTAK6S6R

BV_{DSS}	60V	
$I_D @ V_{GS}=4.5V, T_A=25^\circ C$	250mA	
$R_{DS(on)(TYP)}$	$V_{GS}=4.5V, I_D=200mA$	1.3 Ω
	$V_{GS}=2.5V, I_D=100mA$	1.7 Ω

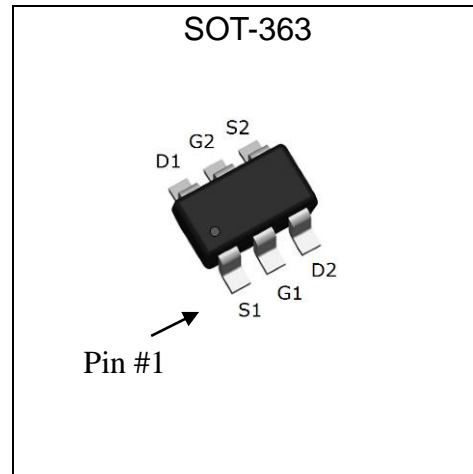
Description

- Low voltage drive(2.5V drive) makes this device ideal for portable equipment.
- The MOSFET elements are independent, eliminating mutual interference.
- Mounting cost and area can be cut in half.
- High speed switching
- ESD protected device, $HBM \geq 2kV$
- Pb-free lead plating & halogen-free package

Symbol

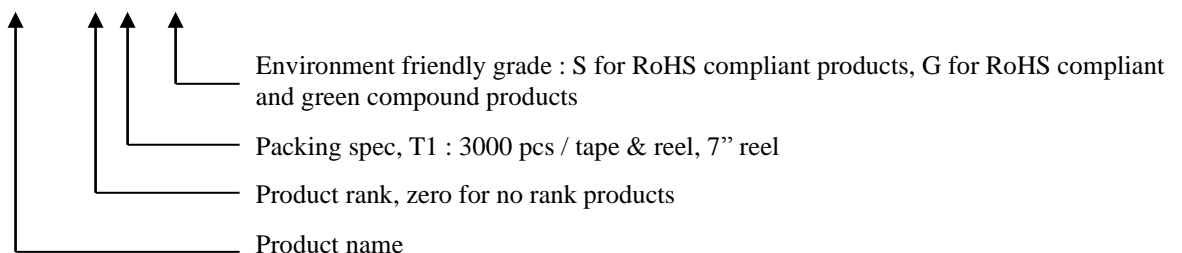


Outline



Ordering Information

Device	Package	Shipping
MTAK6S6R-0-T1-G	SOT-363 (Pb-free lead plating & halogen-free package)	3000 pcs / Tape & Reel





The following characteristics apply to both Tr1 and Tr2
Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	BV _{DSS}	60	V
Gate-Source Voltage	V _{GS}	±20	
Continuous Drain Current	I _D	250	mA
Pulsed Drain Current	I _{DM}	800 *1	
Total Power Dissipation	P _D	200 *2	mW
ESD susceptibility	V _{ESD}	2000 *3	V
Operating Junction and Storage Temperature Range	T _j ; T _{stg}	-55~+150	°C

Note : *1. Pulse Width ≤ 10μs, Duty cycle ≤ 1%
 *2. With each pin mounted on the recommended lands.
 *3. Human body model, 1.5kΩ in series with 100pF

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Channel-to-ambient, max	*R _{th,ch-a}	625 (total)	°C/W
		800 (per element)	

Note : With each pin mounted on the recommended lands.

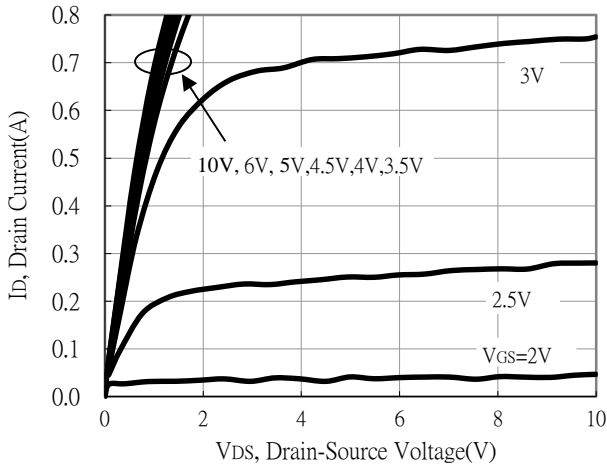
Electrical Characteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	60	-	-	V	V _{GS} =0V, I _D =250μA
V _{GS(th)}	0.5	-	1.5		I _D =250μA, V _{DS} =V _{GS}
I _{GSS}	-	-	±10	μA	V _{GS} =±16V, V _{DS} =0V
I _{DSS}	-	-	1		V _{DS} =60V, V _{GS} =0V
R _{DS(ON)}	-	1.3	3	Ω	V _{GS} =4.5V, I _D =200mA
	-	1.7	5.1		V _{GS} =2.5V, I _D =100mA
G _{FS}	100	322	-	mS	V _{DS} =5V, I _D =100mA
Dynamic					
C _{iss}	-	25.6	-	pF	V _{DS} =30V, V _{GS} =0V, f=1MHz
C _{oss}	-	8.8	-		
C _{rss}	-	6.8	-		
t _{d(on)}	-	5.8	-	ns	V _{DD} =30V, I _D =200mA, V _{GS} =10V, R _G =25Ω
t _r	-	0.8	-		
t _{d(off)}	-	19	-		
t _f	-	1.4	-		
Q _g	-	0.82	-	nC	V _{DS} =48V, I _D =0.5A, V _{GS} =4.5V
Q _{gs}	-	0.34	-		
Q _{gd}	-	0.2	-		
Source-Drain Diode					
*V _{SD}	-	0.74	1.2	V	V _{GS} =0V, I _S =100mA
*t _{rr}	-	8.2	-	ns	I _F =0.5A, dI _F /dt=100A/μs
*Q _{rr}	-	2.3	-	nC	

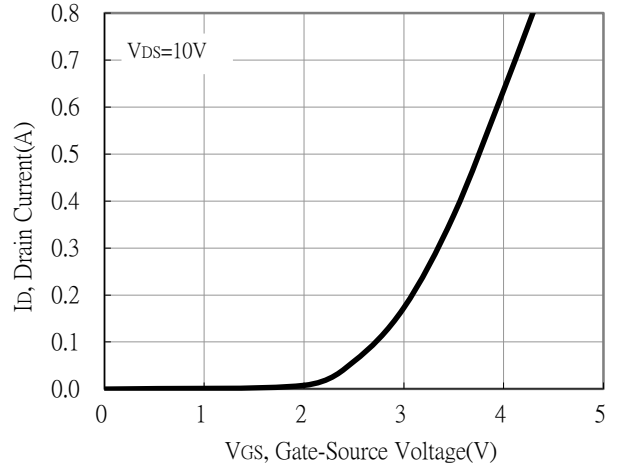
*Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%

Typical Characteristics

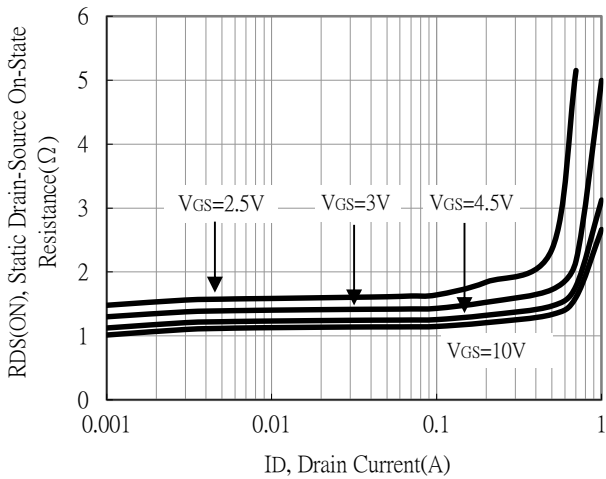
Typical Output Characteristics



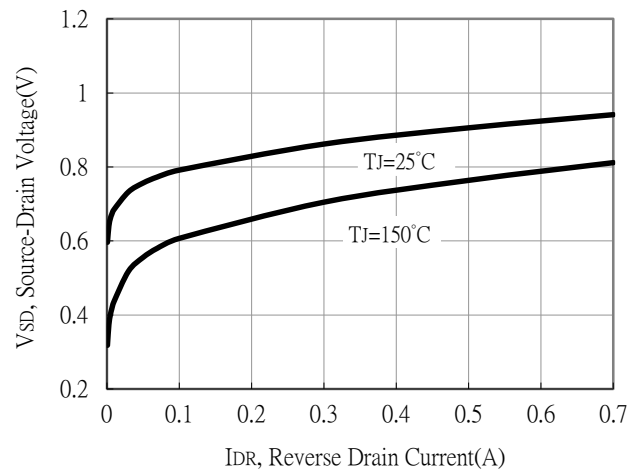
Typical Transfer Characteristics



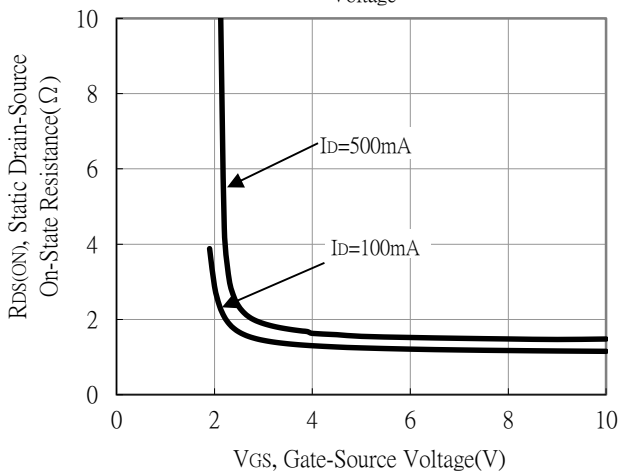
Static Drain-Source On-State resistance vs Drain Current



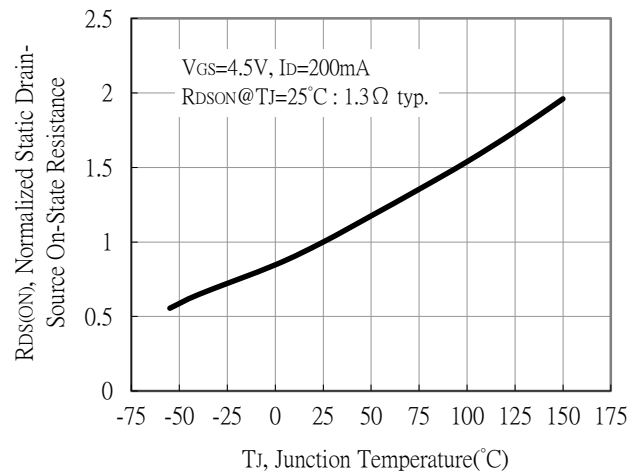
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

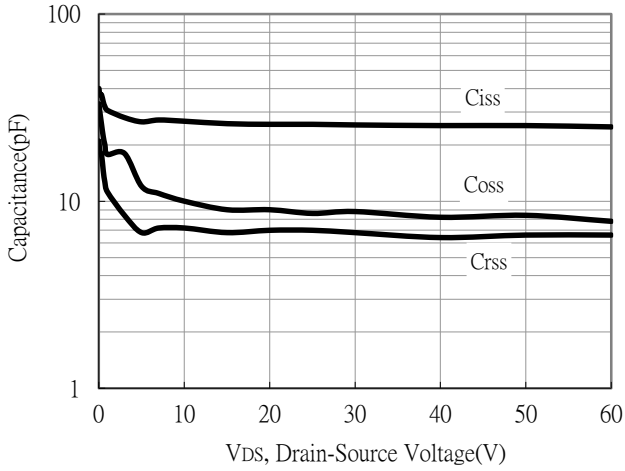


Drain-Source On-State Resistance vs Junction Temperature

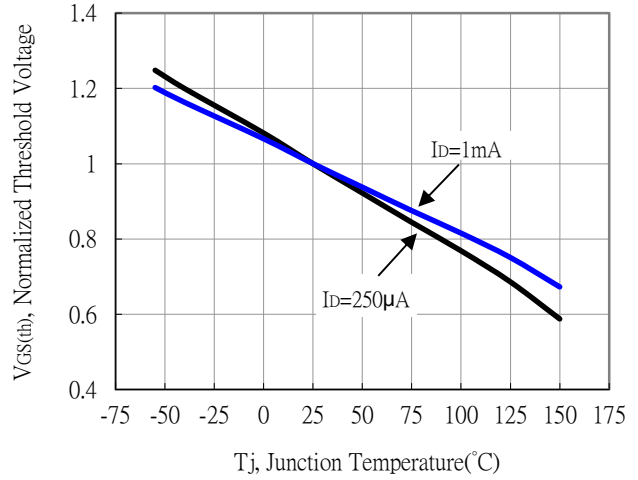


Typical Characteristics(Cont.)

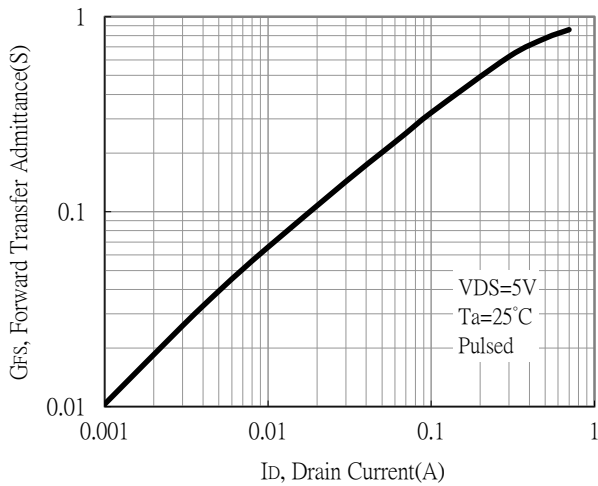
Capacitance vs Drain-to-Source Voltage



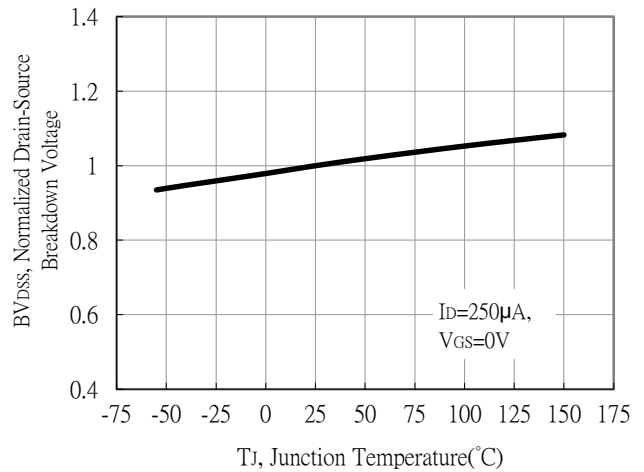
Threshold Voltage vs Junction Temperature



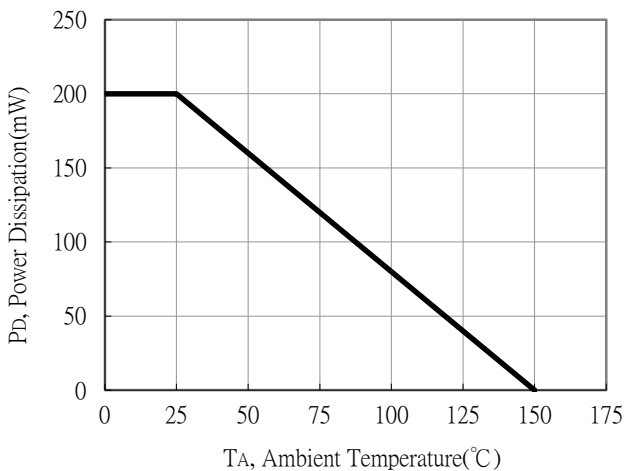
Forward Transfer Admittance vs Drain Current



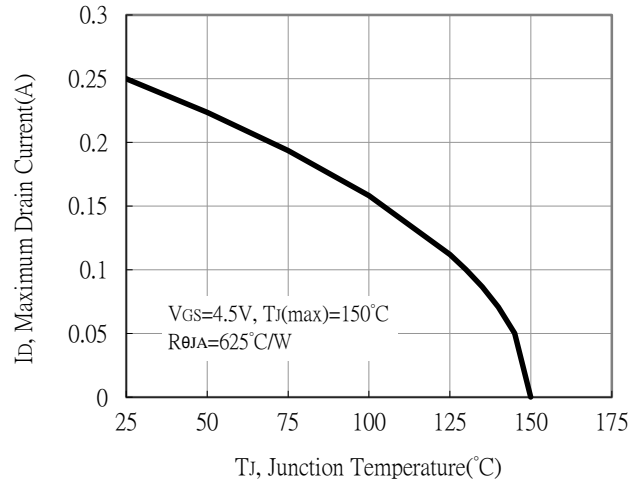
Brekdown Voltage vs Ambient Temperature



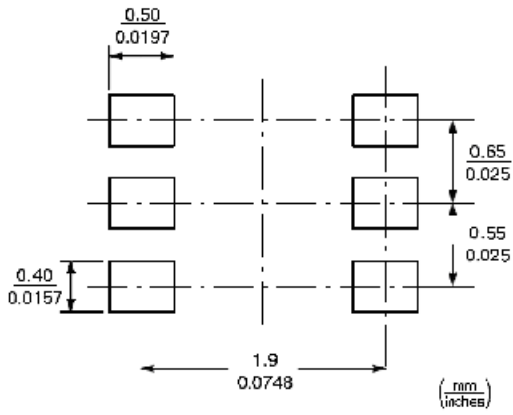
Power Derating Curve



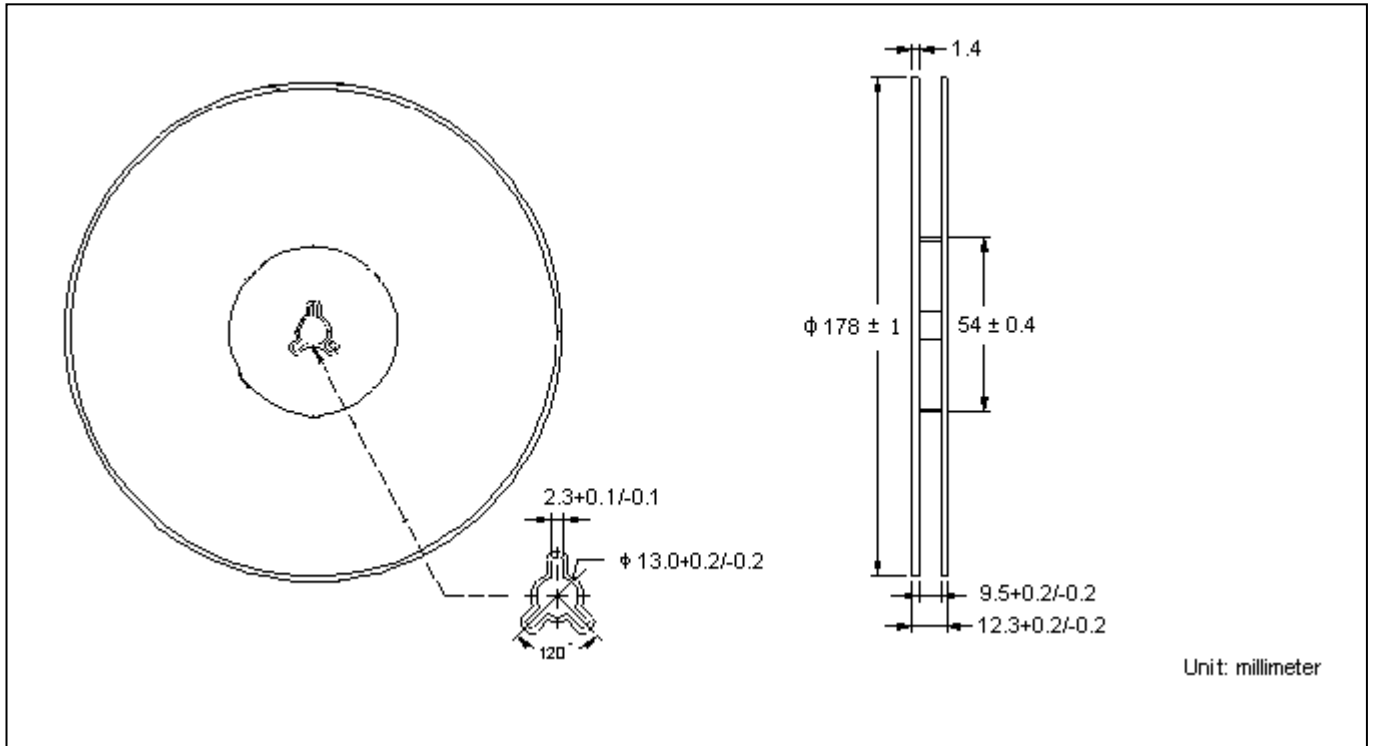
Maximum Drain Current vs Junction Temperature



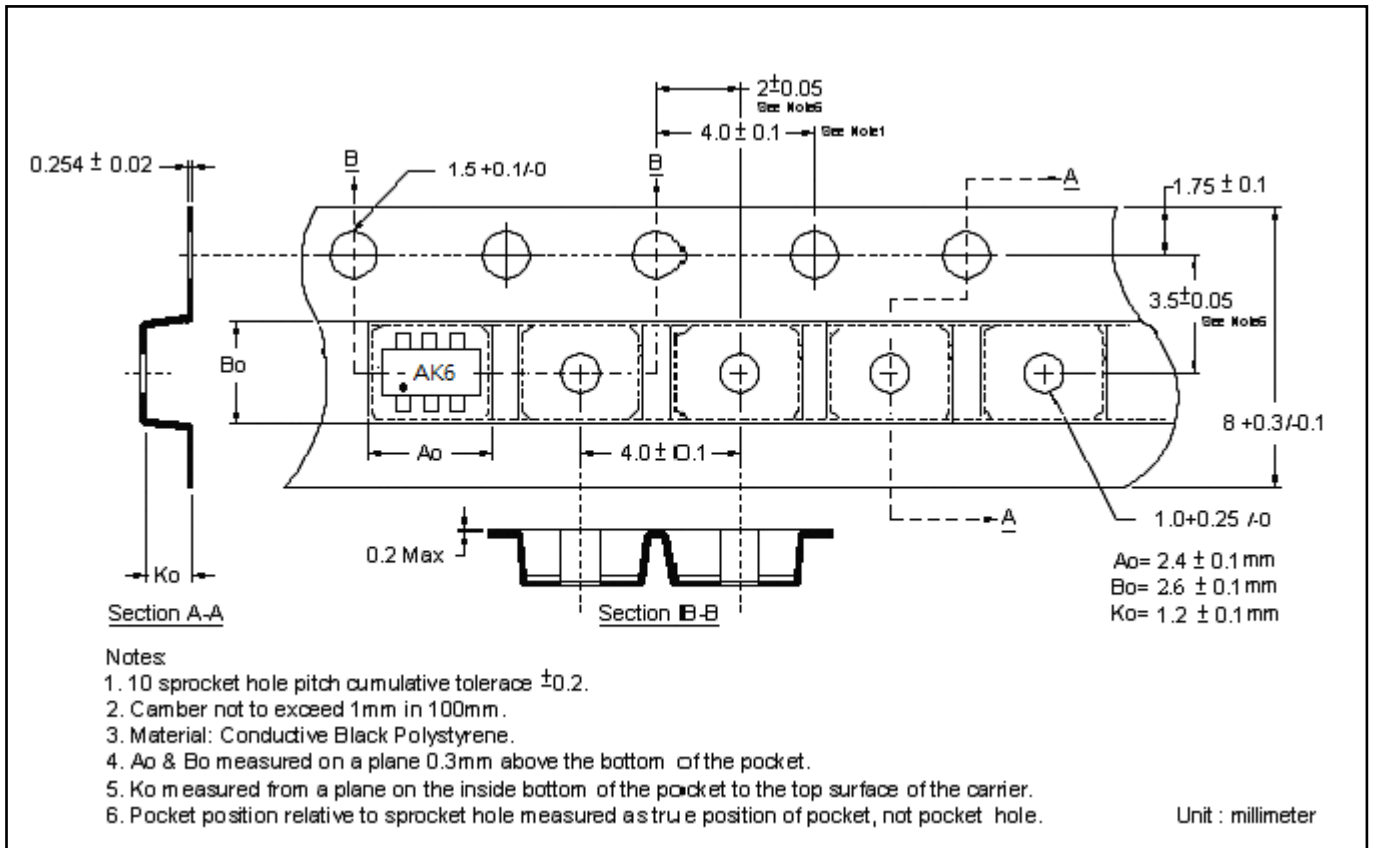
Recommended Soldering Footprint



Reel Dimension



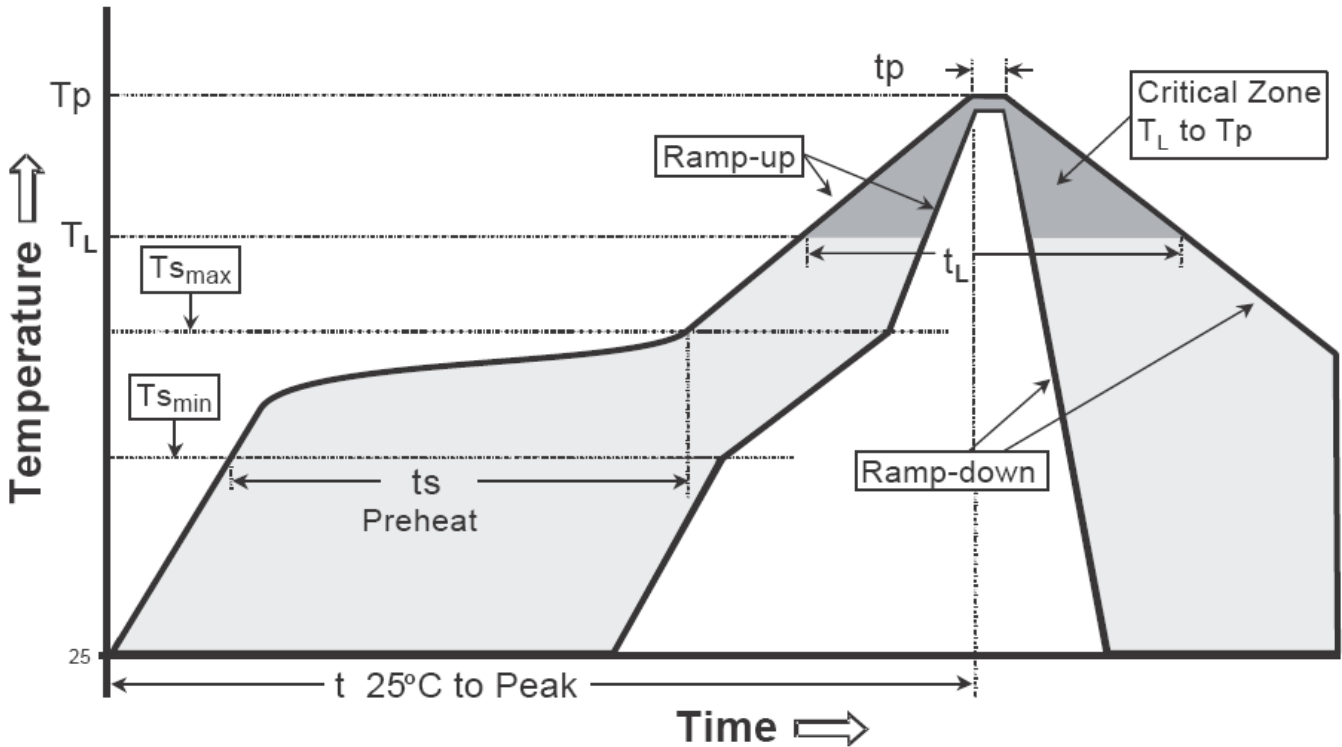
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

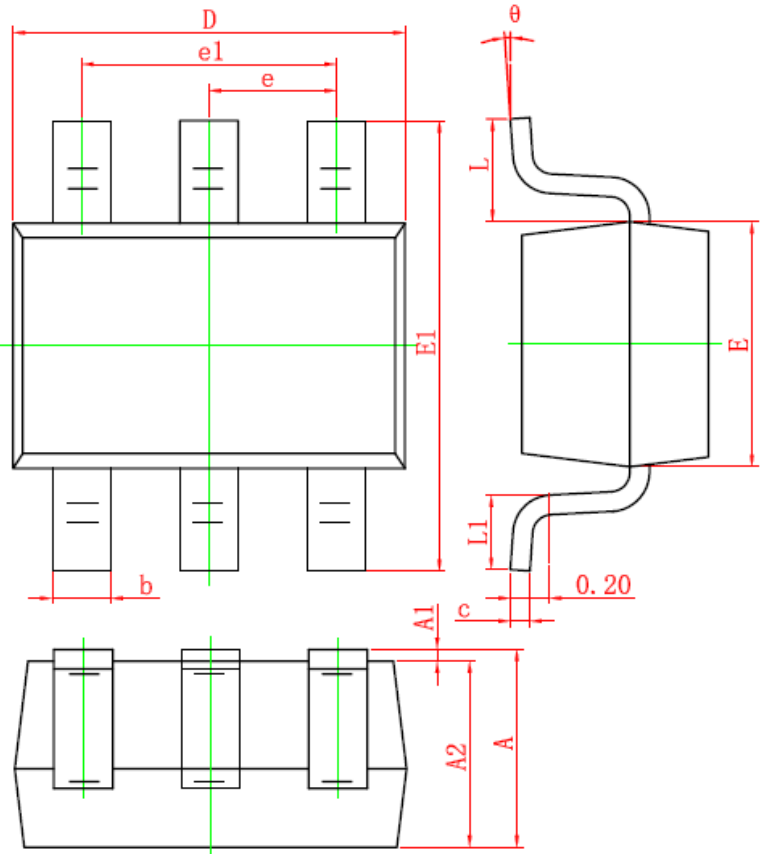
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

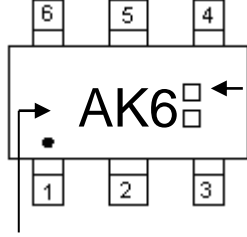
Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-363 Dimension



The diagram shows three views of the SOT-363 package: a top view, a side view, and a bottom view. Dimensions are labeled in red: D (total width), e1 (lead pitch), e (lead width), E1 (total height), E (package height), L (lead length), L1 (lead thickness), b (lead width), A1 (lead height), c (lead thickness), A2 (lead height), and A (total height). The lead angle is labeled as θ. A 0.20 mm dimension is shown for the lead thickness at the base.

Marking:



Date Code:
 Year + Month
 Year : 9→2019,
 0→2020, ..., etc
 Month : 1→Jan
 2→Feb, ..., 9→
 Sep, A→Oct, B
 →Nov, C→Dec

Device Code

6-Lead SOT-363R Plastic Surface Mounted Package
 CYStek Package Code: S6R

Style:
 Pin 1. Source1 (S1)
 Pin 2. Gate1 (G1)
 Pin 3. Drain2 (D2)
 Pin 4. Source2 (S2)
 Pin 5. Gate2 (G2)
 Pin 6. Drain1 (D1)

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.900	1.100	0.035	0.043	E1	2.150	2.450	0.085	0.096
A1	0.000	0.100	0.000	0.004	e	0.650	TYP	0.026	TYP
A2	0.900	1.000	0.035	0.039	e1	1.200	1.400	0.047	0.055
b	0.150	0.350	0.006	0.014	L	0.525	REF	0.021	REF
c	0.080	0.150	0.003	0.006	L1	0.260	0.460	0.010	0.018
D	2.000	2.200	0.079	0.087	θ	0°	8°	0°	8°
E	1.150	1.350	0.045	0.053					

Notes : 1.Controlling dimension : millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

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