

**P-Channel Enhancement Mode Power MOSFET**

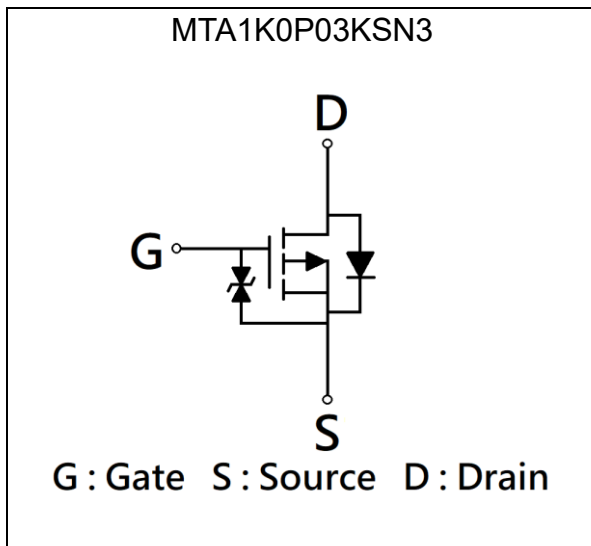
# MTA1K0P03KSN3

**Features**

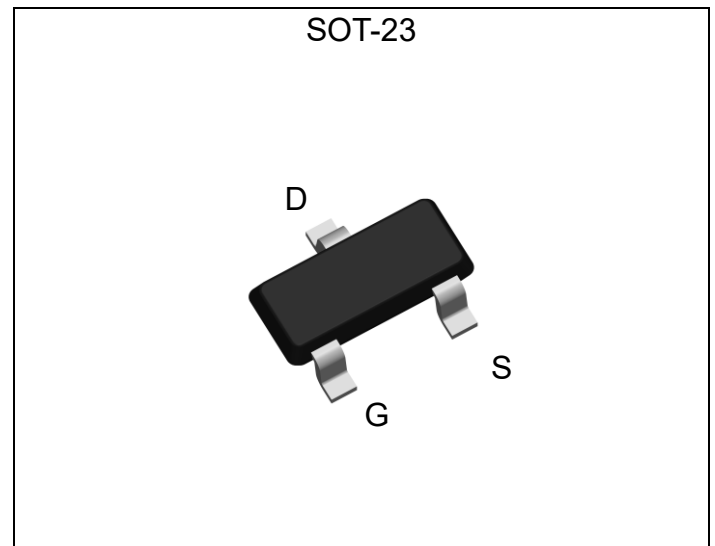
- Low On Resistance
- Low Gate Charge
- Fast Switching Characteristic
- ESD protected gate, typical 4kV (HBM)

$BV_{DSS}$	-30V
$I_D@V_{GS}=-4.5V, T_A=25^{\circ}C$	-0.56A
$R_{DS(ON)}$ typ. @ $V_{GS}=-4.5V, I_D=-0.2A$	$0.9\ \Omega$
$R_{DS(ON)}$ typ. @ $V_{GS}=-2.5V, I_D=-0.2A$	$1.1\ \Omega$
$R_{DS(ON)}$ typ. @ $V_{GS}=-1.8V, I_D=-10mA$	$1.3\ \Omega$

**Equivalent Circuit**

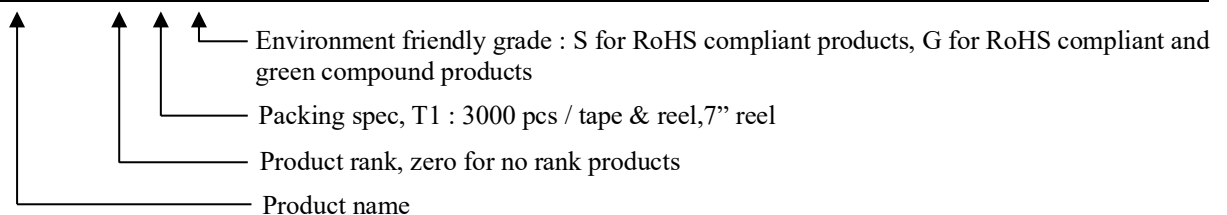


**Outline**



**Ordering Information**

Device	Package	Shipping
MTA1K0P03KSN3-0-T1-G	SOT-23 (Pb-free lead plating and halogen-free package)	3000 pcs / tape & reel



**Absolute Maximum Ratings (T<sub>A</sub>=25°C)**

Parameter	Symbol	Limits	Unit	
Drain-Source Voltage	V <sub>DS</sub>	-30	V	
Gate-Source Voltage	V <sub>GS</sub>	±8		
Continuous Drain Current @ V <sub>GS</sub> =-4.5V, T <sub>A</sub> =25°C	I <sub>D</sub>	-0.56	A	
Continuous Drain Current @ V <sub>GS</sub> =-4.5V, T <sub>A</sub> =70°C		-0.45		
Pulsed Drain Current *a	I <sub>DM</sub>	-2.2		
Continuous Body Diode Forward Current @ T <sub>A</sub> =25°C	I <sub>S</sub>	-0.56		
ESD susceptibility *b	V <sub>ESD</sub>	4000	V	
Total Power Dissipation	P <sub>D</sub>	T <sub>A</sub> =25°C	0.69	W
		T <sub>A</sub> =70°C	0.44	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55~+150	°C	

**Thermal Data**

Parameter	Symbol	Steady State	Unit
Thermal Resistance, Junction-to-ambient	R <sub>θJA</sub>	181	°C/W

Note:

\*a. Repetitive rating, pulse width limited by junction temperature T<sub>J</sub>(MAX)=150°C. Ratings are based on low frequency and low duty cycles to keep initial T<sub>J</sub>=25°C.

\*b. Human body model, 1.5kΩ in series with 100pF



**Electrical Characteristics (T<sub>A</sub>=25°C, unless otherwise specified)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
<b>Static</b>					
BV <sub>DSS</sub>	-30	-	-	V	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA
V <sub>GS(th)</sub>	-0.4	-	-1.2		V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA
G <sub>FS</sub>	-	0.8	-	S	V <sub>DS</sub> =-5V, I <sub>D</sub> =-0.2A
I <sub>GSS</sub>	-	-	±10	μA	V <sub>GS</sub> =±8V, V <sub>DS</sub> =0V
I <sub>DSS</sub>	-	-	-1		V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V
R <sub>DS(ON)</sub>	-	0.9	1.3	Ω	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-0.2A
	-	1.1	1.7		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-0.2A
	-	1.3	2.7		V <sub>GS</sub> =-1.8V, I <sub>D</sub> =-10mA
<b>Dynamic</b>					
C <sub>iss</sub>	-	46	-	pF	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1MHz
C <sub>oss</sub>	-	13	-		
C <sub>rss</sub>	-	10	-		
Q <sub>g</sub> *1, 2	-	1	-	nC	V <sub>DS</sub> =-20V, I <sub>D</sub> =-0.4A, V <sub>GS</sub> =-4.5V
Q <sub>gs</sub> *1, 2	-	0.2	-		
Q <sub>gd</sub> *1, 2	-	0.2	-		
t <sub>d(ON)</sub> *1, 2	-	13	-	ns	V <sub>DS</sub> =-15V, I <sub>D</sub> =-0.4A, V <sub>GS</sub> =-4.5V, R <sub>GS</sub> =1 Ω
t <sub>r</sub> *1, 2	-	21	-		
t <sub>d(OFF)</sub> *1, 2	-	44	-		
t <sub>f</sub> *1, 2	-	29	-		
<b>Source-Drain Diode</b>					
V <sub>SD</sub> *1	-	-0.85	-1.2	V	I <sub>S</sub> =-0.2A, V <sub>GS</sub> =0V
t <sub>rr</sub>	-	25	-	ns	I <sub>F</sub> =-0.5A, dI <sub>F</sub> /dt=100A/μs
Q <sub>rr</sub>	-	5	-	nC	

Note:

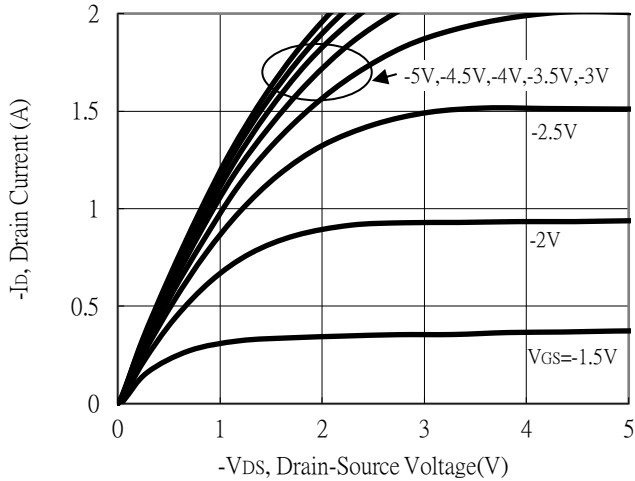
\*1. Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

\*2. Independent of operating temperature

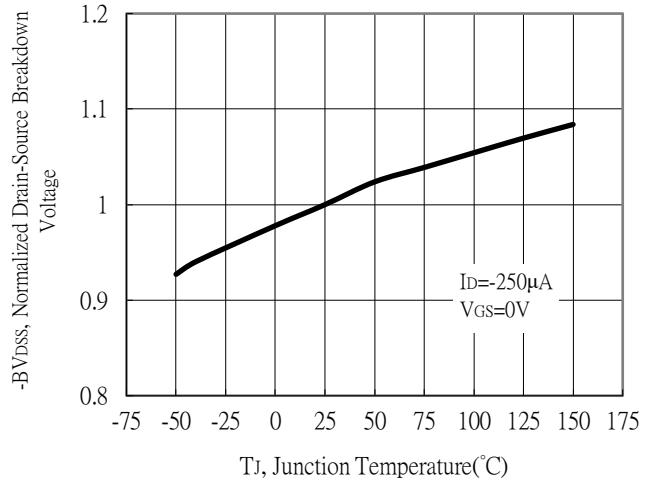


**Typical Characteristics**

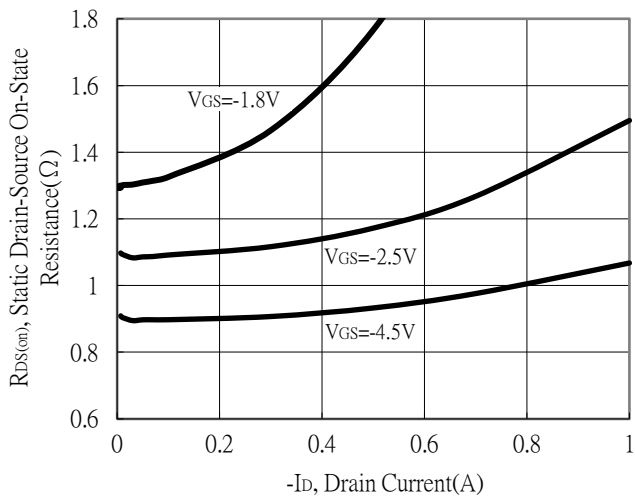
Typical Output Characteristics



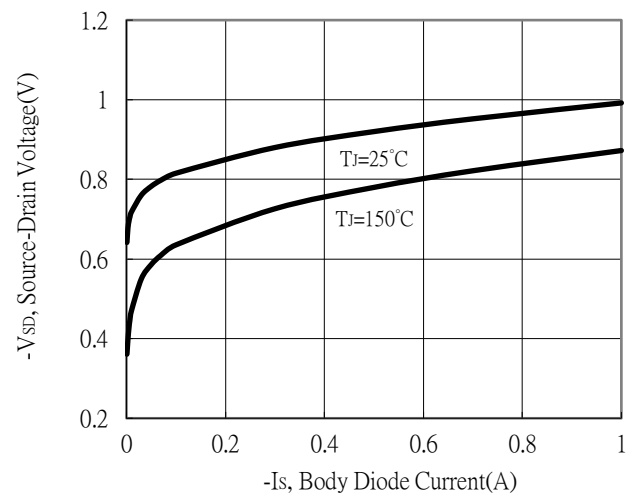
Breakdown Voltage vs Ambient Temperature



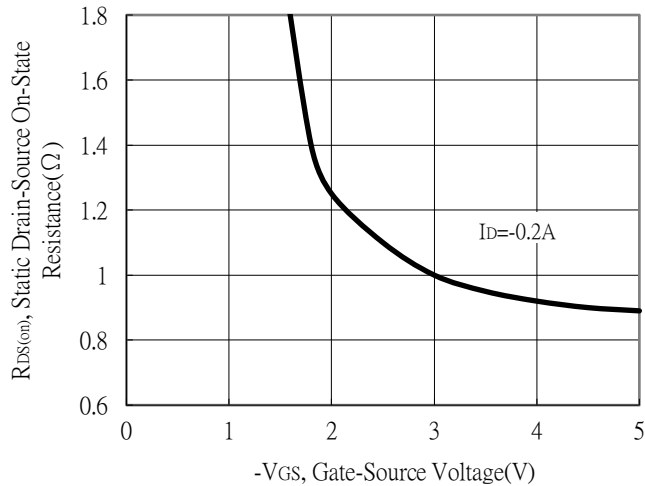
Static Drain-Source On-State resistance vs Drain Current



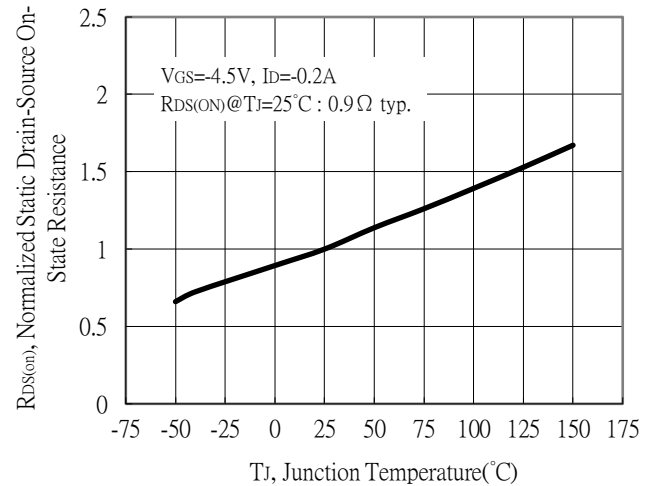
Body Diode Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

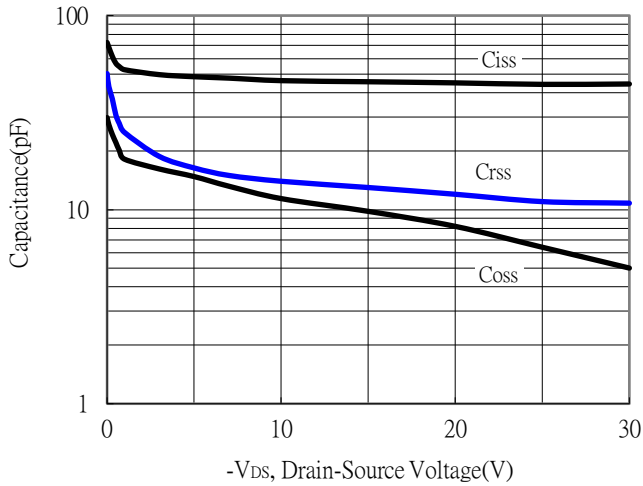


Drain-Source On-State Resistance vs Junction Temperature

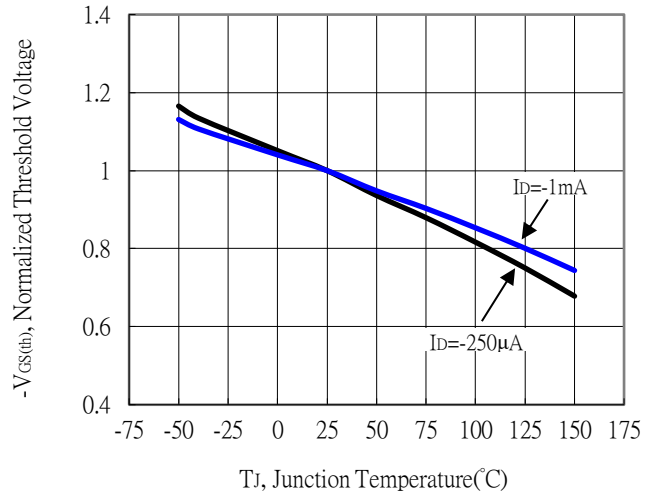


**Typical Characteristics (Cont.)**

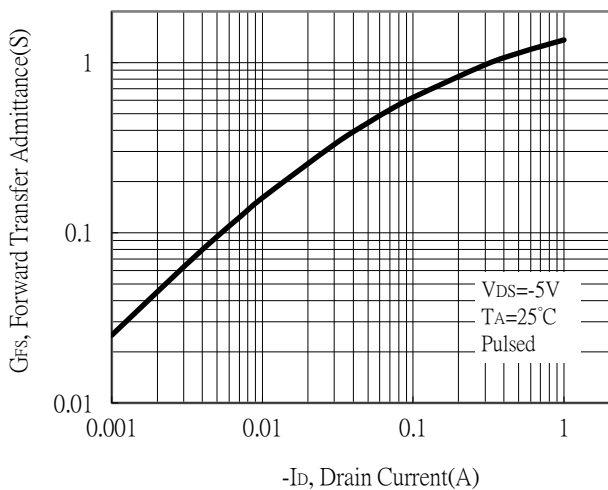
Capacitance vs Drain-to-Source Voltage



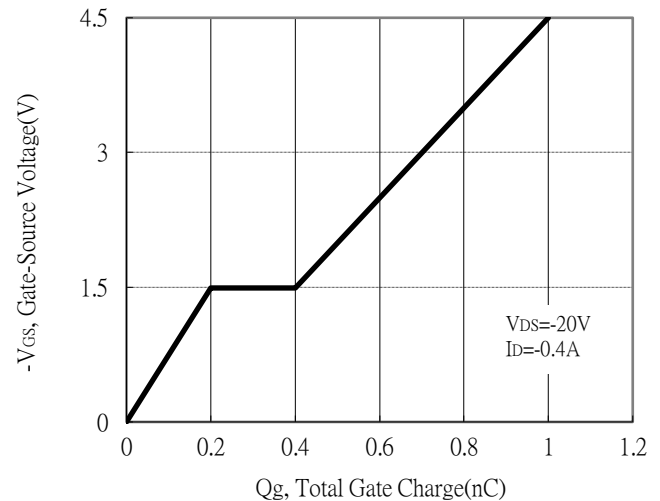
Threshold Voltage vs Junction Temperature



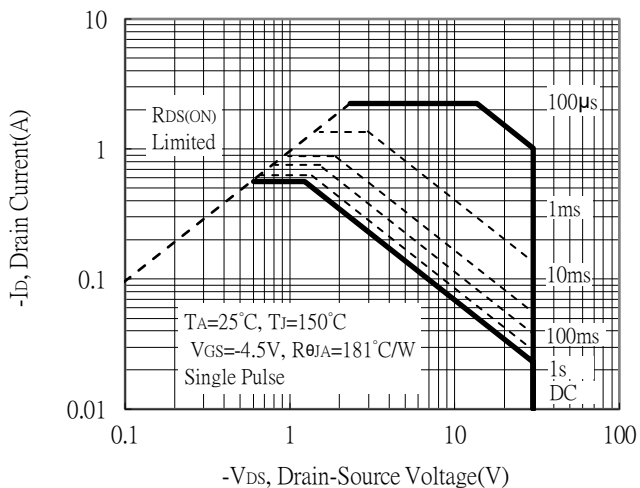
Forward Transfer Admittance vs Drain Current



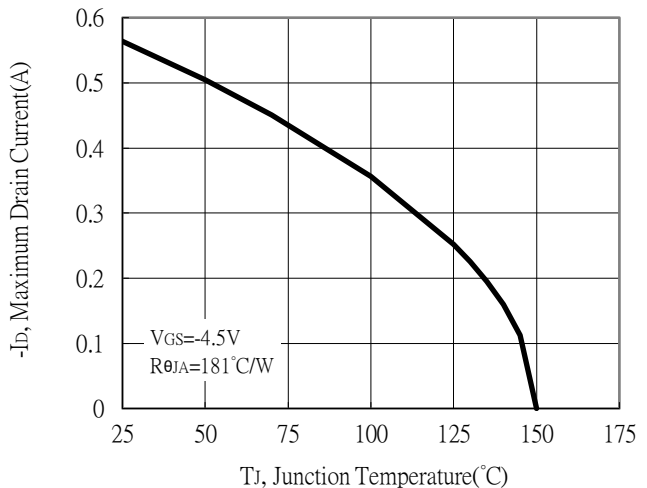
Gate Charge Characteristics



Maximum Safe Operating Area

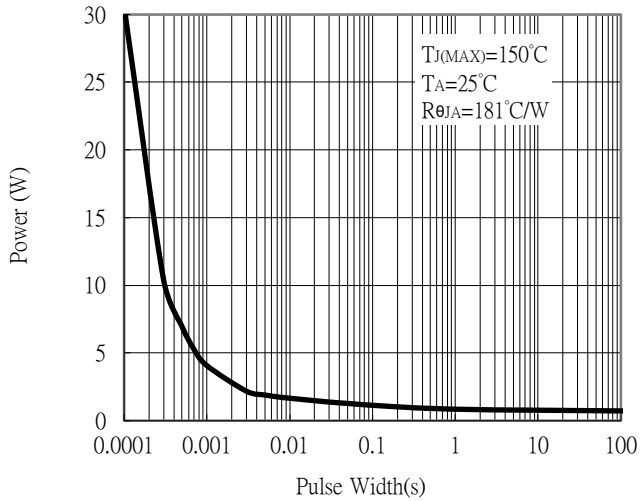


Maximum Drain Current vs Junction Temperature

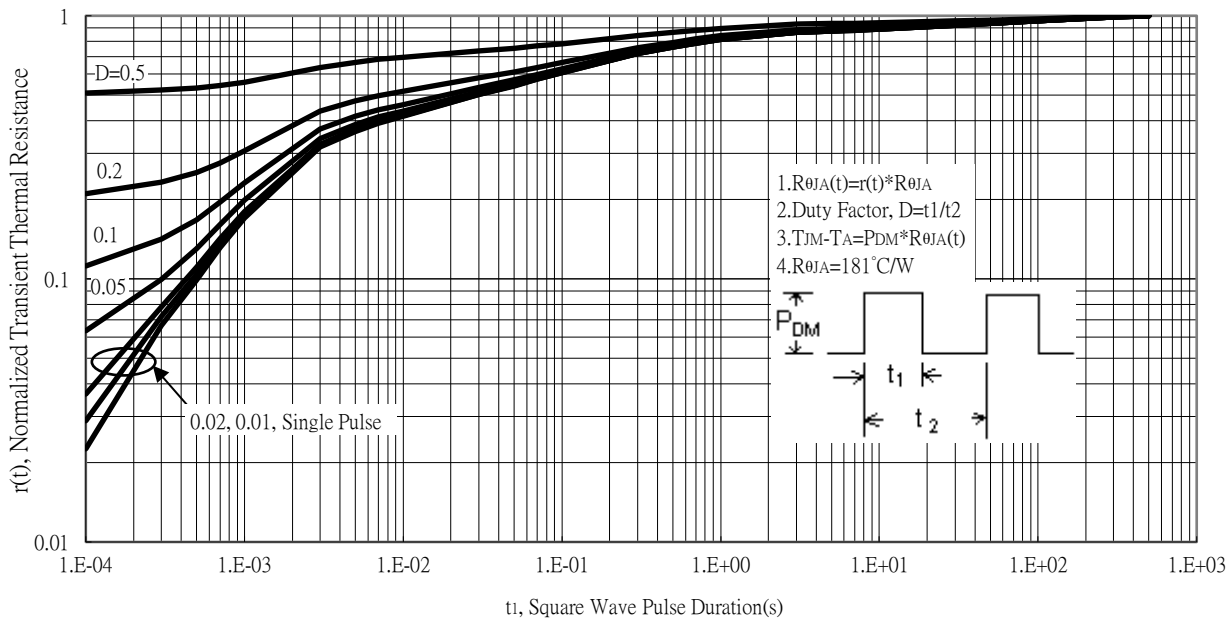


**Typical Characteristics (Cont.)**

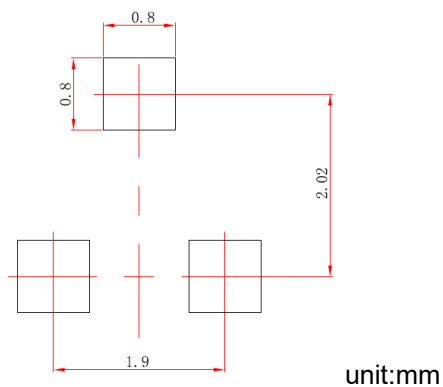
Single Pulse Power Rating, Junction to Ambient



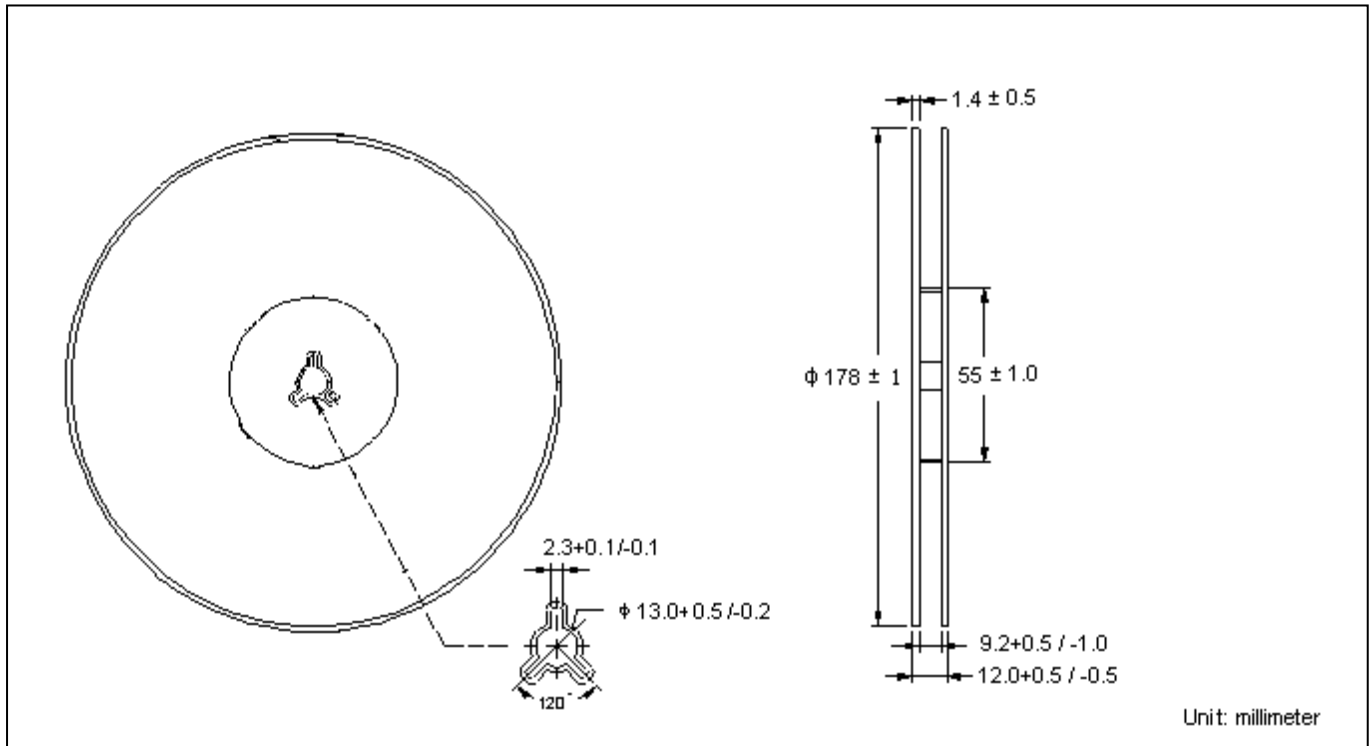
Transient Thermal Response Curves



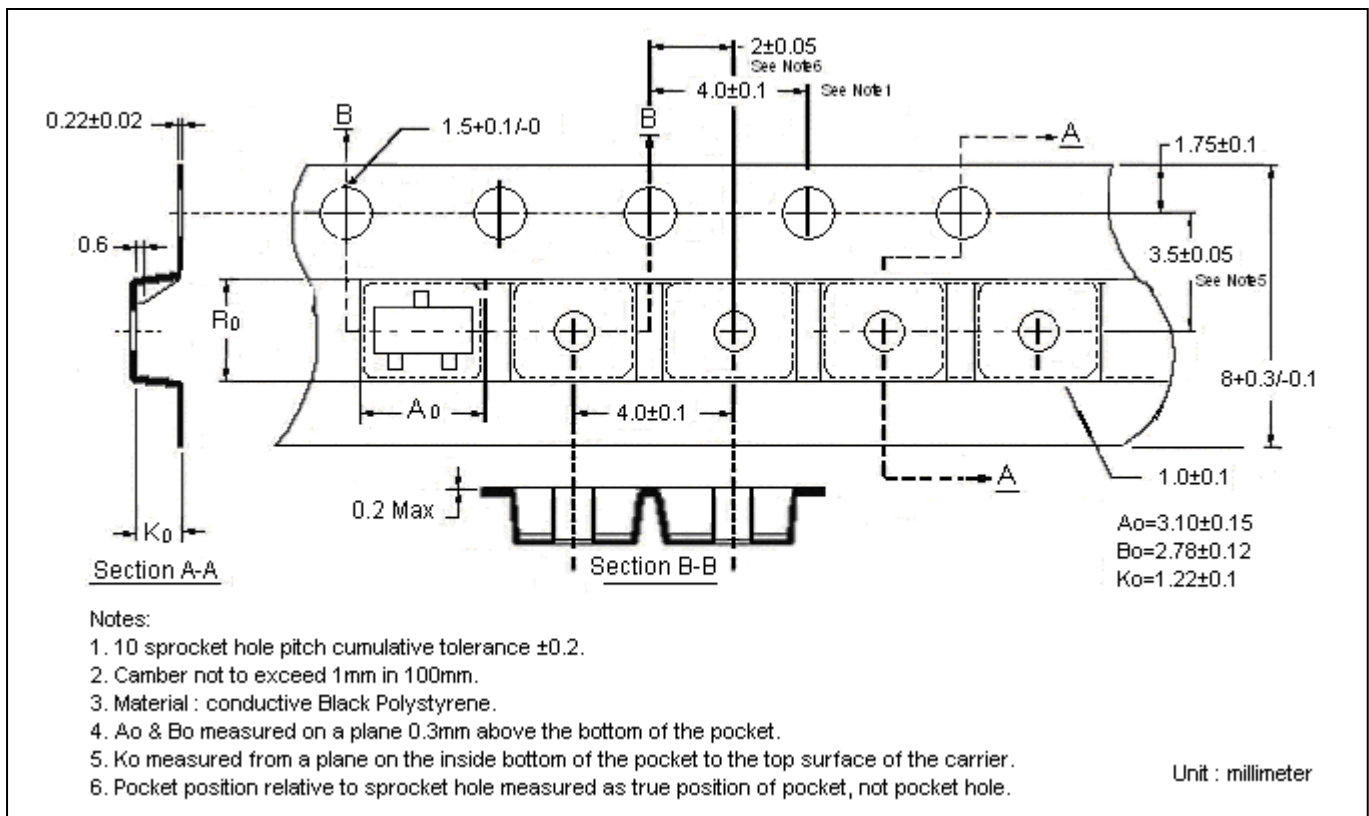
**Recommended Soldering Footprint**



**Reel Dimension**



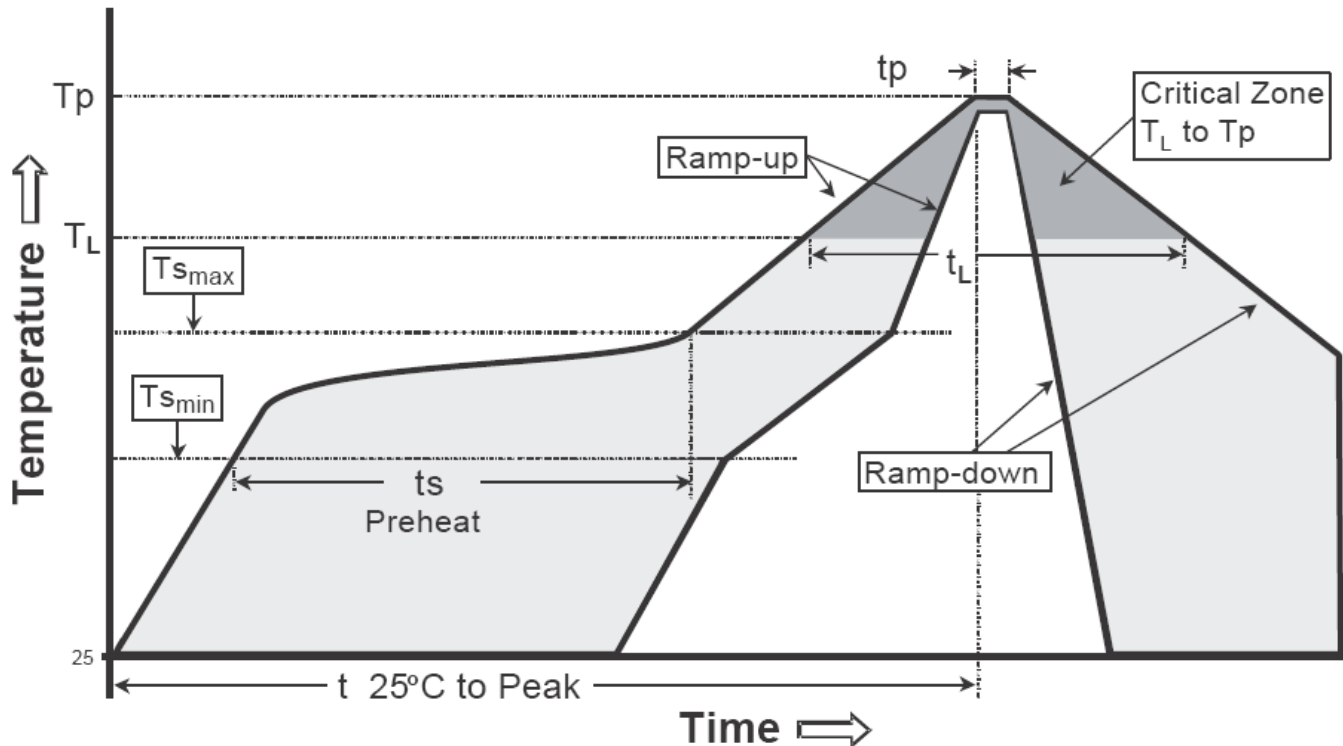
**Carrier Tape Dimension**



**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

**Recommended temperature profile for IR reflow**

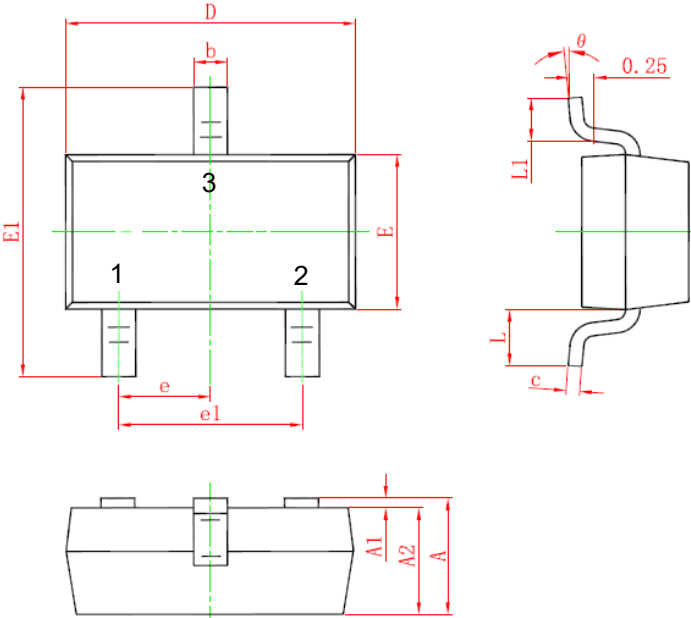


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T <sub>s min</sub> )	100°C	150°C
-Temperature Max(T <sub>s max</sub> )	150°C	200°C
-Time(t <sub>s min</sub> to t <sub>s max</sub> )	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T <sub>L</sub> )	183°C	217°C
- Time (t <sub>L</sub> )	60-150 seconds	60-150 seconds
Peak Temperature(T <sub>P</sub> )	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

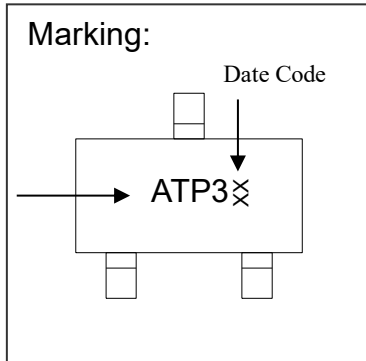


**SOT-23 Dimension**



The diagram shows three views of the SOT-23 package: a top view with dimensions D, b, E1, E, e, and e1; a side view with dimensions L1, c, and  $\theta$  (0.25); and a bottom view with dimensions A1, A2, and A.

**Marking:**



The marking diagram shows a rectangular package with three leads. The top lead is labeled 'Date Code'. The bottom lead is labeled 'Device Code' and points to the marking 'ATP3' followed by a crossed-circle symbol.

3-Lead SOT-23 Plastic Surface Mounted Package  
 CYStek Package Code: N3

Style: Pin 1.Gate 2.Source 3.Drain

Date Code: Year+Month  
 Year: 3→2003, 4→2004  
 Month: 1→1, 2→2, . . .  
 9→9, A→10, B→11, C→12

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.035	0.045	0.900	1.150	E1	0.089	0.100	2.250	2.550
A1	0.000	0.004	0.000	0.100	e	0.037 TYP		0.950 TYP	
A2	0.035	0.041	0.900	1.050	e1	0.071	0.079	1.800	2.000
b	0.012	0.020	0.300	0.500	L	0.022 REF		0.550 REF	
c	0.003	0.006	0.080	0.150	L1	0.012	0.020	0.300	0.500
D	0.110	0.118	2.800	3.000	$\theta$	0°	8°	0°	8°
E	0.047	0.055	1.200	1.400					

**Notes:** 1.Controlling dimension: millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

**Important Notice:**

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.