

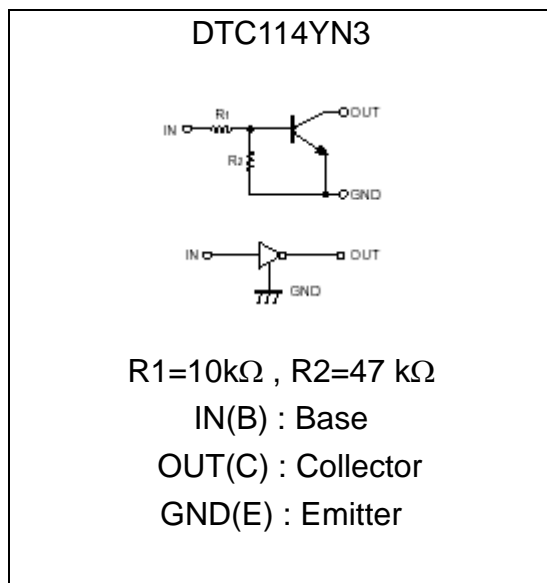
**NPN Digital Transistors (Built-in Resistors)**

# DTC114YN3

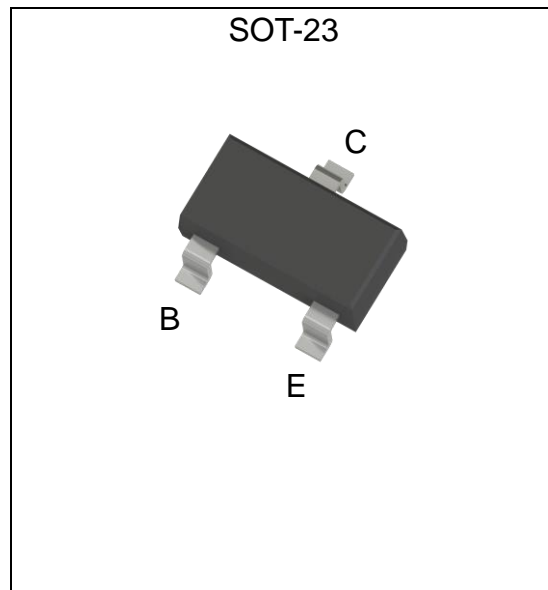
## Features

- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- The bias resistors consist of thin-film resistors with complete isolation to allow negative biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- Only the on/off conditions need to be set for operation, making device design easy.
- Complements the DTA114YN3

## Equivalent Circuit

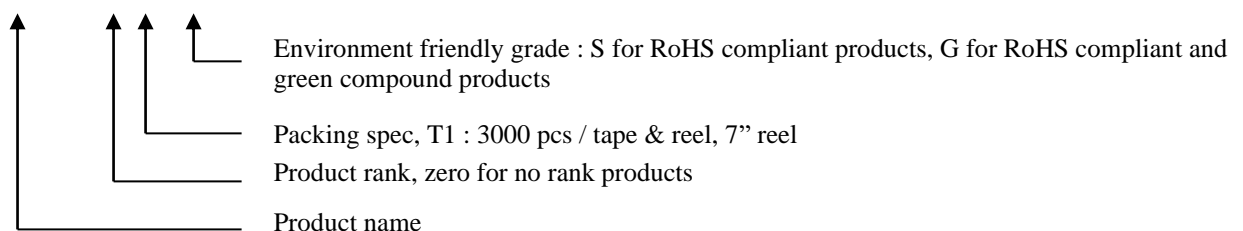


## Outline



## Ordering Information

Device	Package	Shipping
DTC114YN3-0-T1-G	SOT-23 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel



**Absolute Maximum Ratings (Ta=25°C)**

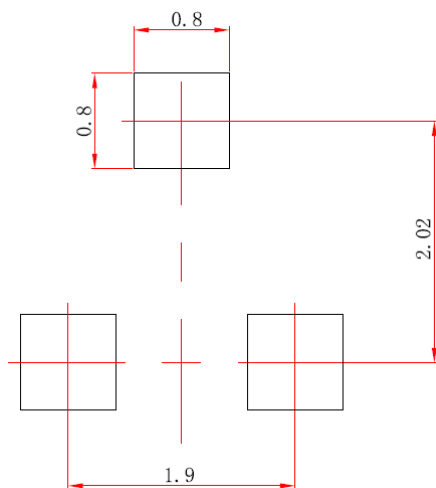
Parameter	Symbol	Limits	Unit
Supply Voltage	V <sub>CC</sub>	50	V
Input Voltage	V <sub>I</sub>	-6~+40	V
Output Current	I <sub>O</sub>	70	mA
	I <sub>O(max.)</sub>	100	mA
Power Dissipation	P <sub>d</sub>	200	mW
Junction Temperature	T <sub>j</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55~+150	°C

**Electrical Characteristics (Ta=25°C)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Voltage	V <sub>i(off)</sub>	-	-	0.3	V	V <sub>CC</sub> =5V, I <sub>O</sub> =100uA
	V <sub>i(on)</sub>	3	-	-	V	V <sub>O</sub> =0.3V, I <sub>O</sub> =1mA
Output Voltage	V <sub>O(on)</sub>	-	0.1	0.3	V	I <sub>O</sub> /I <sub>i</sub> =5mA/0.25mA
Input Current	I <sub>i</sub>	-	-	0.88	mA	V <sub>i</sub> =5V
Output Current	I <sub>O(off)</sub>	-	-	0.5	uA	V <sub>CC</sub> =50V, V <sub>i</sub> =0V
DC Current Gain	G <sub>i</sub>	68	-	-	-	V <sub>O</sub> =5V, I <sub>O</sub> =5mA
Input Resistance	R <sub>1</sub>	7	10	13	kΩ	-
Resistance Ratio	R <sub>2</sub> /R <sub>1</sub>	3.7	4.7	5.7	-	-
Transition Frequency	f <sub>T</sub>	-	250	-	MHz	V <sub>CE</sub> =10V, I <sub>C</sub> =5mA, f=100MHz *

\* Transition frequency of the device

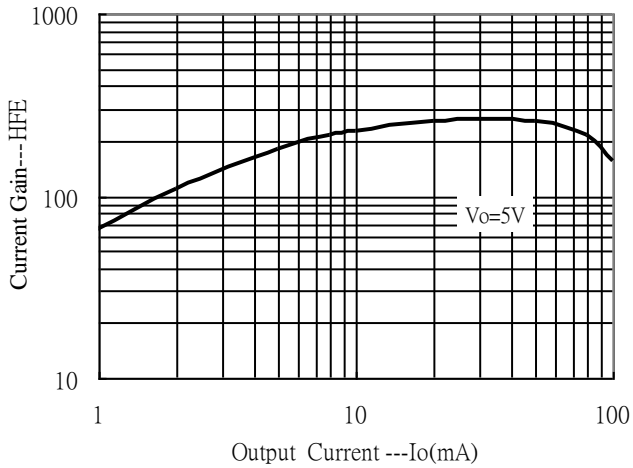
**Recommended Soldering Footprint**



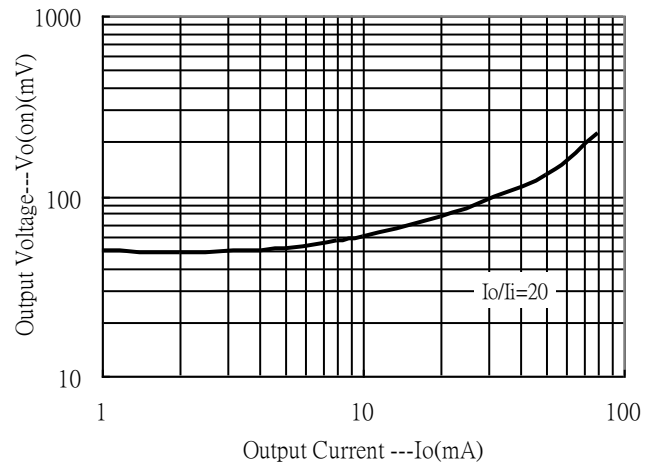
Unit : mm

## Typical Characteristics

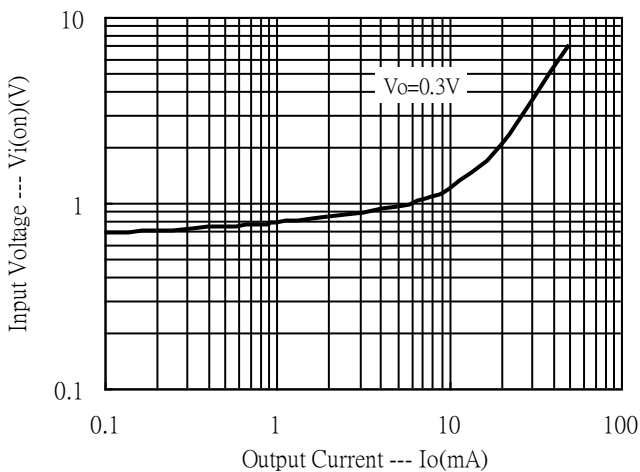
DC Current Gain vs Output Current



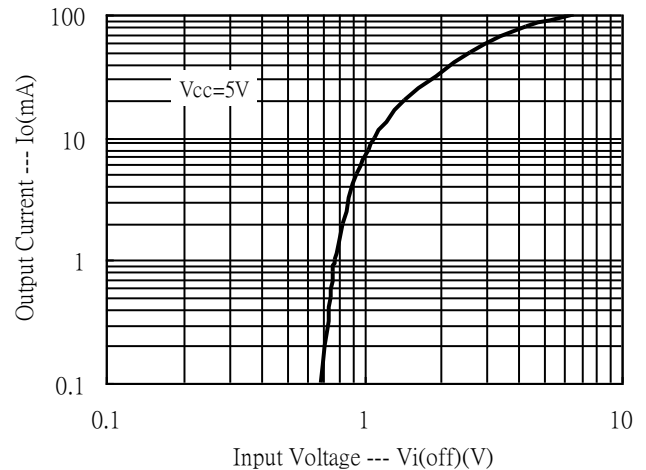
Output Voltage vs Output Current



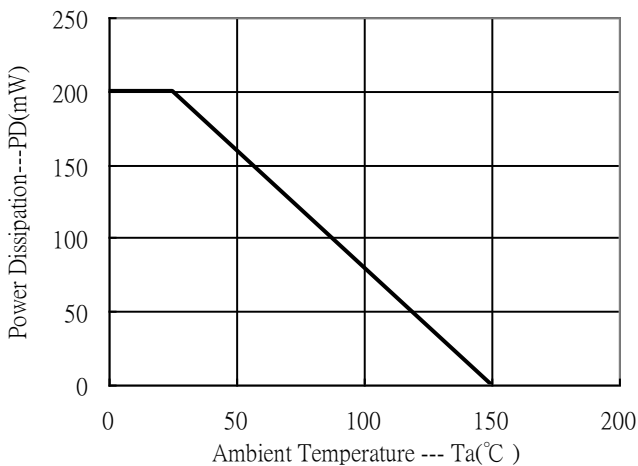
Input Voltage vs Output Current (ON Characteristics)



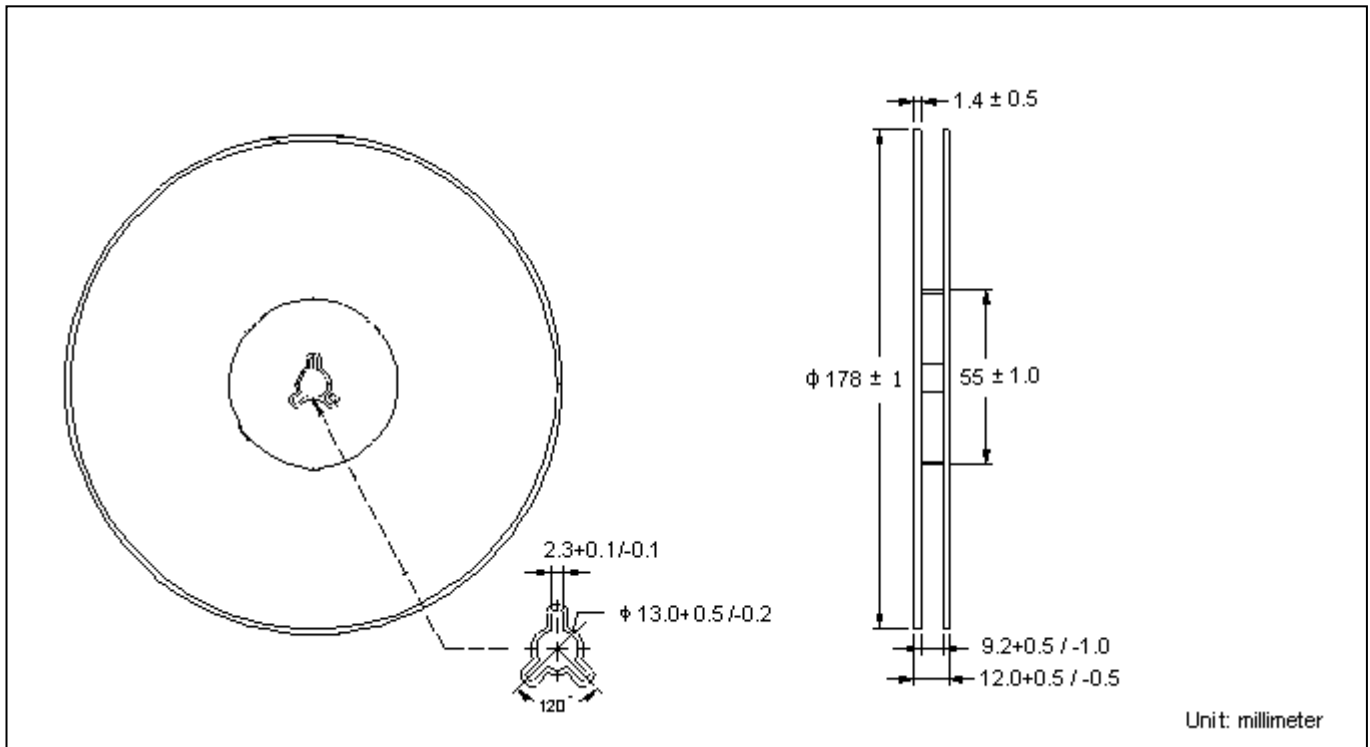
Output Current vs Input Voltage (OFF Characteristics)



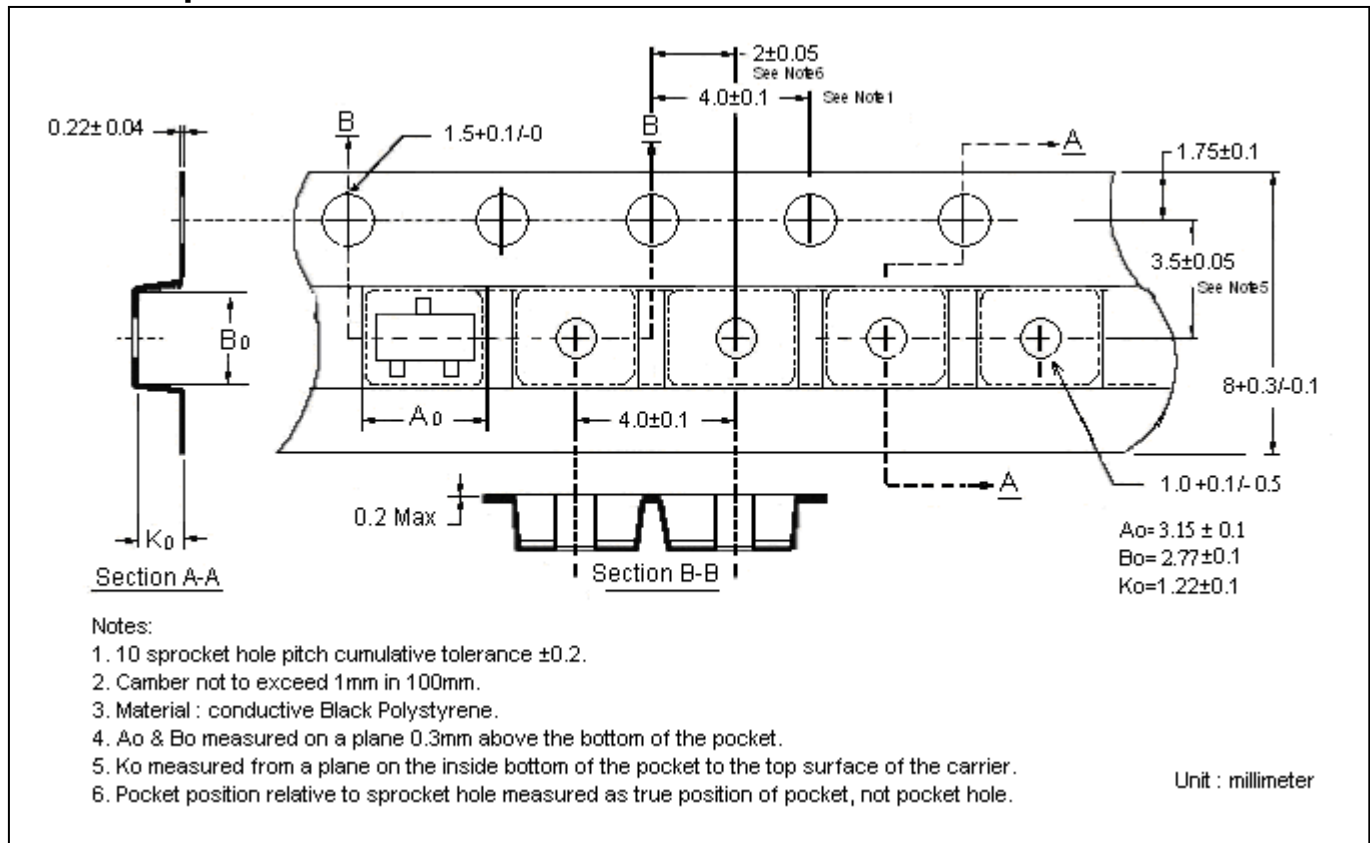
Power Derating Curve



**Reel Dimension**

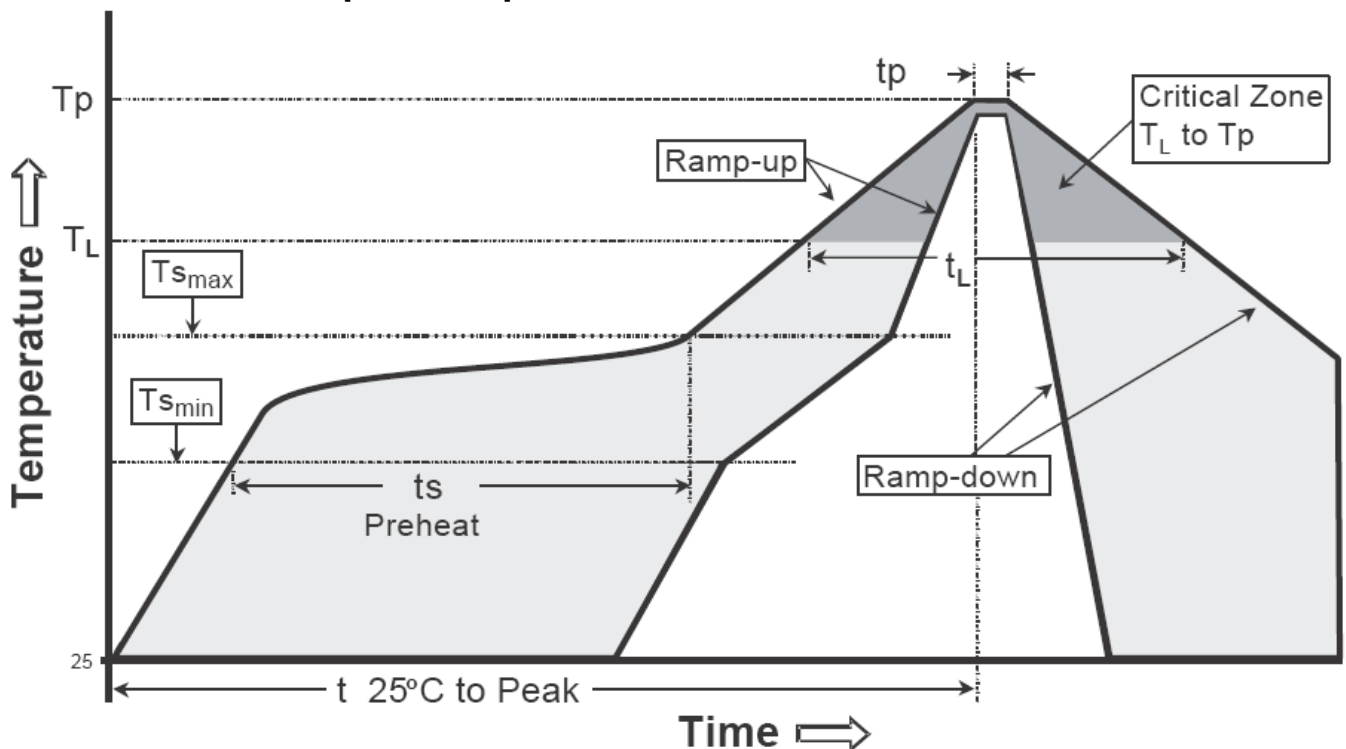


**Carrier Tape Dimension**



**Recommended wave soldering condition**

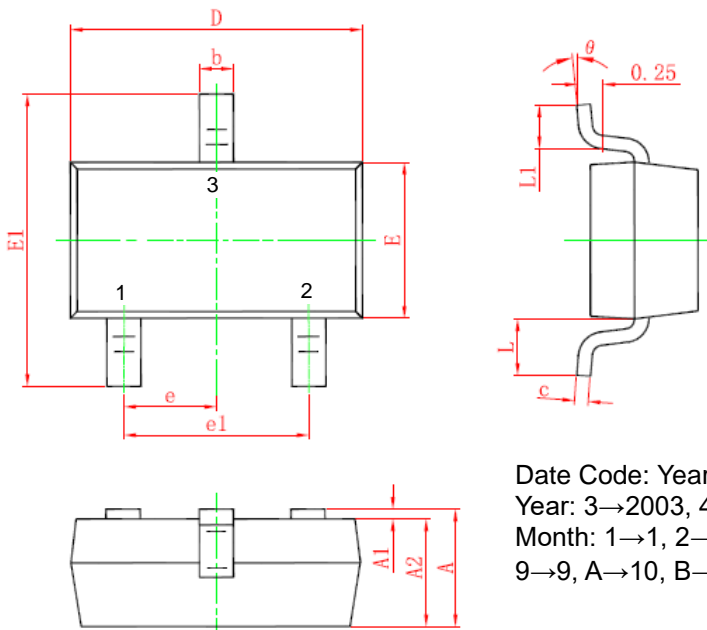
Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

**Recommended temperature profile for IR reflow**


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T <sub>s min</sub> )	100°C	150°C
-Temperature Max(T <sub>s max</sub> )	150°C	200°C
-Time(t <sub>s min</sub> to t <sub>s max</sub> )	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T <sub>L</sub> )	183°C	217°C
- Time (t <sub>L</sub> )	60-150 seconds	60-150 seconds
Peak Temperature(T <sub>p</sub> )	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(t <sub>p</sub> )	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

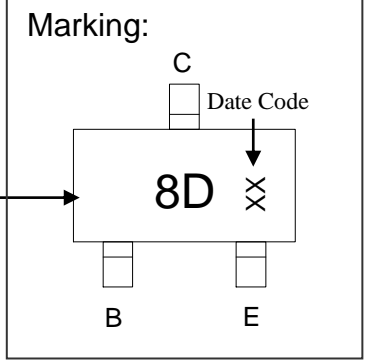
Note : All temperatures refer to topside of the package, measured on the package body surface.

**SOT-23 Dimension**



The diagram shows three views of the SOT-23 package: a top view with dimensions D, b, E1, E, 1, 2, 3, e, and e1; a side view with dimensions L, L1, c, and lead angle θ (0.25); and a perspective view with dimensions A1, A2, and A.

**Marking:**



The marking diagram shows a rectangular package with pins B, C, and E. Pin C is at the top, B at the bottom left, and E at the bottom right. The marking '8D' is in the center, with 'Date Code' above it and 'Device Code' to its left.

Style : Pin 1.Base 2.Emitter 3.Collector

3-Lead SOT-23 Plastic Surface Mounted Package  
 CYS Package Code: N3

**Date Code: Year+Month**  
 Year: 3→2003, 4→2004  
 Month: 1→1, 2→2, . . .  
 9→9, A→10, B→11, C→12

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.035	0.045	0.900	1.150	E1	0.089	0.100	2.250	2.550
A1	0.000	0.004	0.000	0.100	e	0.037 TYP.		0.950 TYP.	
A2	0.035	0.041	0.900	1.050	e1	0.071	0.079	1.800	2.000
b	0.012	0.020	0.300	0.500	L	0.022 REF.		0.550 REF.	
c	0.003	0.006	0.080	0.150	L1	0.012	0.020	0.300	0.500
D	0.110	0.118	2.800	3.000	θ	0°	8°	0°	8°
E	0.047	0.055	1.200	1.400					

- Notes:** 1.Controlling dimension: millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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