

Low Vcesat PNP Epitaxial Planar Transistor

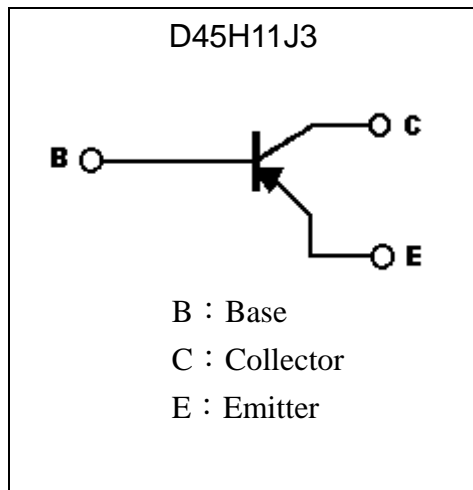
D45H11J3

BV_{CEO}	-80V
I_C	-8A
R_{CESAT}	75mΩ (typ.)

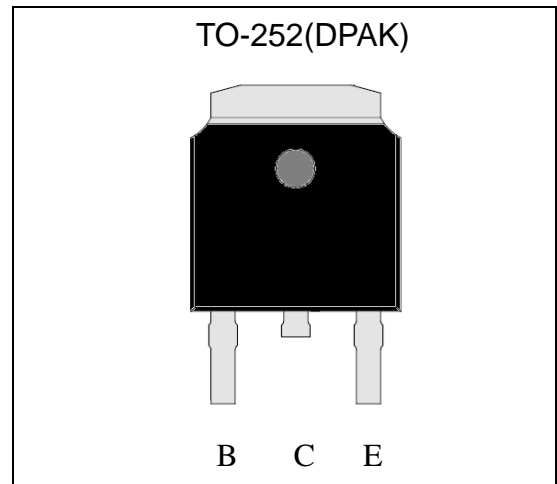
Features

- Low $V_{CE(sat)}$
- High BV_{CEO}
- Excellent current gain characteristics
- RoHS compliant package
- Pb-free lead-free and halogen-free package

Symbol

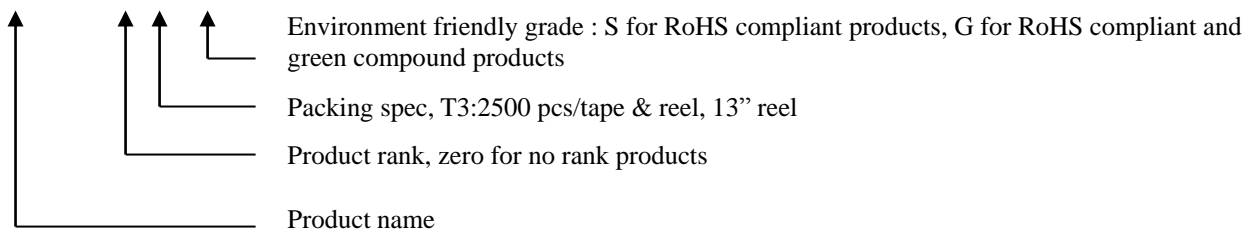


Outline



Ordering Information

Device	Package	Shipping
D45H11J3-0-T3-G	TO-252 (RoHS compliant and halogen-free package)	2500 pcs / Tape & Reel





Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V _{CBO}	-80	V
Collector-Emitter Voltage	V _{CEO}	-80	V
Emitter-Base Voltage	V _{EBO}	-5	V
Collector Current (DC)	I _C	-8	A
Collector Current (Pulse)	I _{CP}	-16 (Note 1)	
Power Dissipation @ T _A =25°C	P _D	1.75 (Note 2)	W
Power Dissipation @ T _C =25°C	P _D	20	
Thermal Resistance, Junction to Ambient	R _{θJA}	71.4 (Note 2)	°C/W
Thermal Resistance, Junction to Case	R _{θJC}	6.25	°C/W
Junction Temperature	T _J	150	°C
Storage Temperature	T _{stg}	-55~+150	°C

Note : 1. Single Pulse , Pw ≤ 380μs, Duty ≤ 2%.
 2. When mounted on a PCB with the minimum pad size.

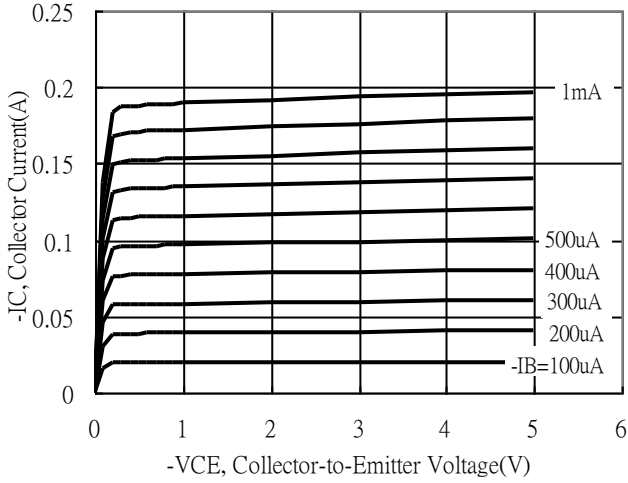
Characteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CEO(SUS)}	-80	-	-	V	I _C =-30mA, I _B =0
I _{CEO}	-	-	-10	μA	V _{CE} =-80V, I _B =0
I _{CES}	-	-	-10	μA	V _{CE} =-80V, V _{BE} =0
I _{EBO}	-	-	-50	μA	V _{EB} =-5V, I _C =0
*V _{CE(sat)}	-	-0.6	-1.0	V	I _C =-8A, I _B =-0.4A
*V _{BE(sat)}	-	-1.0	-1.5	V	I _C =-8A, I _B =-0.8A
*h _{FE}	60	-	-	-	V _{CE} =-1V, I _C =-2A
*h _{FE}	40	-	-	-	V _{CE} =-1V, I _C =-4A
f _T	-	40	-	MHz	V _{CE} =-10V, I _C =-500mA, f=20MHz
Cob	-	98	-	pF	V _{CB} =-10V, f=1MHz

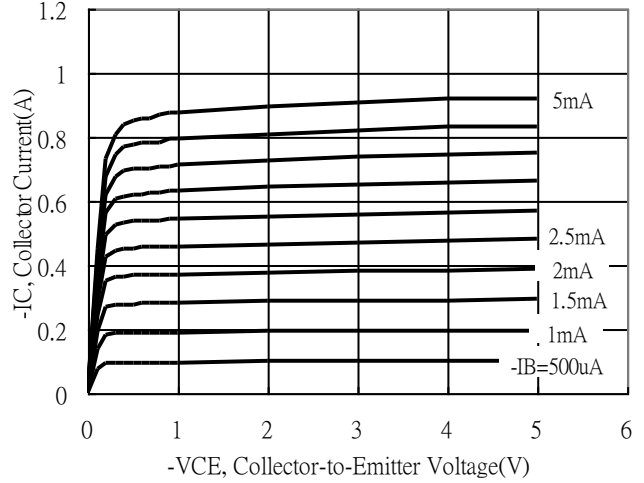
*Pulse Test : Pulse Width ≤ 380μs, Duty Cycle ≤ 2%

Typical Characteristics

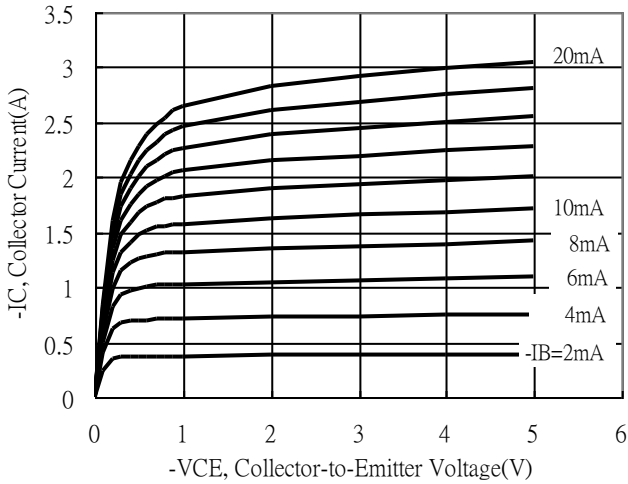
Emitter Grounded Output Characteristics



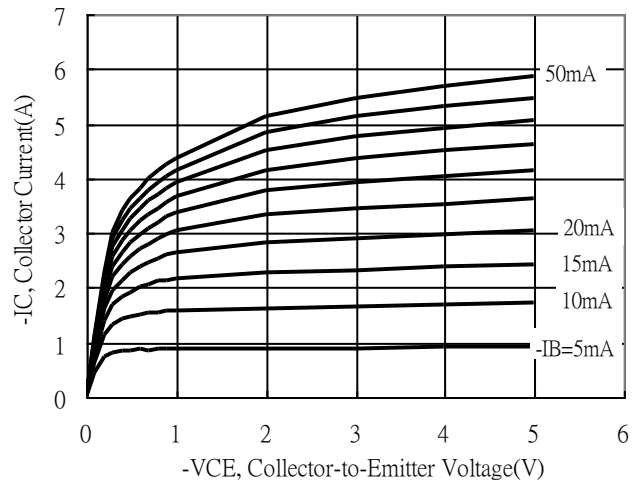
Emitter Grounded Output Characteristics



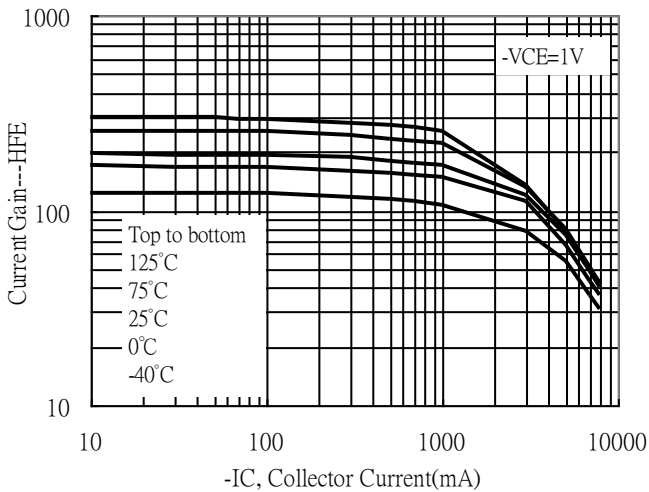
Emitter Grounded Output Characteristics



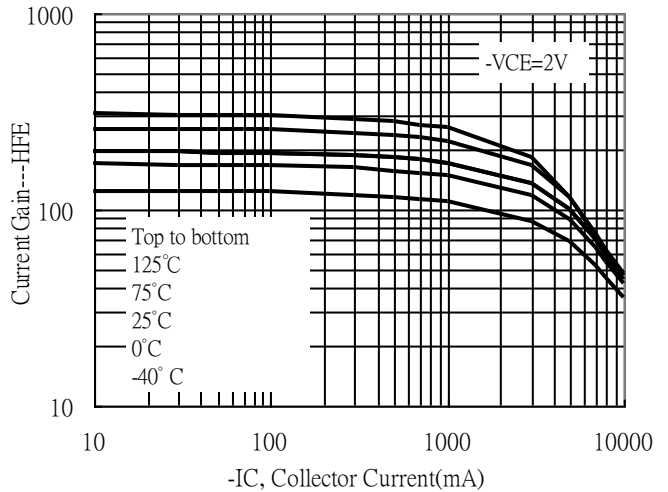
Emitter Grounded Output Characteristics



Current Gain vs Collector Current

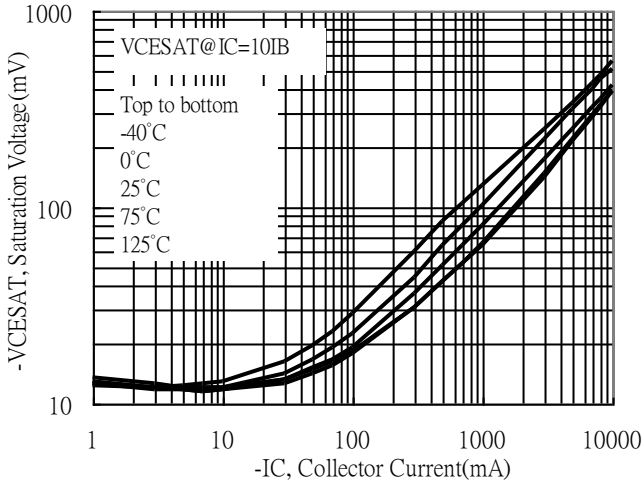


Current Gain vs Collector Current

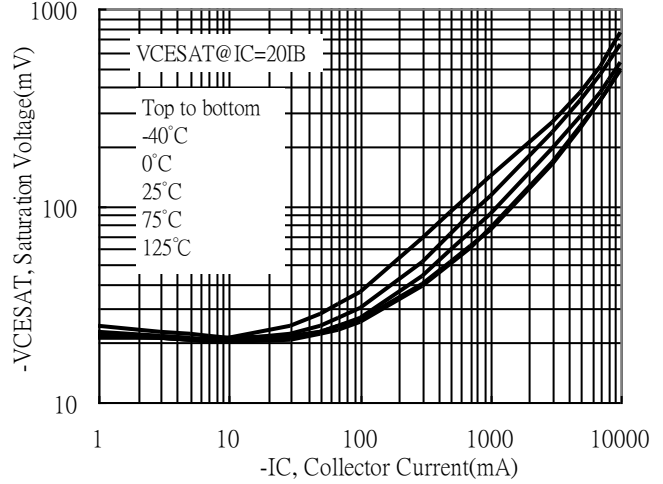


Typical Characteristics (Cont.)

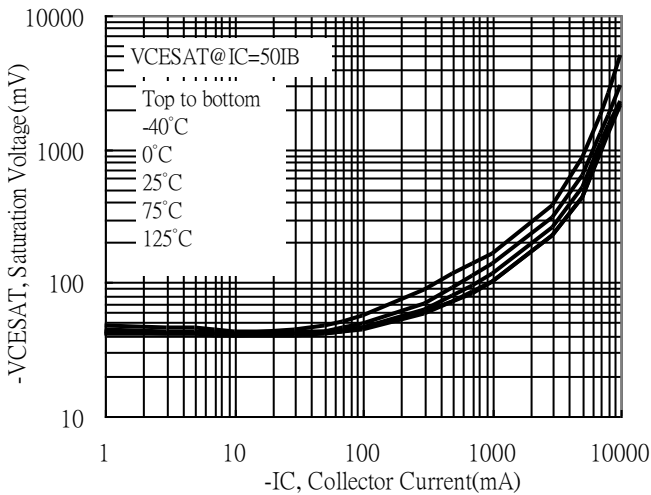
Saturation Voltage vs Collector Current



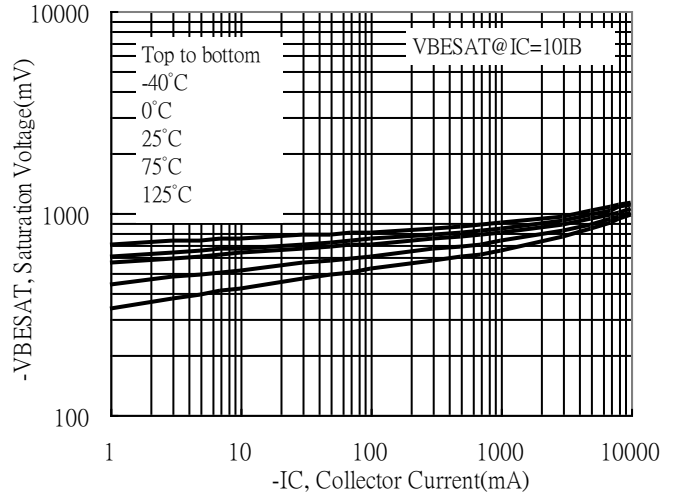
Saturation Voltage vs Collector Current



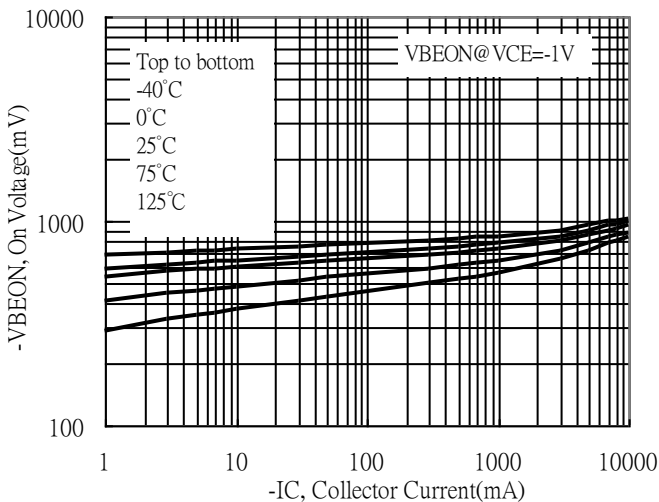
Saturation Voltage vs Collector Current



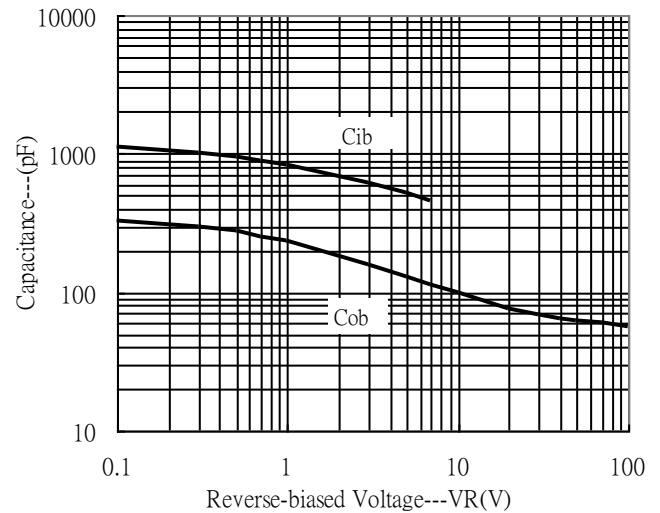
Saturation Voltage vs Collector Current



On Voltage vs Collector Current

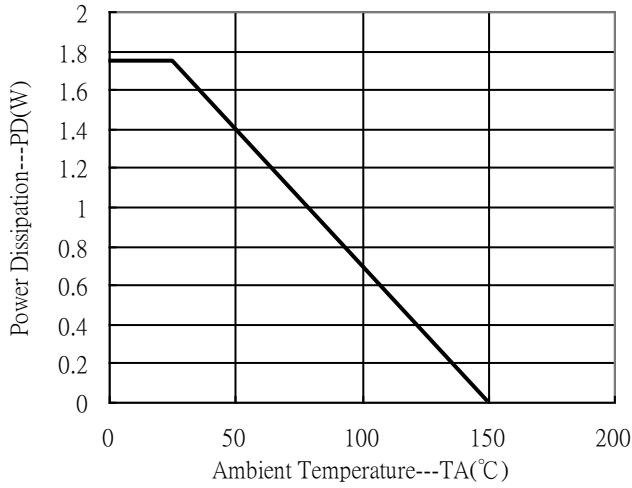


Capacitance vs Reverse-biased Voltage

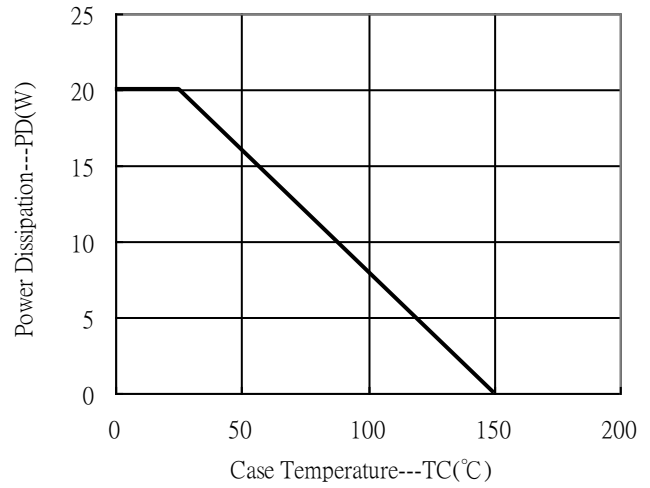


Typical Characteristics (Cont.)

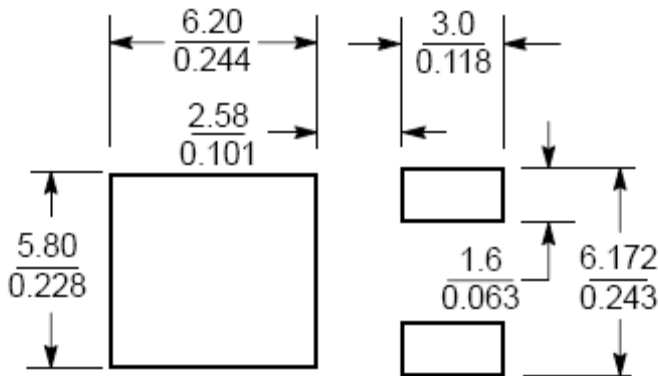
Power Derating Curve



Power Derating Curve

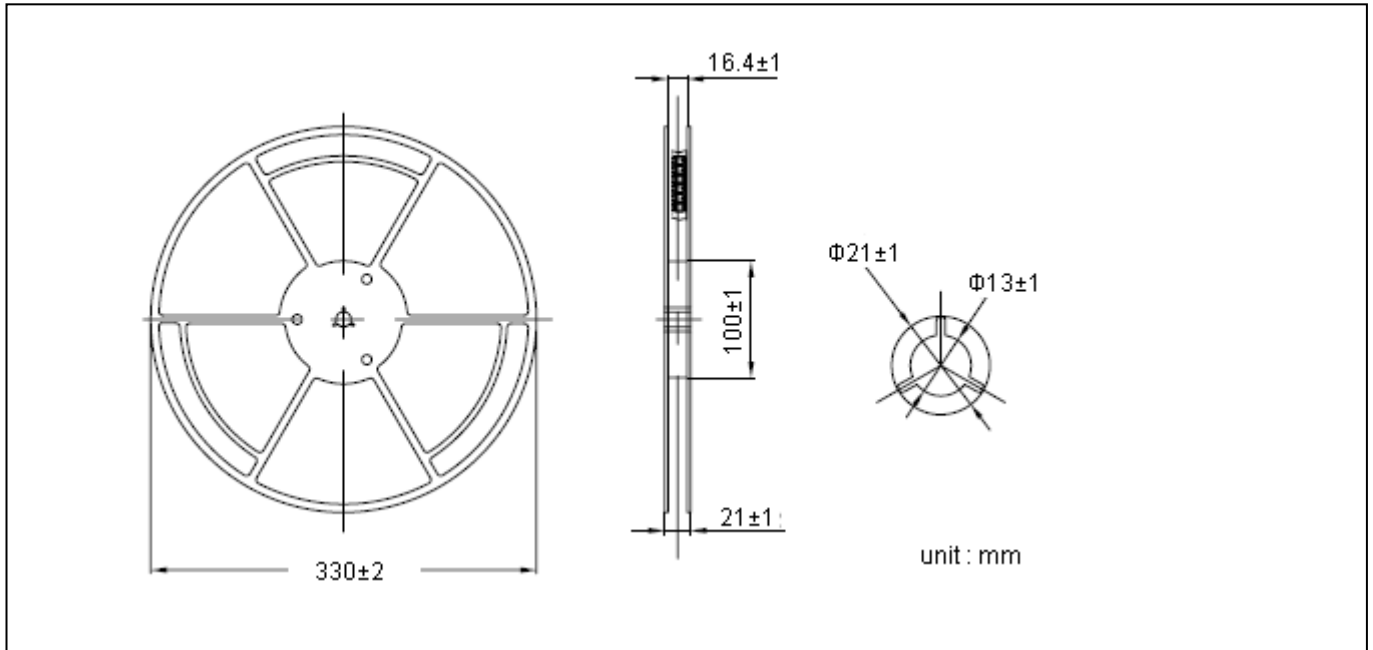


Recommended soldering footprint

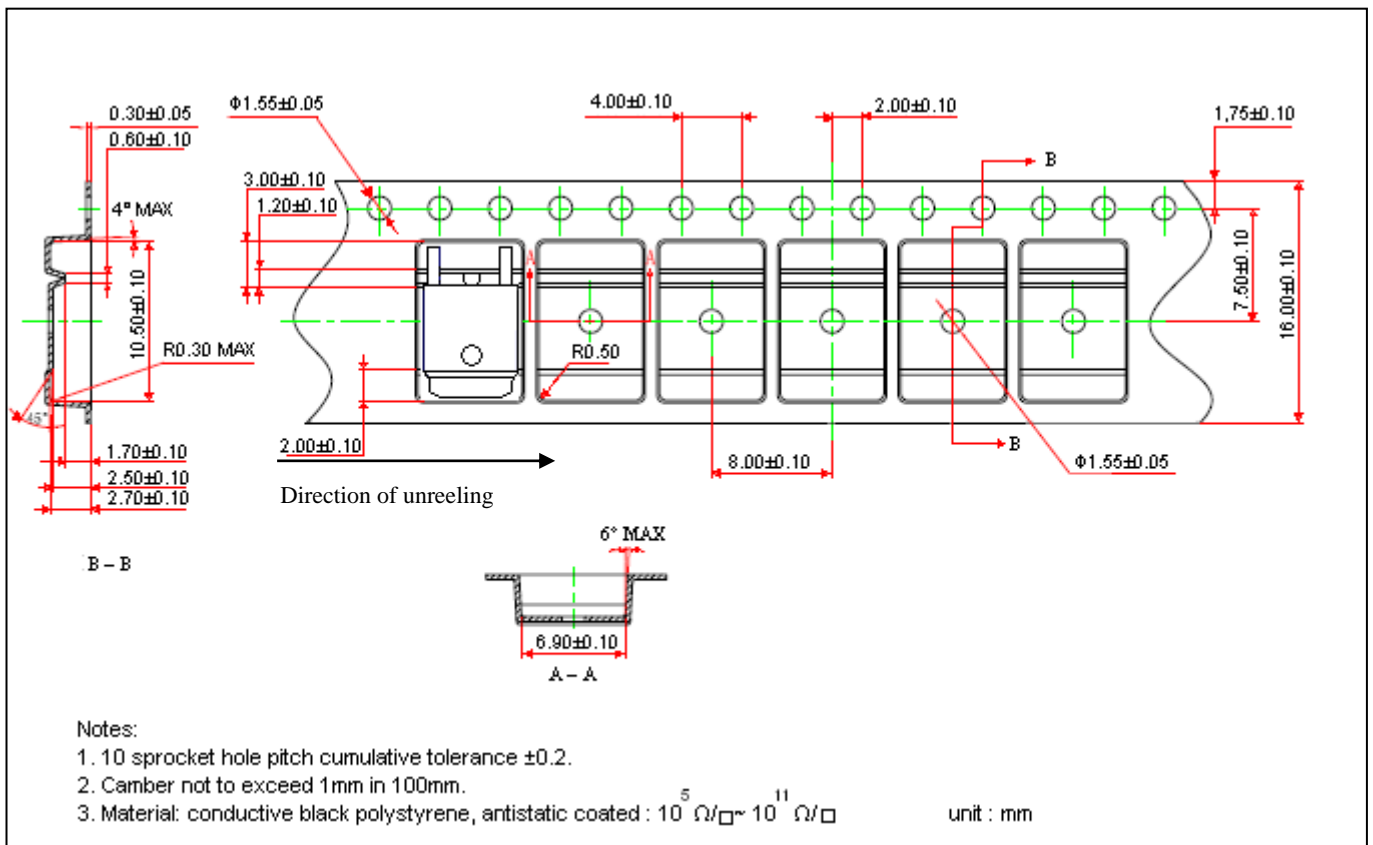


Unit ($\frac{\text{mm}}{\text{inch}}$)

Reel Dimension



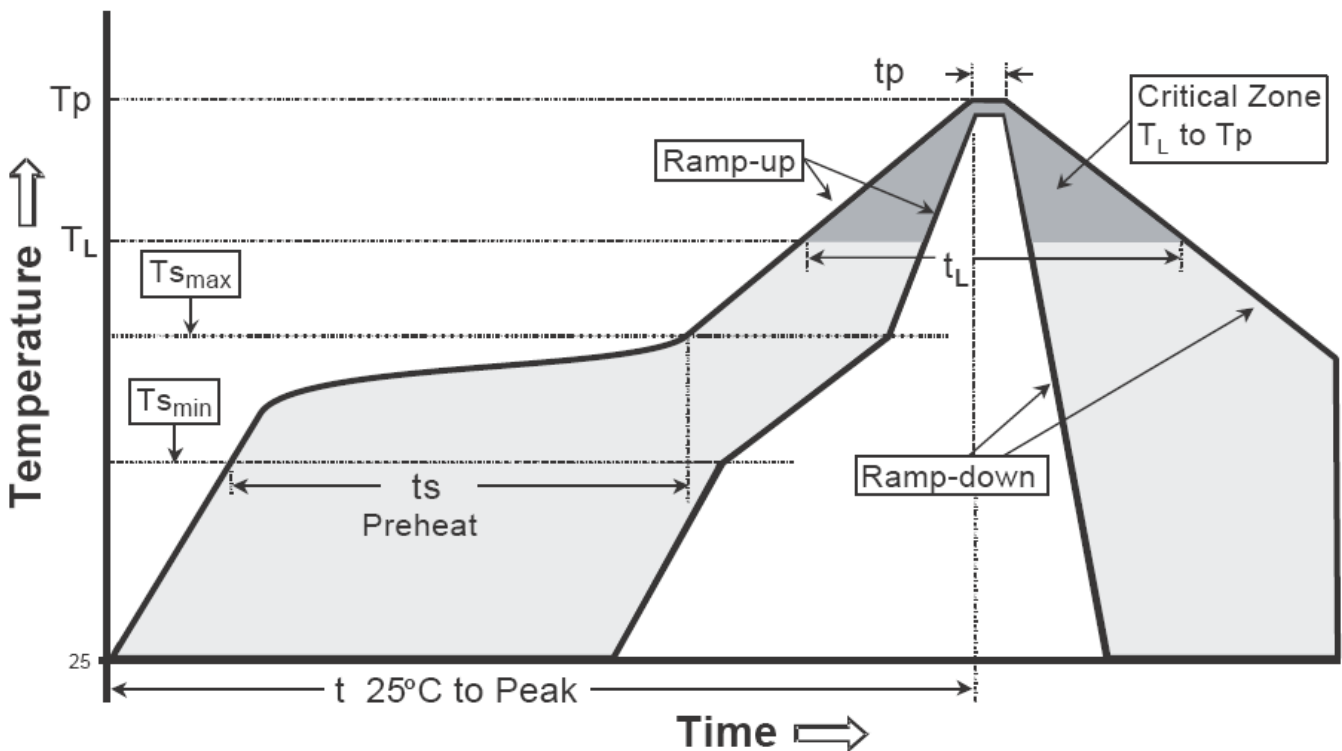
Carrier Tape Dimension



Recommended wave soldering condition

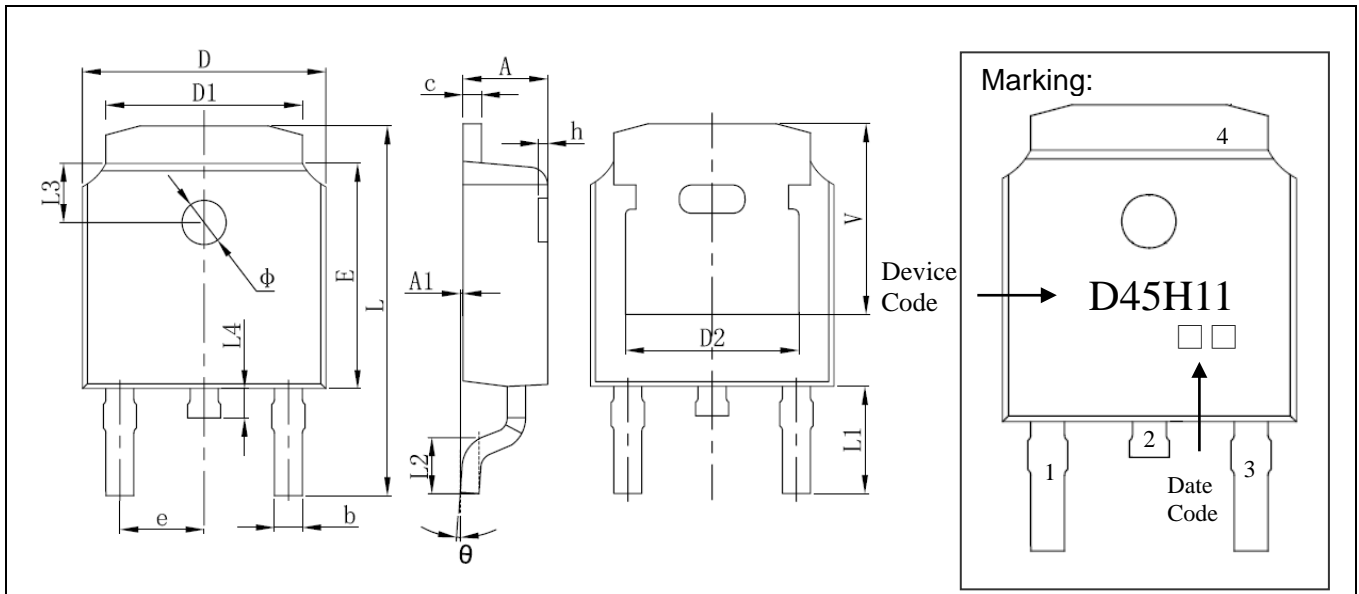
Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(t _p)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

TO-252 Dimension



3-Lead TO-252 Plastic Surface Mount Package
 CYStek Package Code: J3

Style: Pin 1.Base 2.Collector 3.Emitter 4.Collector

Date Code :

1st Code : year code, the last digit of Christian year, 2018→8, 2019→9, 2020→0, 2021→1, ..., etc.
 2nd Code : month code, Jan→1, Feb→2, Mar→3, Apr→4, May→5, Jun→6, Jul→7, Aug→8, Sep→9, Oct→A, Nov→B, Dec→C

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.087	0.094	2.200	2.400	L	0.382	0.406	9.712	10.312
A1	0.000	0.005	0.000	0.127	L1	0.114	REF	2.900	REF
b	0.025	0.030	0.635	0.770	L2	0.055	0.067	1.400	1.700
c	0.018	0.023	0.460	0.580	L3	0.063	REF	1.600	REF
D	0.256	0.264	6.500	6.700	L4	0.024	0.039	0.600	1.000
D1	0.201	0.215	5.100	5.460	Φ	0.043	0.051	1.100	1.300
D2	0.190	REF	4.830	REF	θ	0°	8°	0°	8°
E	0.236	0.244	6.000	6.200	h	0.000	0.012	0.000	0.300
e	0.086	0.094	2.186	2.386	v	0.207	REF	5.250	REF

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead : Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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