

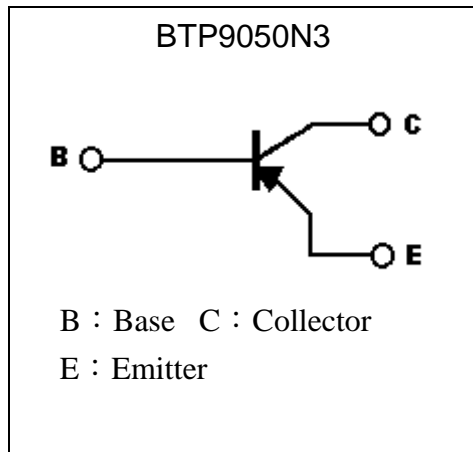
**High Voltage PNP Epitaxial Planar Transistor**

# BTP9050N3

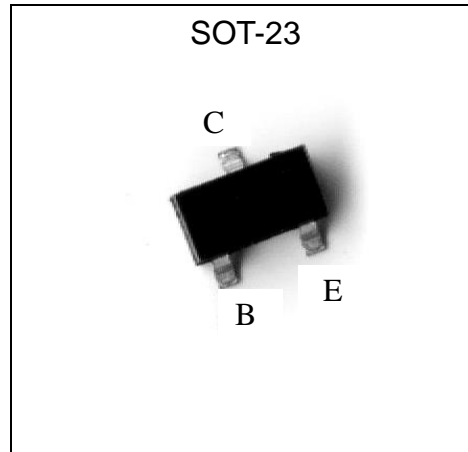
**Description**

- High breakdown voltage. ( $BV_{CEO} = -500V$ )
- Low saturation voltage, typical  $V_{CE(sat)} = -0.2V$  at  $I_C/I_B = -20mA/-2mA$ .
- Complementary to BTNA45N3
- Pb-free lead plating and halogen-free package

**Symbol**

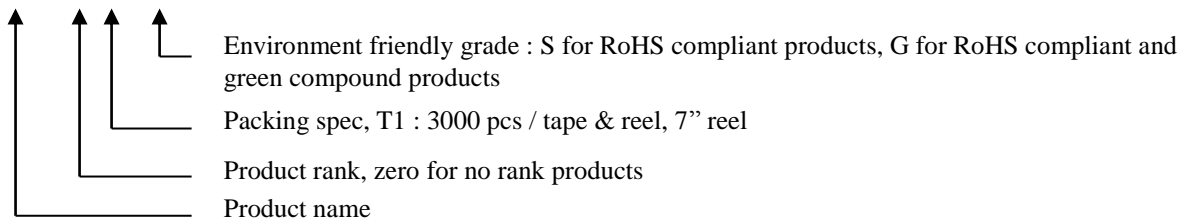


**Outline**



**Ordering Information**

Device	Package	Shipping
BTP9050N3-0-T1-G	SOT-23 (Pb-free lead plating and halogen-free package)	3000 pcs / tape & reel





**Absolute Maximum Ratings** (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V <sub>CB0</sub>	-500	V
Collector-Emitter Voltage	V <sub>CEO</sub>	-500	V
Emitter-Base Voltage	V <sub>EBO</sub>	-5	V
Collector Current(DC)	I <sub>C</sub>	-150	mA
Peak Collector Current , single pulse, pulse width tp<1ms	I <sub>CM</sub>	-500	mA
Peak Base Current, single pulse, pulse width tp<1ms	I <sub>BM</sub>	-200	mA
Power Dissipation	P <sub>D</sub>	300 (Note)	mW
Operating Junction and Storage Temperature Range	T <sub>j</sub> ; T <sub>stg</sub>	-55~+150	°C

Note : Device mounted on a FR-4 PCB, single sided copper, tin plated and standard footprint.

**Thermal Characteristics**

Parameter	Symbol	Limit	Unit
Thermal Resistance, Junction-to-Ambient, in free air (Note)	R <sub>th,j-a</sub>	417	°C/W
Thermal Resistance, Junction-to-Solder point	R <sub>th,j-sp</sub>	70	

Note : Device mounted on a FR-4 PCB, single sided copper, tin plated and standard footprint.

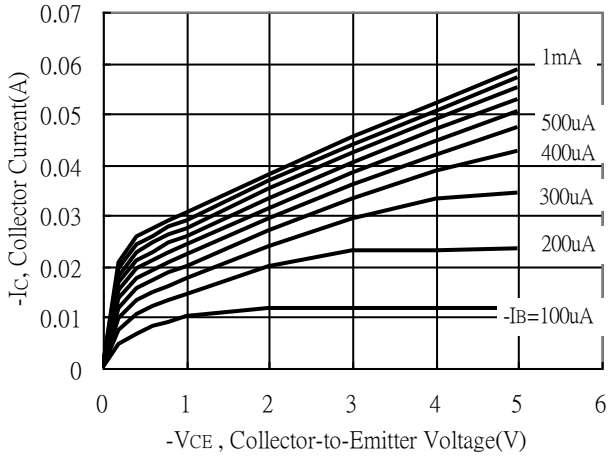
**Characteristics** (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV <sub>CB0</sub>	-500	-	-	V	I <sub>C</sub> =-100μA
BV <sub>CEO</sub>	-500	-	-	V	I <sub>C</sub> =-1mA
BV <sub>EBO</sub>	-5	-	-	V	I <sub>E</sub> =-50μA
I <sub>CB0</sub>	-	-	-100	nA	V <sub>CB</sub> =-480V
I <sub>CES</sub>	-	-	-100	nA	V <sub>CE</sub> =-480V, V <sub>BE</sub> =0V
I <sub>EBO</sub>	-	-	-1	μA	V <sub>EB</sub> =-5V
*V <sub>CE(sat)</sub>	-	-	-0.5	V	I <sub>C</sub> =-20mA, I <sub>B</sub> =-2mA
*V <sub>CE(sat)</sub>	-	-	-0.5	V	I <sub>C</sub> =-50mA, I <sub>B</sub> =-10mA
*V <sub>BE(sat)</sub>	-	-	-0.9	V	I <sub>C</sub> =-50mA, I <sub>B</sub> =-10mA
*h <sub>FE 1</sub>	100	-	300	-	V <sub>CE</sub> =-10V, I <sub>C</sub> =-10mA
*h <sub>FE 2</sub>	80	-	300	-	V <sub>CE</sub> =-10V, I <sub>C</sub> =-50mA
*h <sub>FE 3</sub>	40	-	-	-	V <sub>CE</sub> =-10V, I <sub>C</sub> =-100mA
f <sub>T</sub>	-	50	-	MHz	V <sub>CE</sub> =-10V, I <sub>C</sub> =-10mA, f=10MHz
C <sub>ob</sub>	-	12	-	pF	V <sub>CB</sub> =-10V, I <sub>E</sub> =0A, f=1MHz
C <sub>ib</sub>	-	85	-	pF	V <sub>EB</sub> =-0.5V, I <sub>C</sub> =0A, f=1MHz

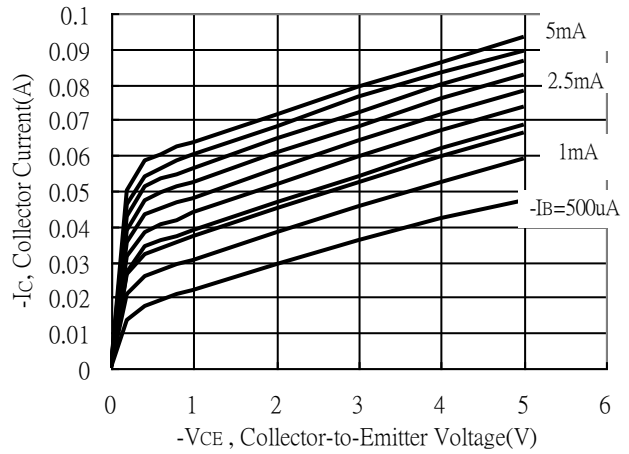
\*Pulse Test: Pulse Width ≤380μs, Duty Cycle≤2%

**Typical Characteristics**

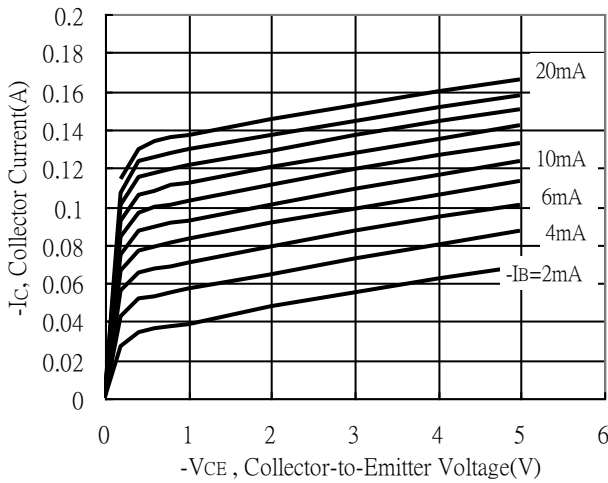
Emitter Grounded Output Characteristics



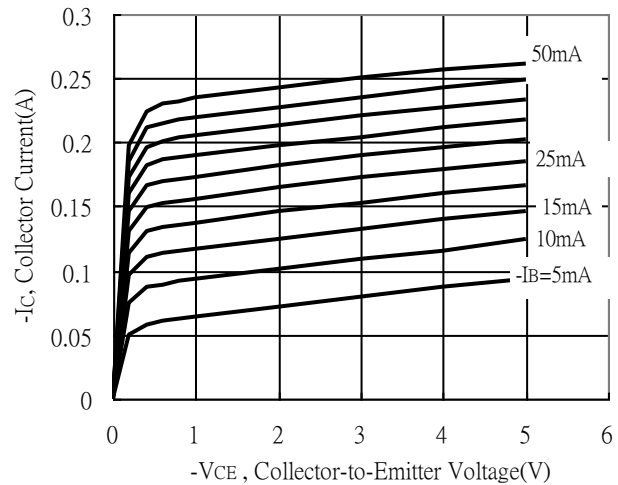
Emitter Grounded Output Characteristics



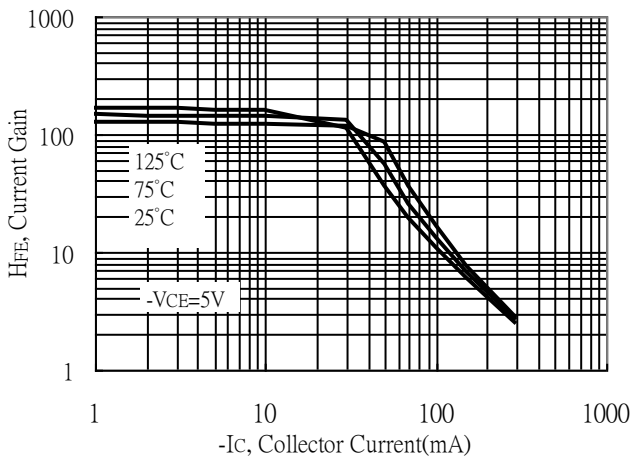
Emitter Grounded Output Characteristics



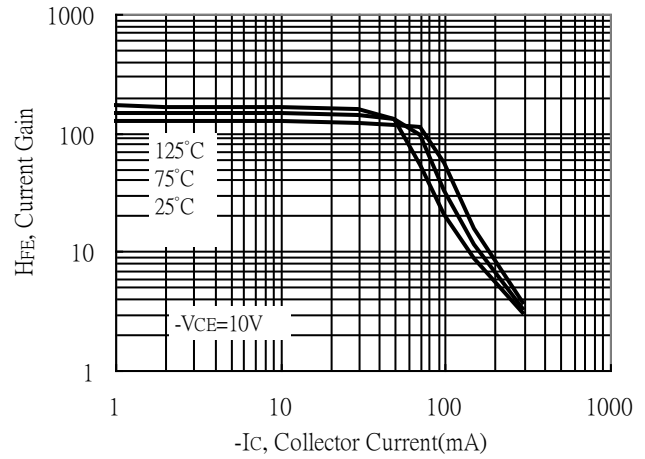
Emitter Grounded Output Characteristics



Current Gain vs Collector Current



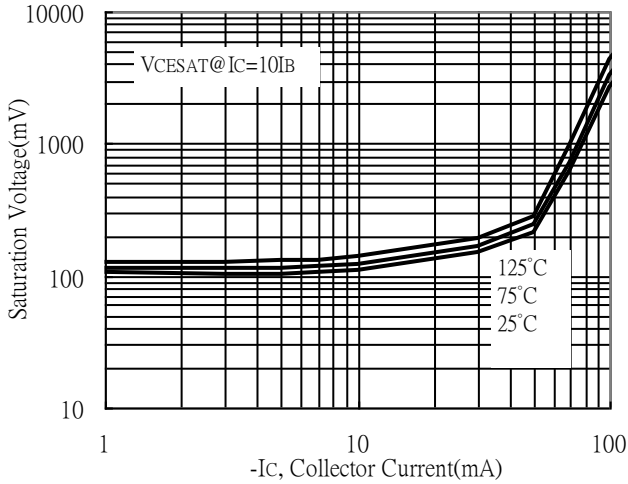
Current Gain vs Collector Current



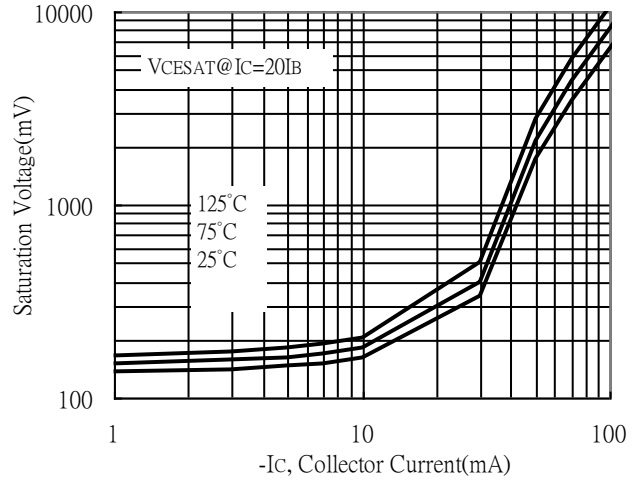


**Typical Characteristics**

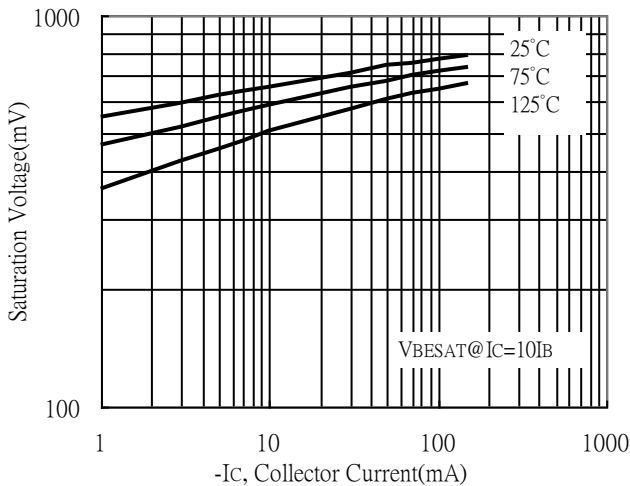
Saturation Voltage vs Collector Current



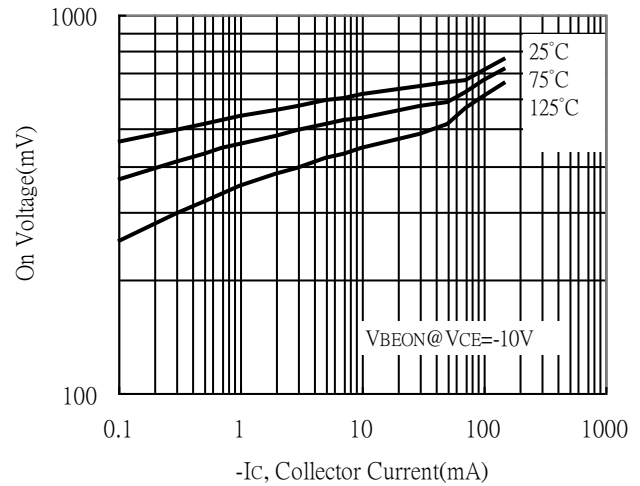
Saturation Voltage vs Collector Current



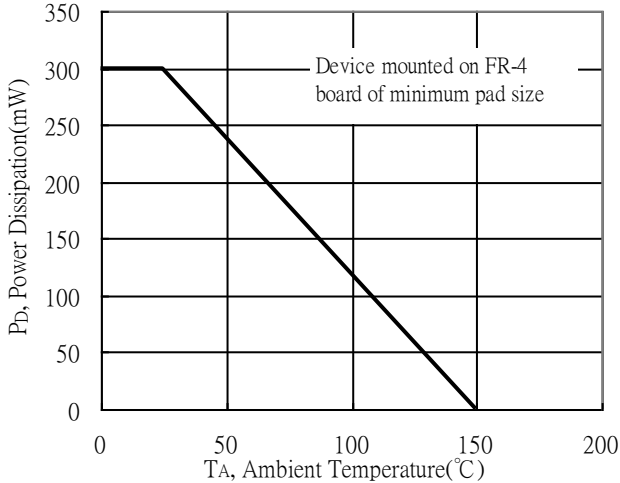
Saturation Voltage vs Collector Current



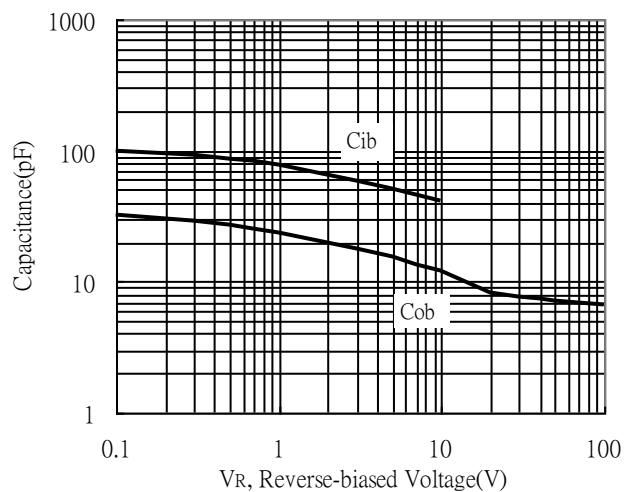
On Voltage vs Collector Current



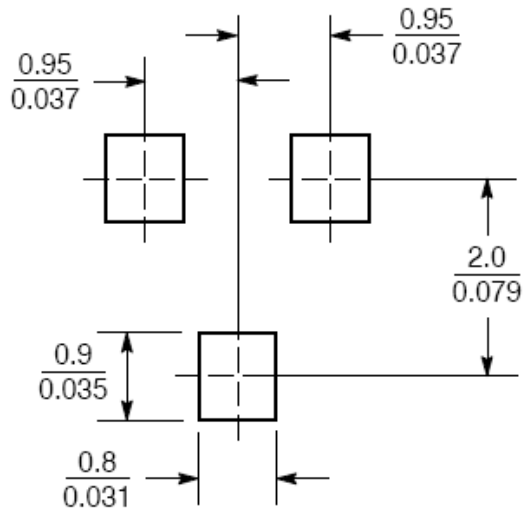
Power Derating Curve



Capacitance vs Reverse-biased Voltage

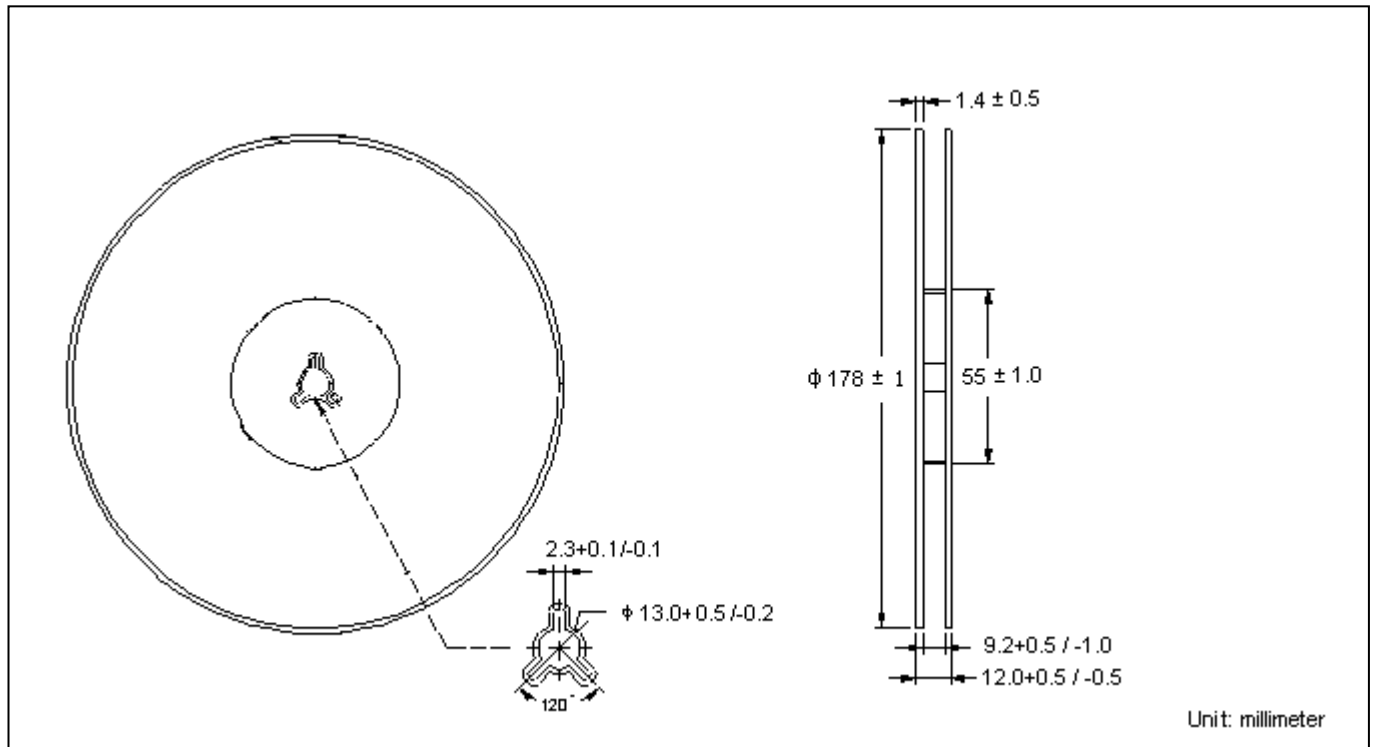


### Recommended Soldering Footprint

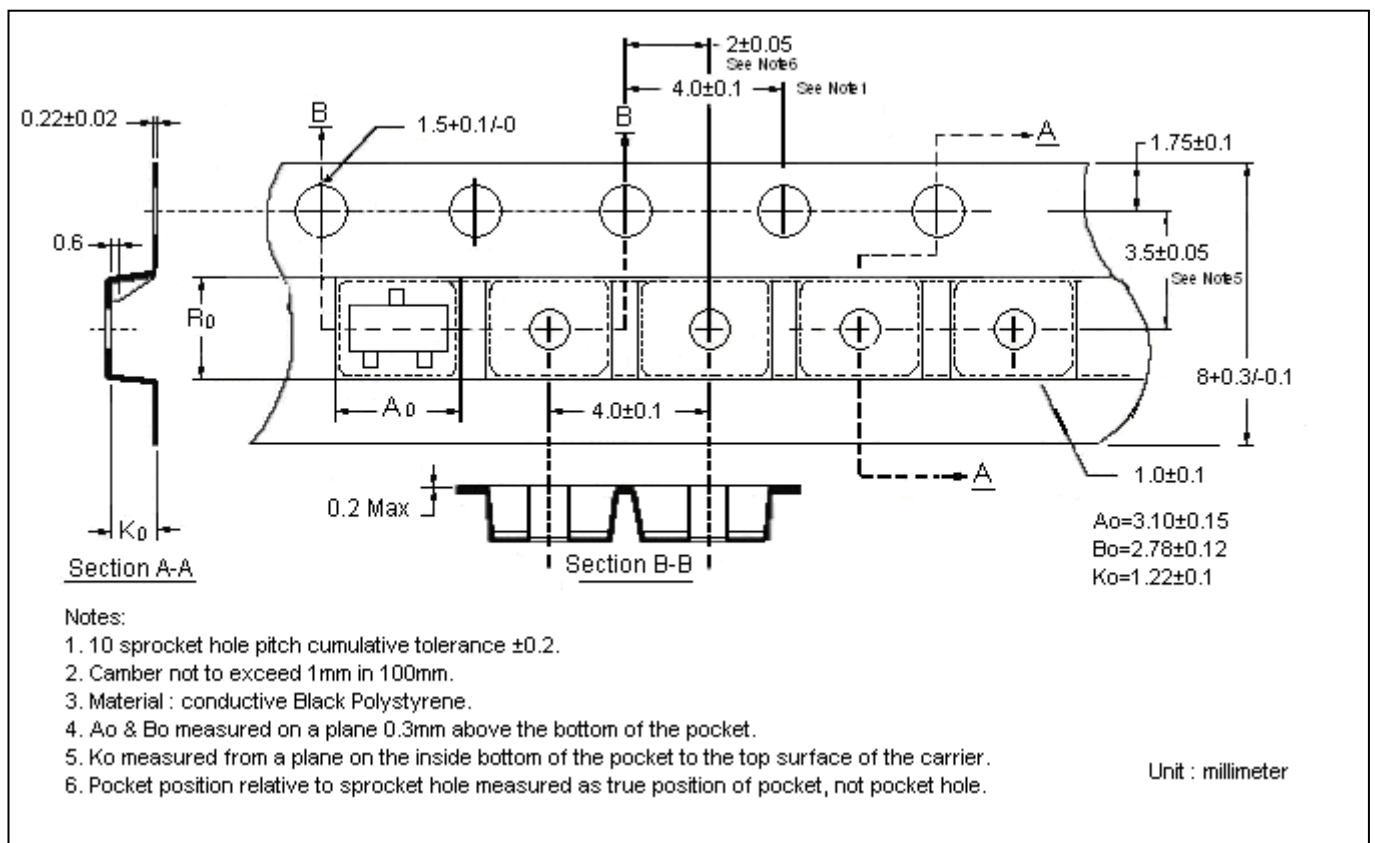


Unit :  $\frac{\text{mm}}{\text{inches}}$

### Reel Dimension



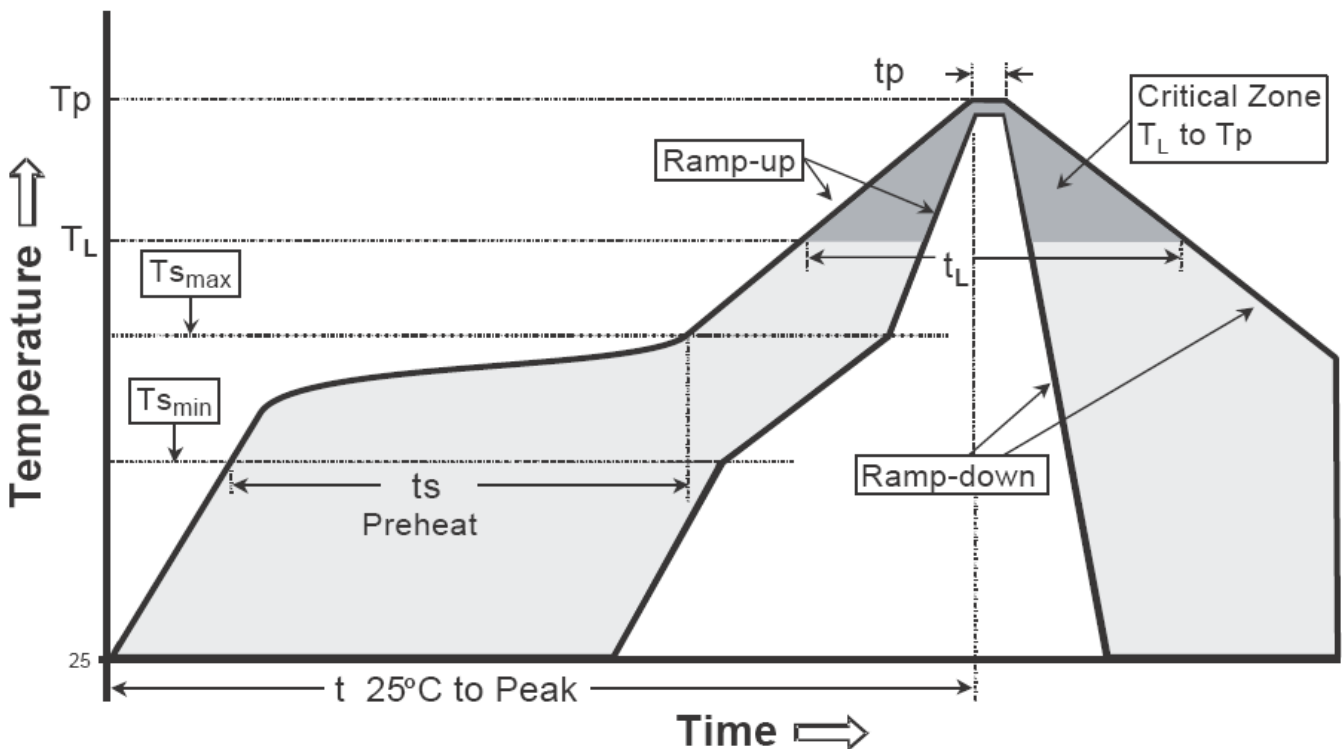
### Carrier Tape Dimension



**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

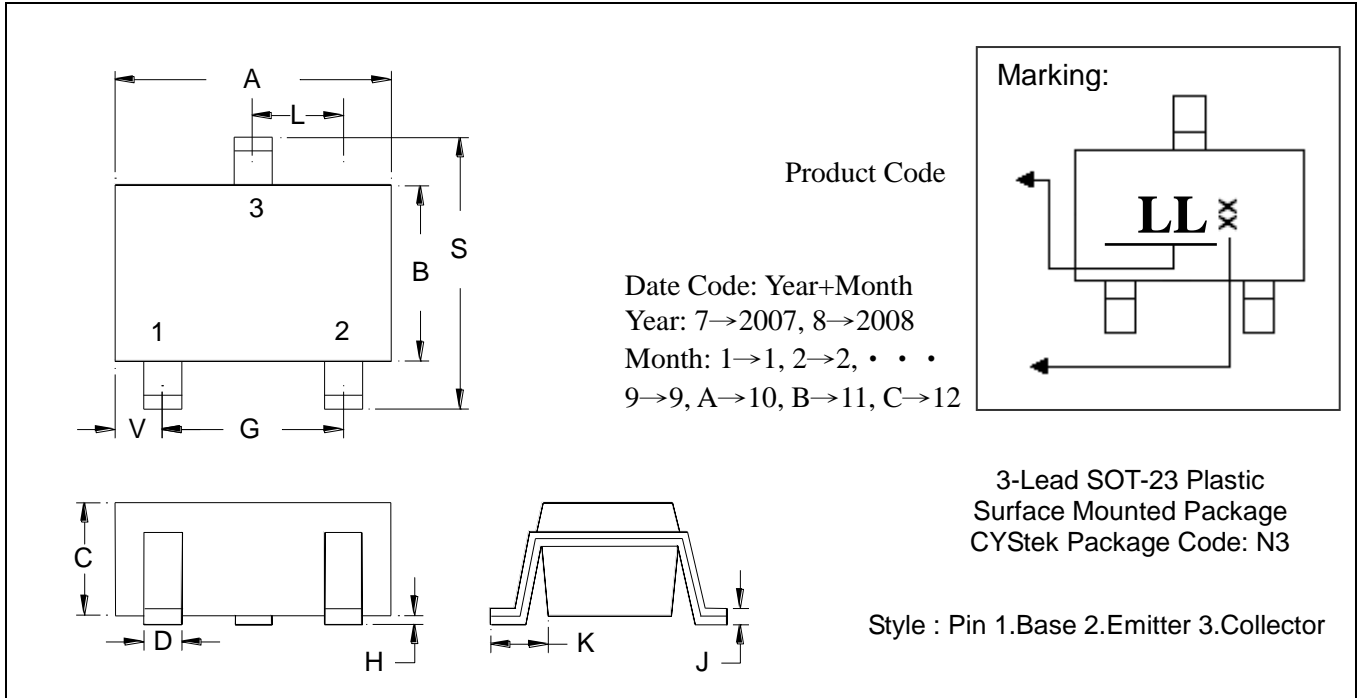
**Recommended temperature profile for IR reflow**



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (Tl)	183°C	217°C
- Time (tl)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

**SOT-23 Dimension**



\*:Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1102	0.1204	2.80	3.04	J	0.0031	0.0071	0.08	0.18
B	0.0472	0.0630	1.20	1.60	K	0.0128	0.0266	0.32	0.67
C	0.0335	0.0512	0.89	1.30	L	0.0335	0.0453	0.85	1.15
D	0.0118	0.0197	0.30	0.50	S	0.0830	0.1161	2.10	2.95
G	0.0669	0.0910	1.70	2.30	V	0.0098	0.0256	0.25	0.65
H	0.0005	0.0040	0.013	0.10					

- Notes : 1.Controlling dimension : millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material :**

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

**Important Notice:**

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.