NPN High Voltage Planar Transistor

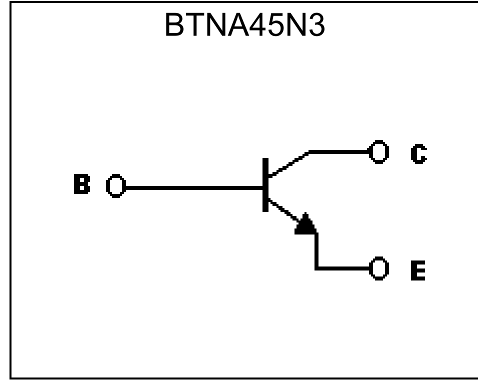
BTNA45N3

BV_{CEO}	500V
I_C	150mA
V_{CESAT}	150mV (max)

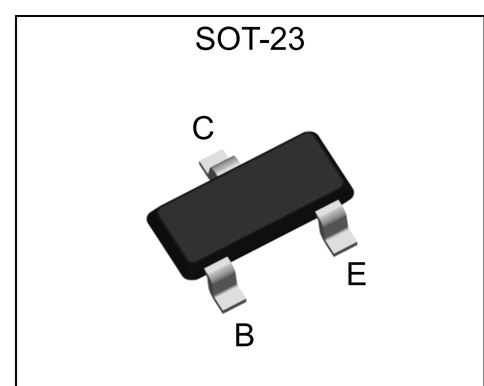
Features

- High breakdown voltage. (BV_{CEO}=500V)
- Low collector-emitter saturation voltage V_{CESAT}.
- High collector current capability I_C and I_{CM}.
- High collector current gain H_{FE} at high collector current I_C.
- Low collector output capacitance. (Typ. 5pF at V_{CB} =20V)
- Pb-free lead plating and halogen-free package.

Symbol

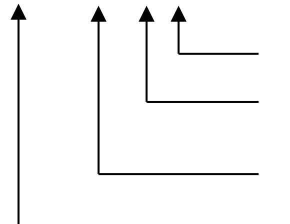


Outline



Ordering Information

Device	Package	Shipping
BTNA45N3-0-T1-G	SOT-23 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel



Environment friendly grade : S for RoHS compliant products, G for RoHS compliant and green compound products

Packing spec, T1 :3000 pcs/tape & reel, 7” reel

Product rank, zero for no rank products

Product name

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CBO}	500	V
Collector-Emitter Voltage	V_{CES}	500	
Collector-Emitter Voltage	V_{CEO}	500	
Emitter-Base Voltage	V_{EBO}	7	
Collector Current	I_C	150	mA
Peak Collector Current , single pulse, pulse width tp<1ms	I_{CM}	500	
Peak Base Current, single pulse, pulse width tp<1ms	I_{BM}	200	
Power Dissipation (Note)	Pd	300	mW
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	-55~+150	°C

Note : Device mounted on a FR-4 PCB, single sided copper, tin plated and standard footprint.

Thermal Characteristics

Parameter	Symbol	Limit	Unit
Thermal Resistance, Junction-to-Ambient, in free air (Note)	Rth,j-a	417	°C/W
Thermal Resistance, Junction-to-Solder point	Rth,j-sp	70	

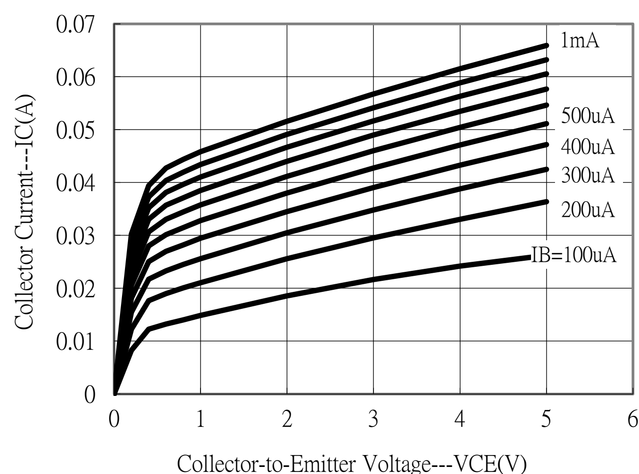
Note : Device mounted on a FR-4 PCB, single sided copper, tin plated and standard footprint.

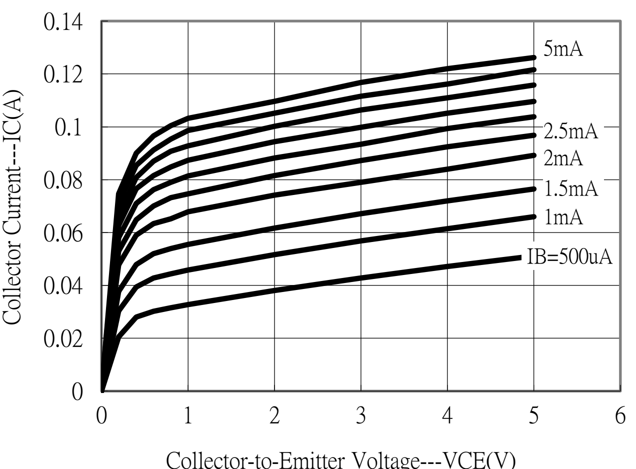
Characteristics (Ta=25°C)

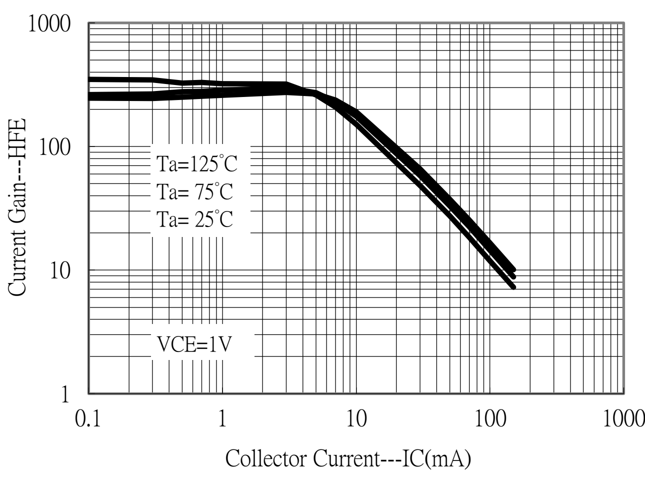
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
*BV_{CBO}	500	-	-	V	I_C=50μA
*BV_{CES}	500	-	-		I_C=50μA
*BV_{CEO}	500	-	-		I_C=10mA
BV_{EBO}	7	-	-		I_E=50μA
I_{CBO}	-	-	100	nA	V_{CB}=500V
I_{CES}	-	-	100		V_{CE}=500V
I_{EBO}	-	-	100		V_{EB}=5V
*$V_{CE(sat)}$ 1	-	-	90	mV	I_C=20mA, I_B=2mA
*$V_{CE(sat)}$ 2	-	-	150		I_C=50mA, I_B=6mA
*$V_{BE(sat)}$	-	-	0.9	V	I_C=50mA, I_B=5mA
*$V_{BE(on)}$	-	-	0.9		V_{CE}=10V, I_C=50mA
*h_{FE} 1	120	-	-	-	V_{CE}=10V, I_C=1mA
*h_{FE} 2	120	-	300	-	V_{CE}=10V, I_C=30mA
*h_{FE} 3	120	-	-	-	V_{CE}=10V, I_C=50mA
*h_{FE} 4	30	-	-	-	V_{CE}=10V, I_C=100mA
f_T	50	-	-	MHz	V_{CE}=20V, I_C=10mA, f=100MHz
Cob	-	5	8	pF	V_{CB}=20V, I_E=0A, f=1MHz
ton	-	110	-	ns	V_{CE}=100V, I_C=50mA, I_B1=5mA, I_B 2=-10mA
toff	-	1500	-		

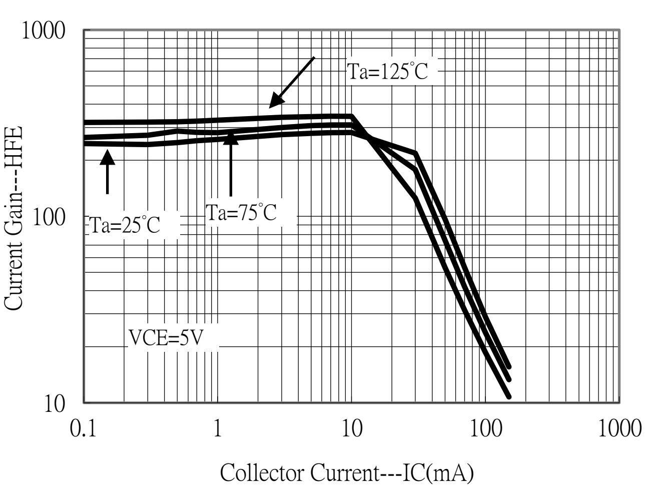
*Pulse Test: Pulse Width ≤300μs, Duty Cycle≤2%

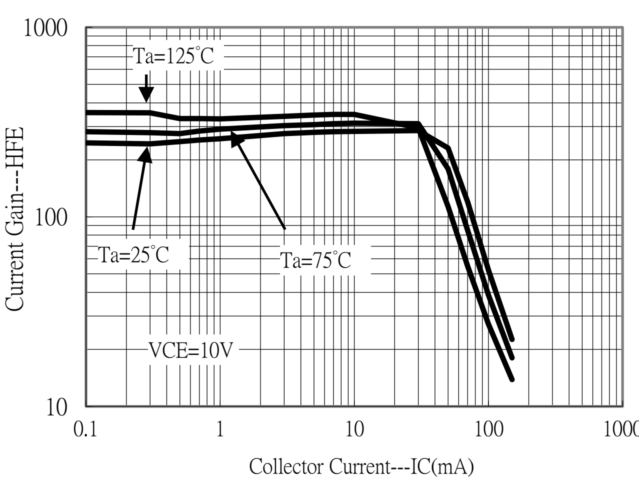
Typical Characteristics

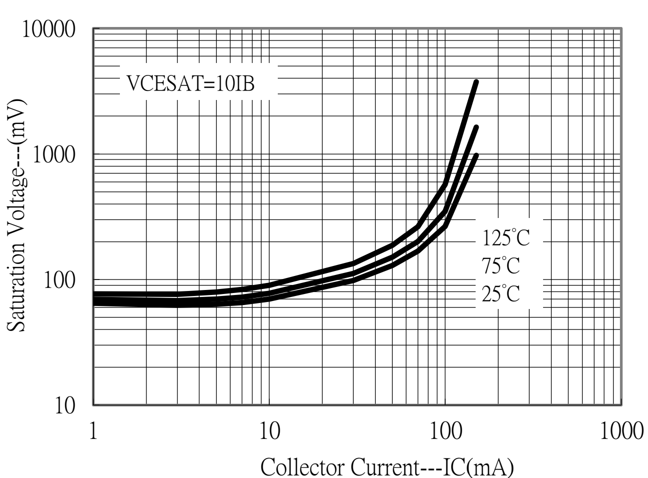




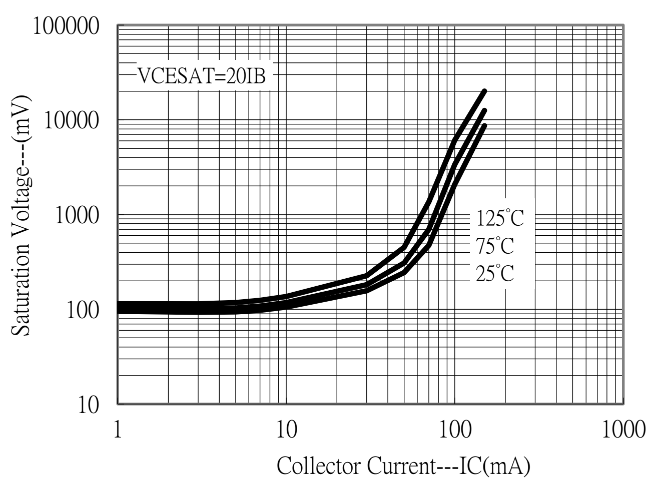


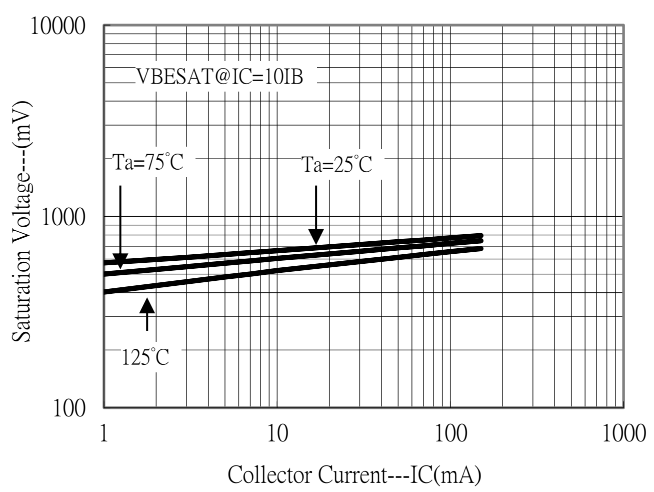


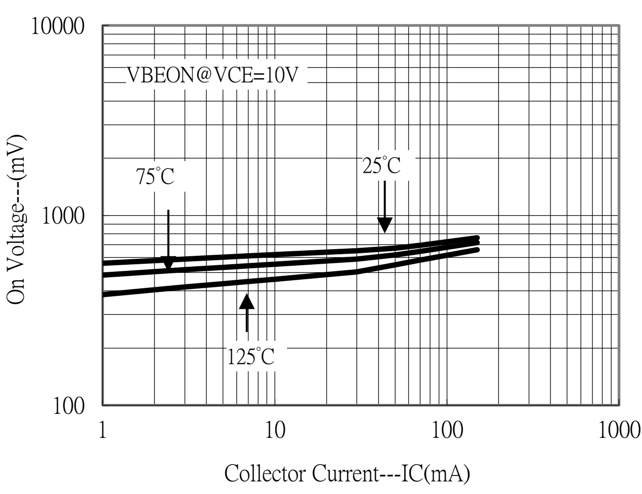


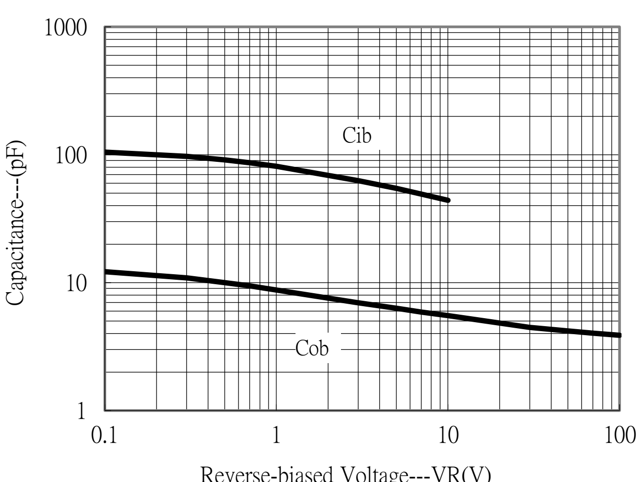


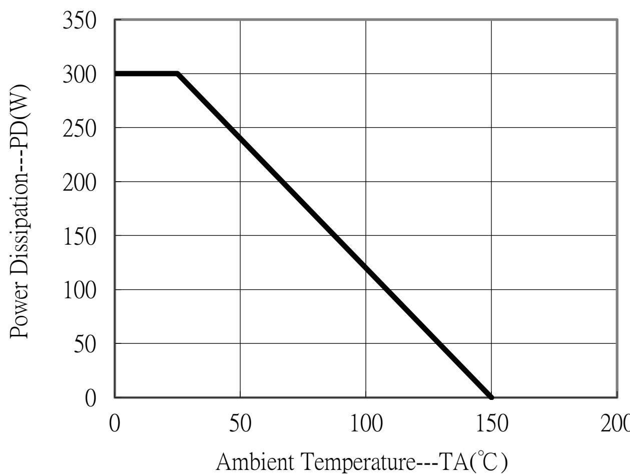
Typical Characteristics(Cont.)



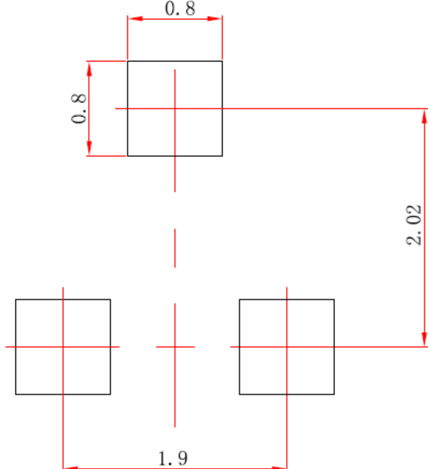






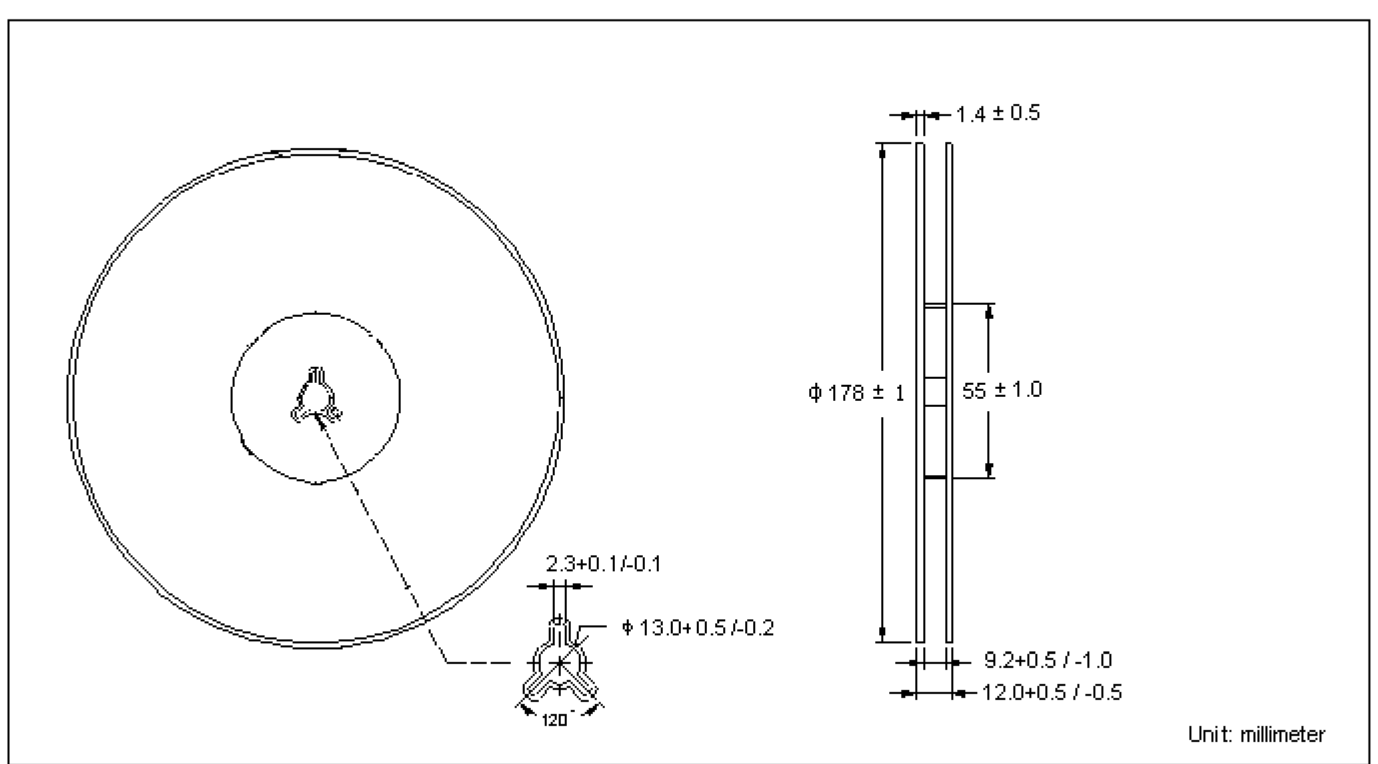


Recommended Soldering Footprint

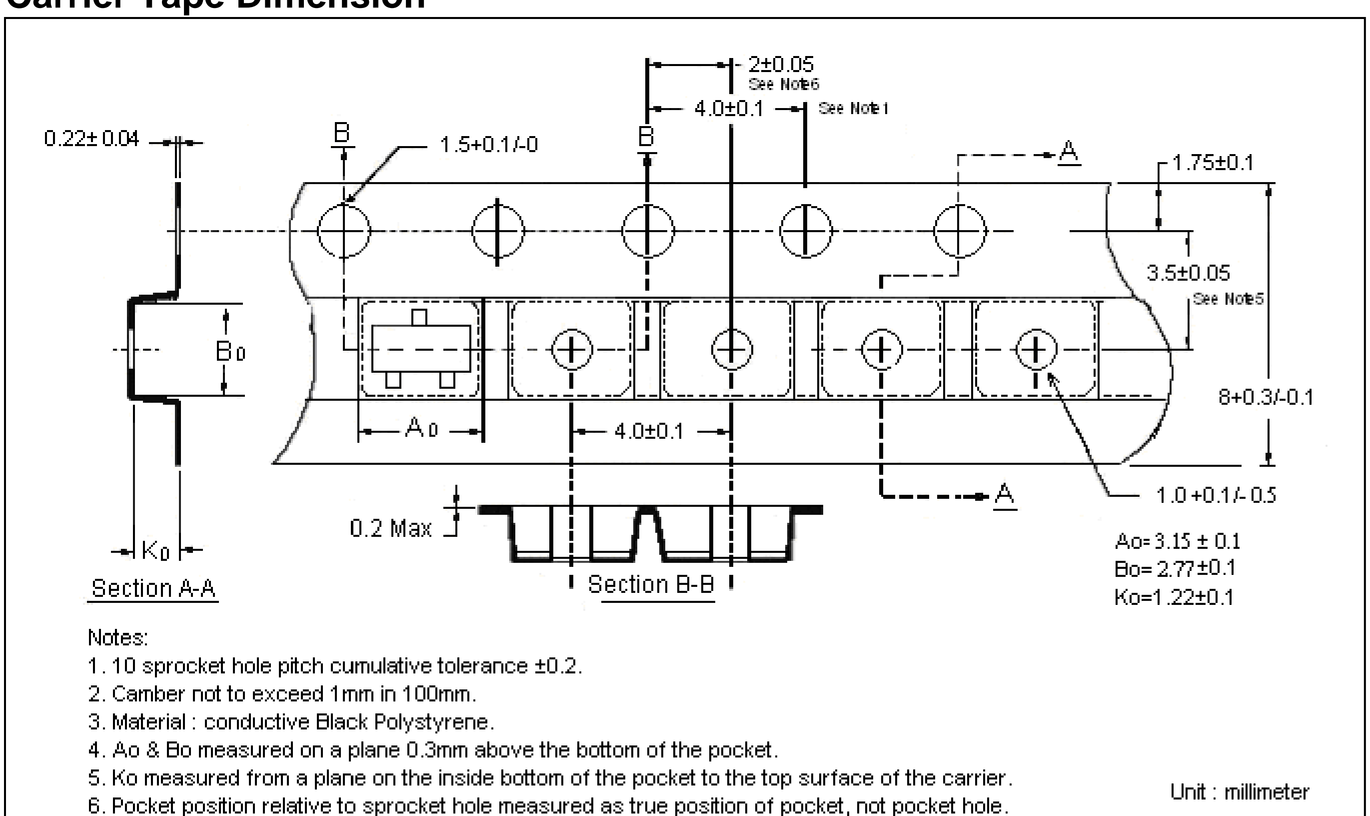


Unit：mm

Reel Dimension



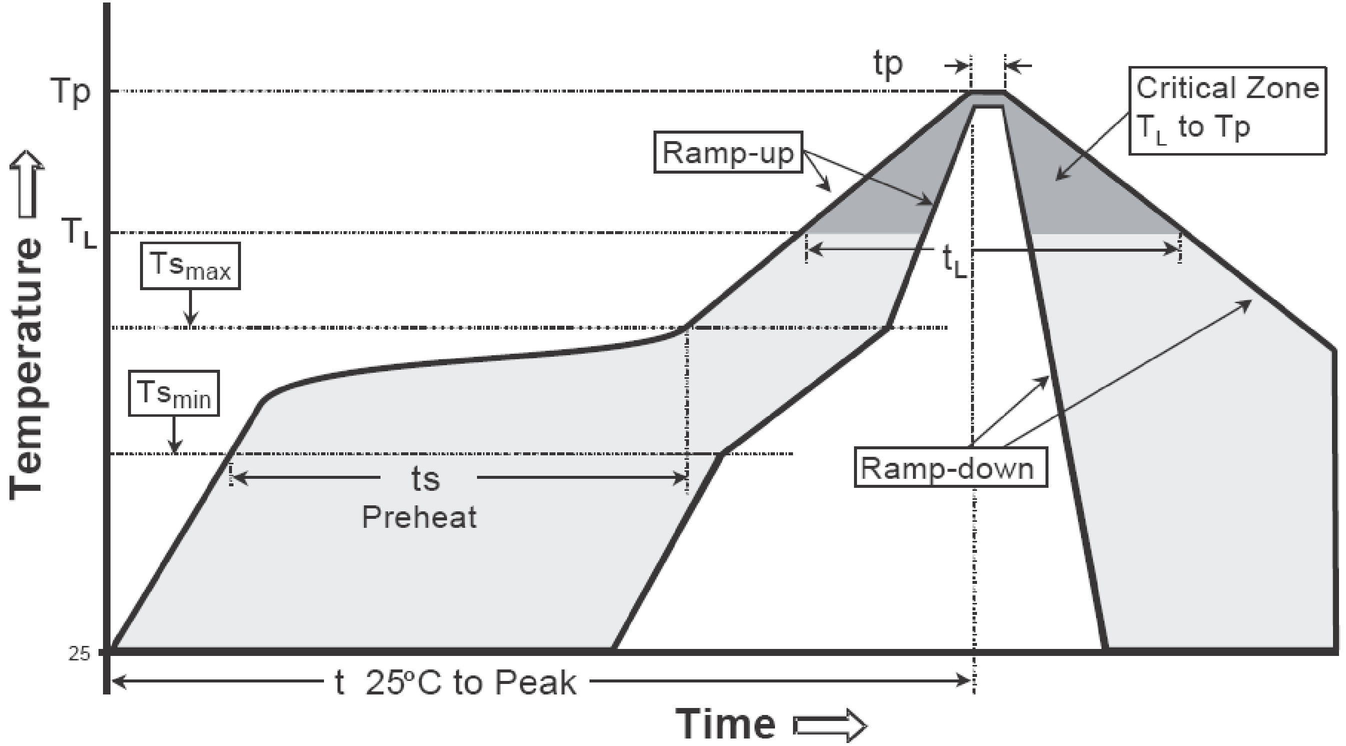
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

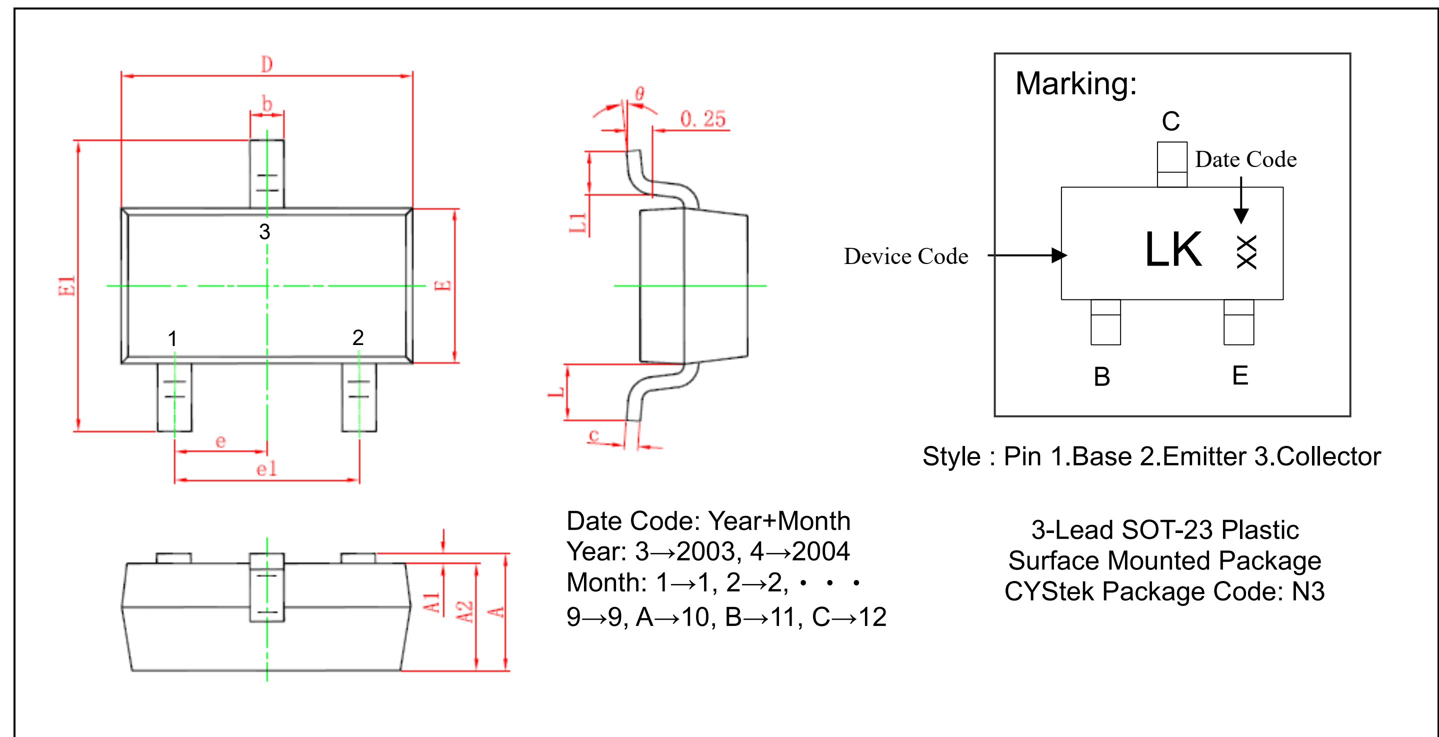
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(Ts min) −Temperature Max(Ts max) −Time(ts min to ts max)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (TL) − Time (tL)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note :1. All temperatures refer to topside of the package, measured on the package body surface.
2. For devices mounted on FR-4 PCB of 1.6mm or equivalent grade PCB. If other grade PCB is used, care should be taken to match the coefficients of thermal expansion between components and PCB. If they are not matched well, the solder joints may crack or the bodies of the parts may crack or shatter as the assembly cools.

SOT-23 Dimension



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.035	0.045	0.900	1.150	E1	0.089	0.100	2.250	2.550
A1	0.000	0.004	0.000	0.100	e	0.037 TYP.		0.950 TYP.	
A2	0.035	0.041	0.900	1.050	e1	0.071	0.079	1.800	2.000
b	0.012	0.020	0.300	0.500	L	0.022 REF.		0.550 REF.	
c	0.003	0.006	0.080	0.150	L1	0.012	0.020	0.300	0.500
D	0.110	0.118	2.800	3.000	θ	0°	8°	0°	8°
E	0.047	0.055	1.200	1.400					

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek ***semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.***
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.