

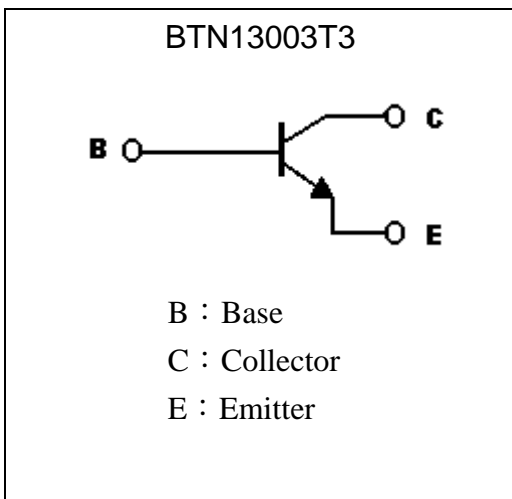
General Purpose NPN Epitaxial Planar Transistor

BTN13003T3

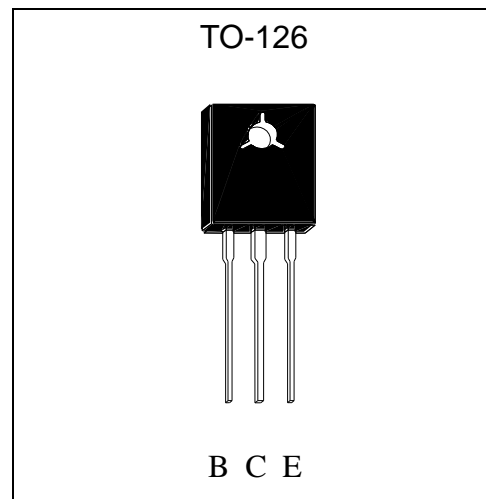
Features

- High breakdown voltage, $V_{CEO}=450V$ (min.)
- High collector current, $I_{C(max)}=1.5A$ (DC)
- Pb-free lead plating package

Symbol

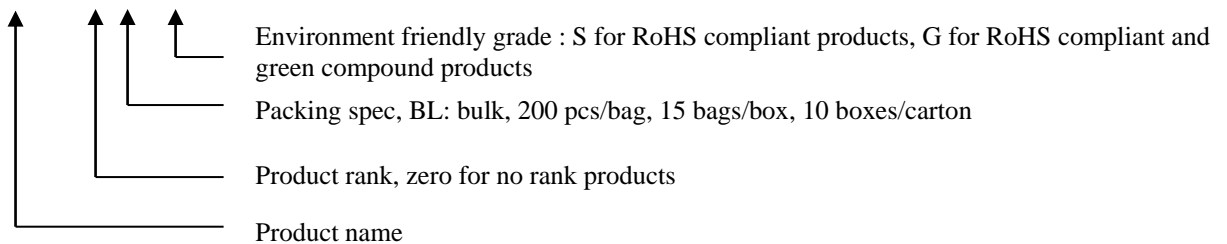


Outline



Ordering Information

Device	Package	Shipping
BTN13003T3-0-BL-X	TO-126 (Pb-free lead plating package)	200 pcs / bag, 3,000 pcs/box 30,000 pcs/carton





Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V _{CBO}	700	V
Collector-Emitter Voltage	V _{CEO}	450	V
Emitter-Base Voltage	V _{EBO}	9	V
Collector Current(DC)	I _C	1.5	A
Collector Current(Pulsed)	I _{CP}	3 (Note)	A
Base Current	I _B	0.2	A
Power Dissipation(T _A =25°C)	P _d	1.5	W
Power Dissipation(T _C =25°C)		20	W
Junction Temperature	T _j	150	°C
Storage Temperature	T _{stg}	-55~+150	°C

Note : Single pulse, Pw≤300μs, Duty Cycle≤2%.

Characteristics (Ta=25°C)

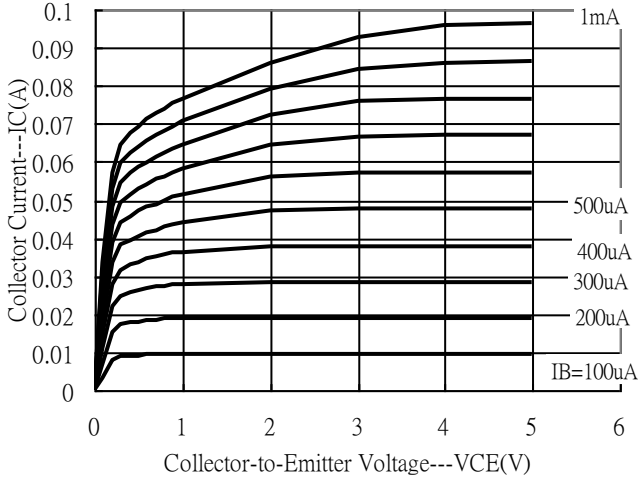
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CBO}	700	-	-	V	I _C =100μA
BV _{CEO}	450	-	-	V	I _C =10mA
BV _{EBO}	9	-	-	V	I _E =100μA
I _{CBO}	-	-	1	μA	V _{CB} =700V, I _E =0
I _{CEO}	-	-	50	μA	V _{CE} =400V, I _E =0
I _{EBO}	-	-	100	nA	V _{EB} =9V, I _C =0
*V _{CE(SAT)}	-	136	300	mV	I _C =500mA, I _B =100mA
*V _{CE(SAT)}	-	256	600	mV	I _C =1A, I _B =250mA
*V _{CE(SAT)}	-	400	800	mV	I _C =1.5A, I _B =500mA
*V _{BE(SAT)}	-	0.84	1	V	I _C =500mA, I _B =100mA
*V _{BE(SAT)}	-	0.92	1.2	V	I _C =1A, I _B =250mA
*h _{FE 1}	18	-	36	-	V _{CE} =2V, I _C =500mA
*h _{FE 2}	5	-	21	-	V _{CE} =2V, I _C =1A
f _T	5	-	-	MHZ	V _{CE} =10V, I _C =100mA, f=100MHZ
t _{stg}	-	-	0.5	μS	V _{CC} =100V, I _C =1A, I _{B1} =-I _{B2} =0.2A, I _C =0.25A
t _f	1.8	-	6.6		

*Pulse Test: Pulse Width ≤380μs, Duty Cycle≤2%

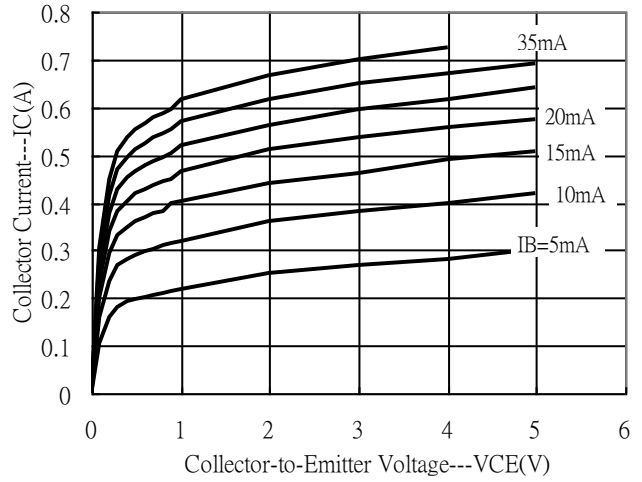


Typical Characteristics

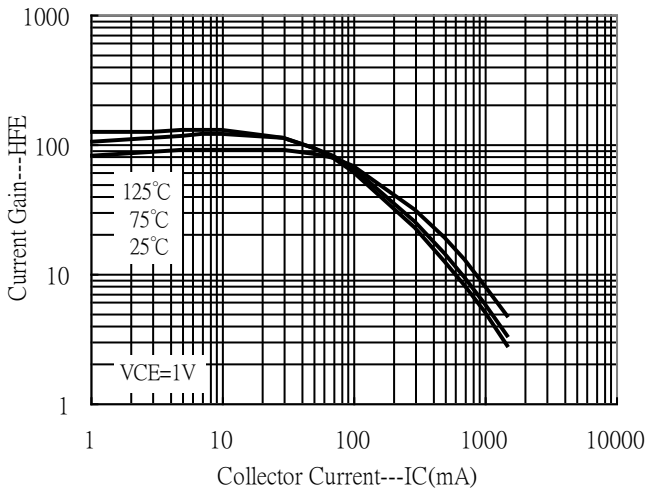
Emitter Grounded Output Characteristics



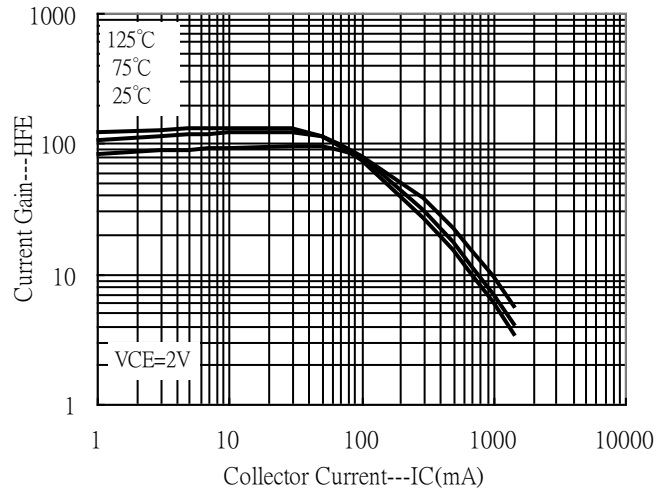
Emitter Grounded Output Characteristics



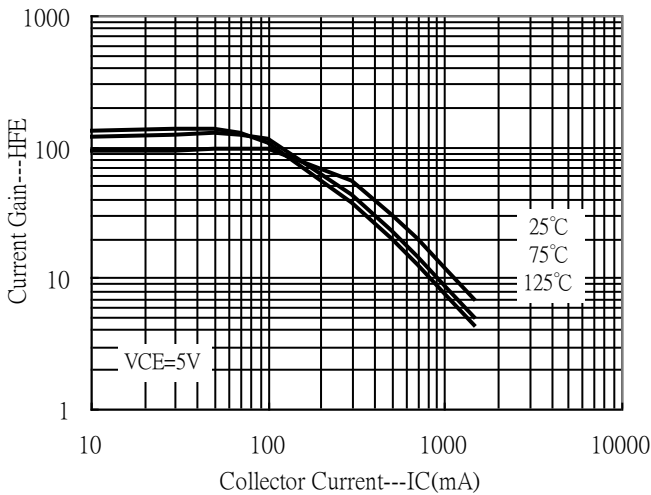
Current Gain vs Collector Current



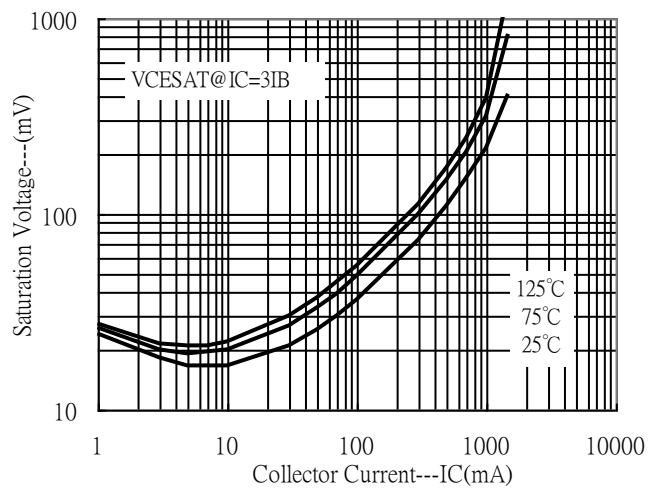
Current Gain vs Collector Current



Current Gain vs Collector Current



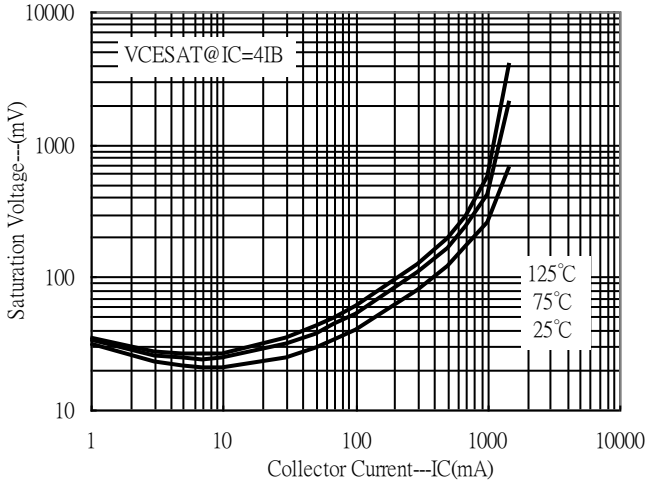
Saturation Voltage vs Collector Current



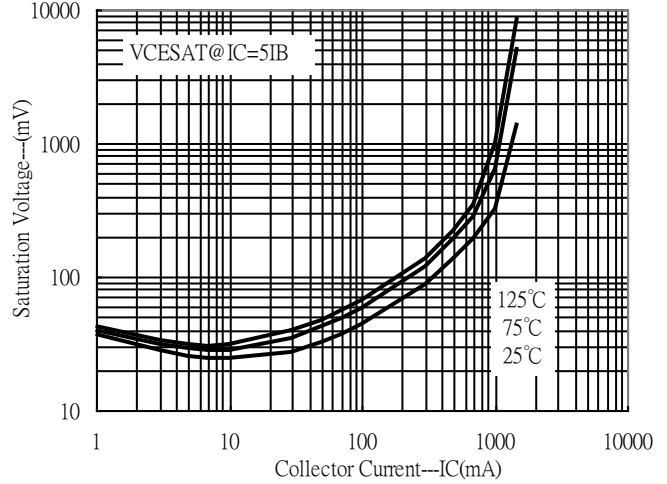


Typical Characteristics(Cont.)

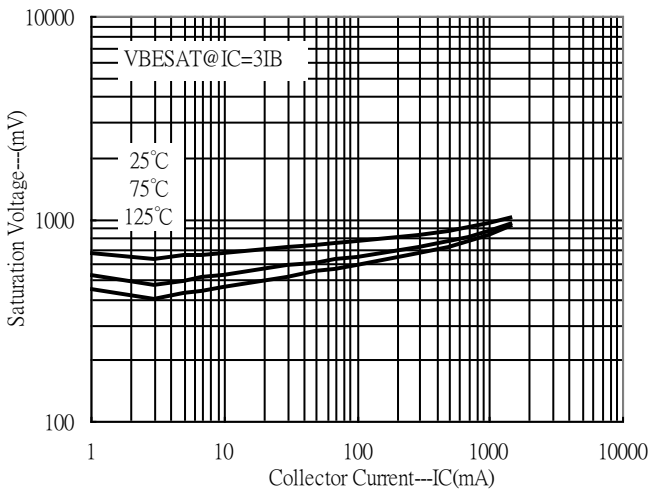
Saturation Voltage vs Collector Current



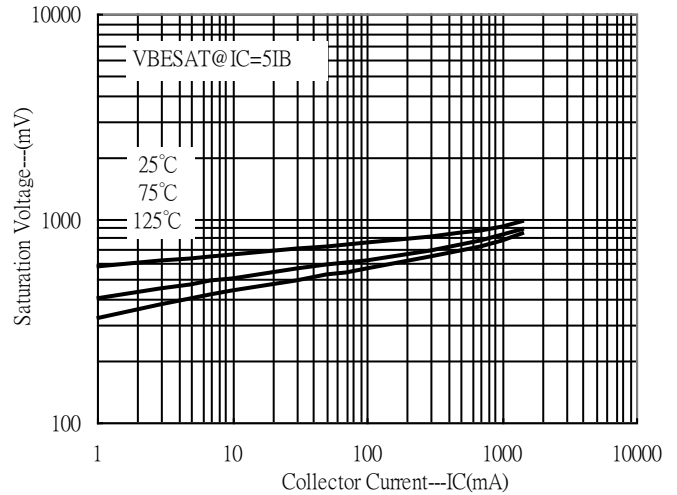
Saturation Voltage vs Collector Current



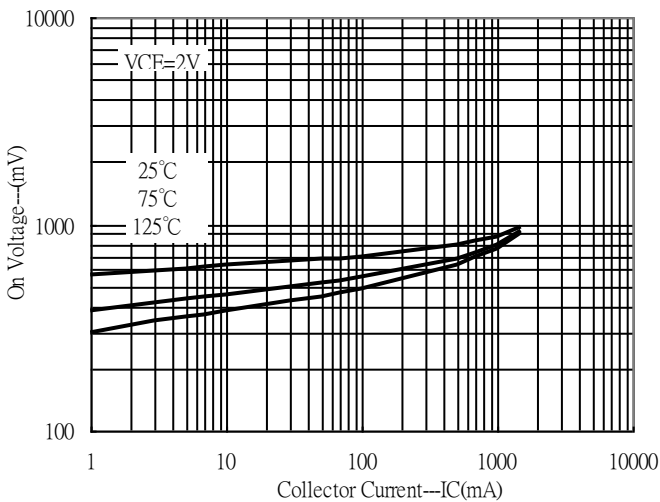
Saturation Voltage vs Collector Current



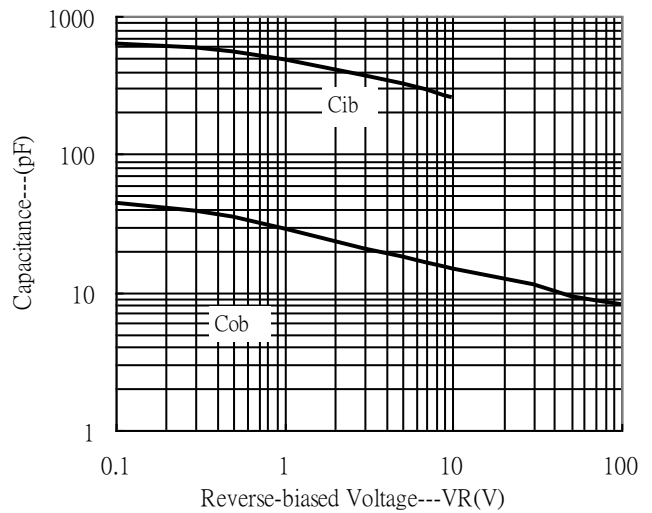
Saturation Voltage vs Collector Current



On Voltage vs Collector Current



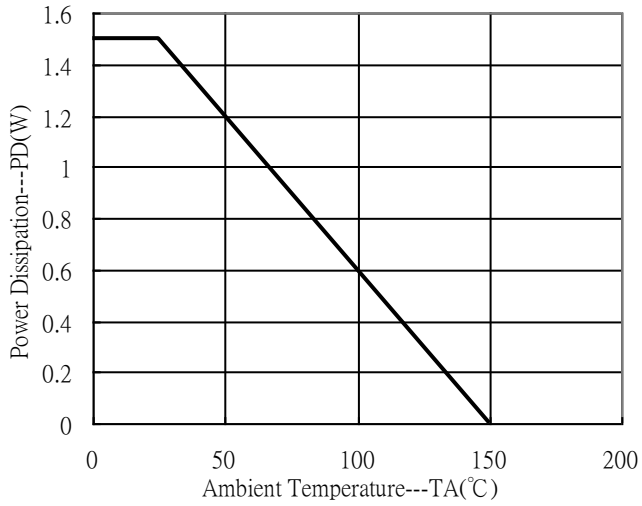
Capacitance vs Reverse-biased Voltage



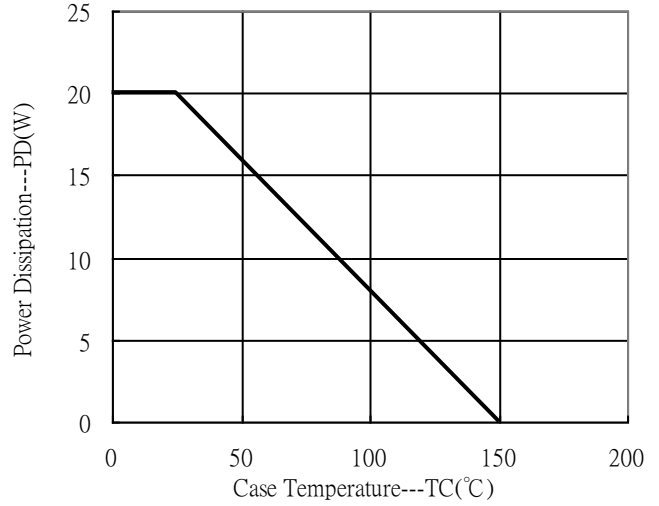


Typical Characteristics(Cont.)

Power Derating Curve

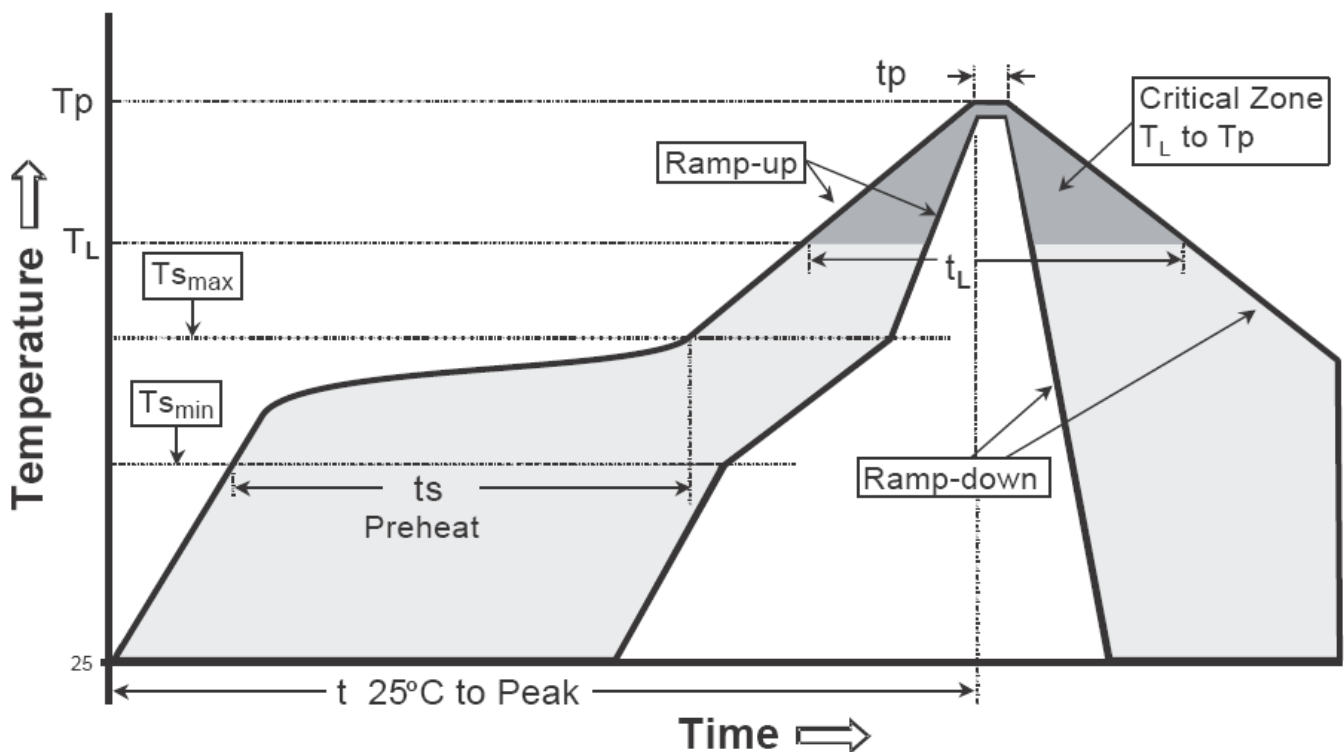


Power Derating Curve



Recommended wave soldering condition

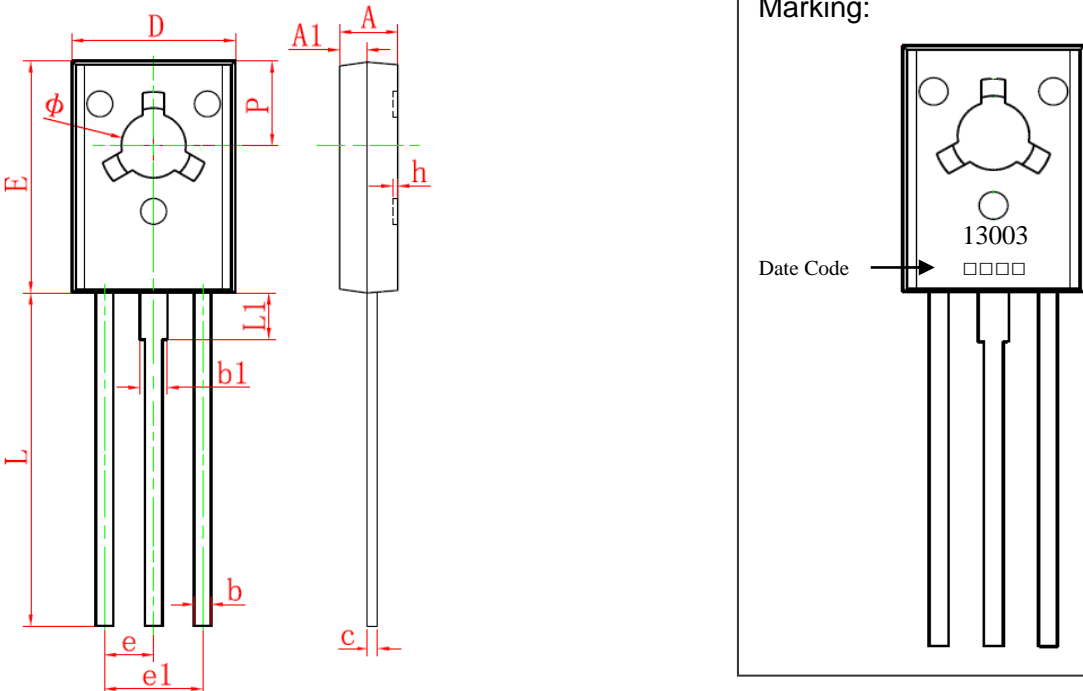
Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

Recommended temperature profile for IR reflow


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-126 Dimension



Marking:

Date Code → □□□□

Style: Pin 1.Base 2.Collector 3.Emitter

3-Lead TO-126 Plastic Package
 CYStek Package Code: T3

*: Typical

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	2.500	2.900	0.098	0.114	e	*2.290		*0.090	
A1	1.100	1.500	0.043	0.059	e1	4.480	4.680	0.176	0.184
b	0.660	0.860	0.026	0.034	h	0.000	0.300	0.000	0.012
b1	1.170	1.370	0.046	0.054	L	15.300	15.700	0.602	0.618
c	0.450	0.600	0.018	0.024	L1	2.100	2.300	0.083	0.091
D	7.400	7.800	0.291	0.307	P	3.900	4.100	0.154	0.161
E	10.600	11.000	0.417	0.433	Φ	3.000	3.200	0.118	0.126

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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