

# Low Vcesat NPN Epitaxial Planar Transistor

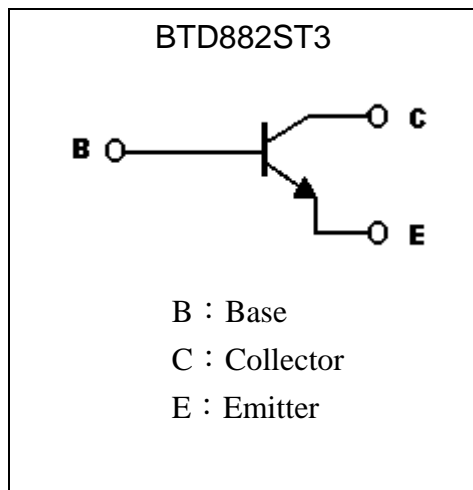
## BTD882ST3

$BV_{CEO}$	30V
$I_C$	3A
$R_{CESAT}(typ)$	150mΩ

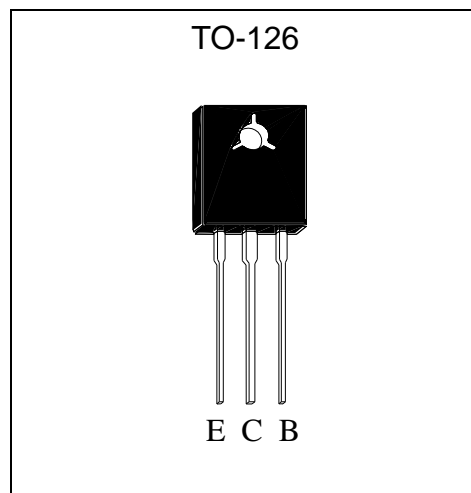
### Features

- Low  $V_{CE(sat)}$ , 0.3V typ. at  $I_C / I_B = 2A / 0.2A$
- Excellent current gain characteristics
- Complementary to BTB772ST3
- Pb-free lead plating package

### Symbol

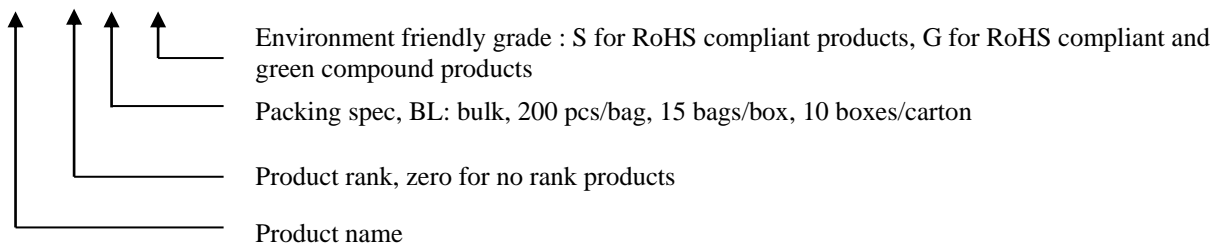


### Outline



### Ordering Information

Device	Package	Shipping
BTD882ST3-X-BL-X	TO-126 (Pb-free lead plating package)	200 pcs / bag, 3,000 pcs/box , 30,000 pcs/carton





**Absolute Maximum Ratings** (Ta=25°C)

Parameter	Symbol	Limit	Unit
Collector-Base Voltage	V <sub>CBO</sub>	60	V
Collector-Emitter Voltage	V <sub>CEO</sub>	30	V
Emitter-Base Voltage	V <sub>EBO</sub>	6	V
Collector Current	I <sub>C</sub> (DC)	3	A
	I <sub>C</sub> (Pulse)	7 *1	A
Power Dissipation	P <sub>d</sub> (Ta=25°C)	1	W
	P <sub>d</sub> (Tc=25°C)	10	
Operating Junction and Storage Temperature Range	T <sub>j</sub> ; T <sub>stg</sub>	-55~+150	°C

Note : \*1. Single Pulse Pw ≤ 350μs, Duty ≤ 2%.

**Characteristics** (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV <sub>CBO</sub>	60	-	-	V	I <sub>C</sub> =50μA, I <sub>E</sub> =0
BV <sub>CEO</sub>	30	-	-	V	I <sub>C</sub> =1mA, I <sub>B</sub> =0
BV <sub>EBO</sub>	6	-	-	V	I <sub>E</sub> =50μA, I <sub>C</sub> =0
I <sub>CBO</sub>	-	-	100	nA	V <sub>CB</sub> =60V, I <sub>E</sub> =0
I <sub>EBO</sub>	-	-	100	nA	V <sub>EB</sub> =6V, I <sub>C</sub> =0
*V <sub>CE(sat)</sub>	-	0.3	0.5	V	I <sub>C</sub> =2A, I <sub>B</sub> =0.2A
*R <sub>CE(sat)</sub>	-	0.15	0.25	Ω	I <sub>C</sub> =2A, I <sub>B</sub> =0.2A
*V <sub>BE(sat)</sub>	-	-	1.5	V	I <sub>C</sub> =2A, I <sub>B</sub> =0.2A
*h <sub>FE1</sub>	160	-	-	-	V <sub>CE</sub> =2V, I <sub>C</sub> =20mA
*h <sub>FE2</sub>	180	-	390	-	V <sub>CE</sub> =2V, I <sub>C</sub> =500mA
*h <sub>FE3</sub>	150	-	-	-	V <sub>CE</sub> =2V, I <sub>C</sub> =1A
f <sub>T</sub>	-	270	-	MHz	V <sub>CE</sub> =5V, I <sub>C</sub> =0.5A, f=100MHz
Cob	-	16	-	pF	V <sub>CB</sub> =10V, f=1MHz

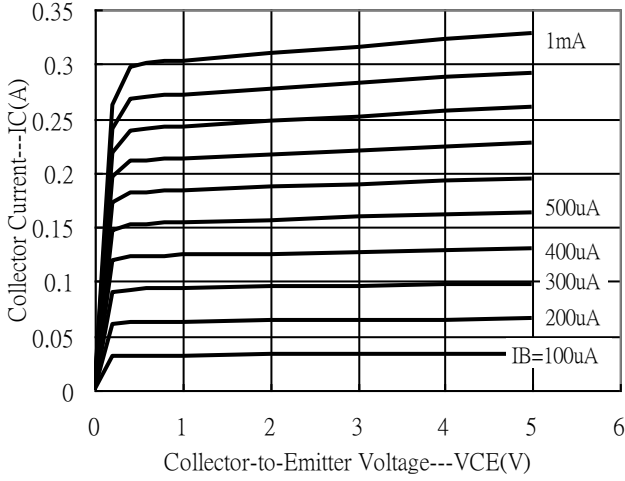
\*Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%

**Classification Of hFE 2**

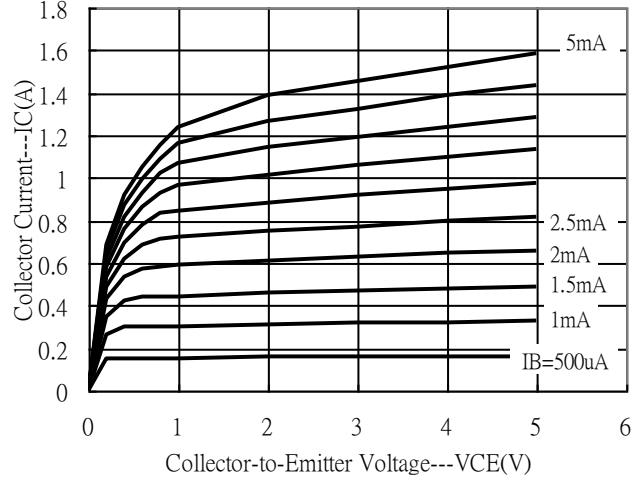
Rank	P
Range	180~390

**Typical Characteristics**

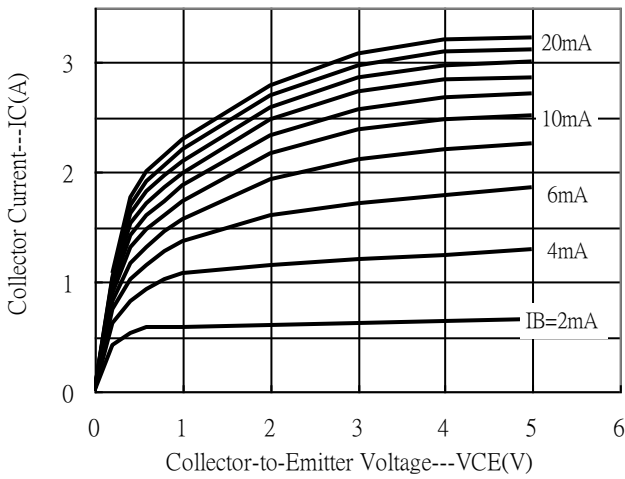
Emitter Grounded Output Characteristics



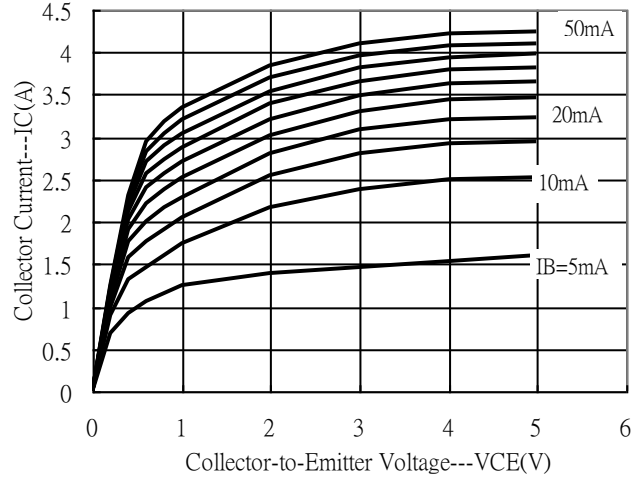
Emitter Grounded Output Characteristics



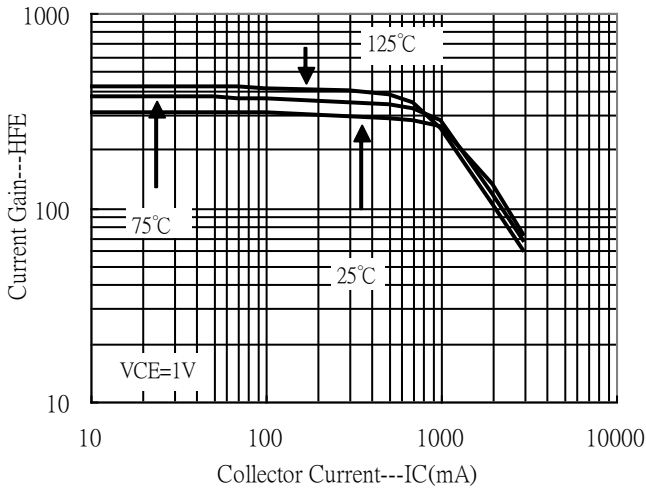
Emitter Grounded Output Characteristics



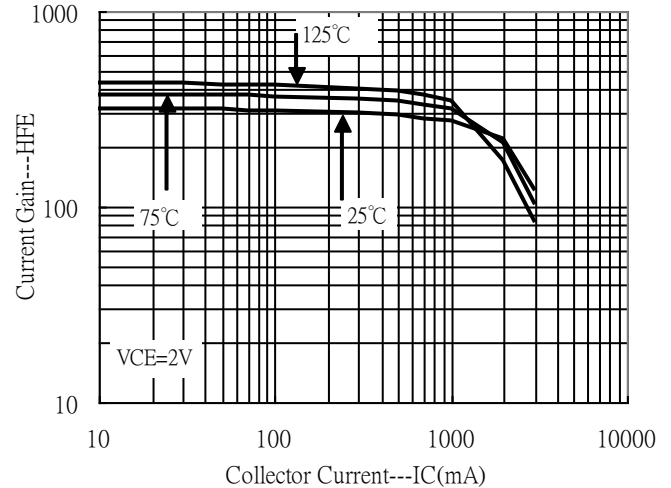
Emitter Grounded Output Characteristics



Current Gain vs Collector Current

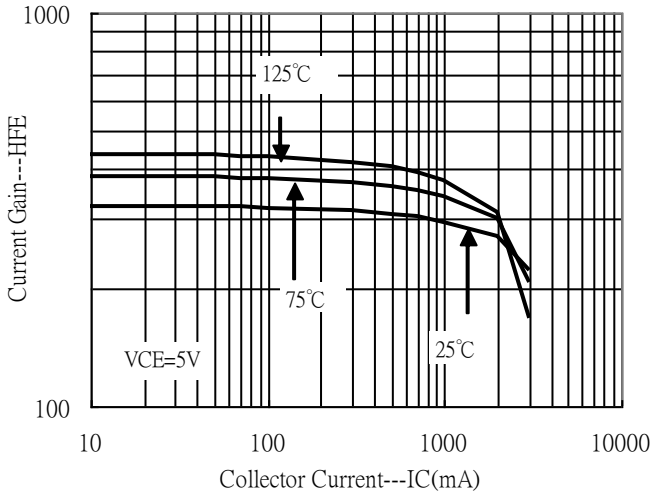


Current Gain vs Collector Current

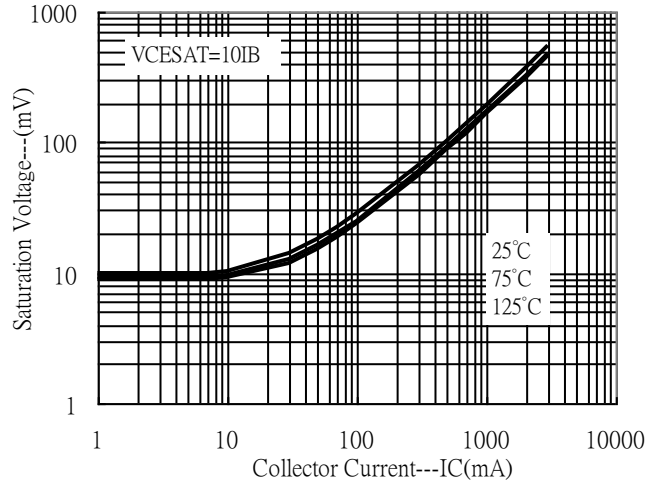


**Typical Characteristics(Cont.)**

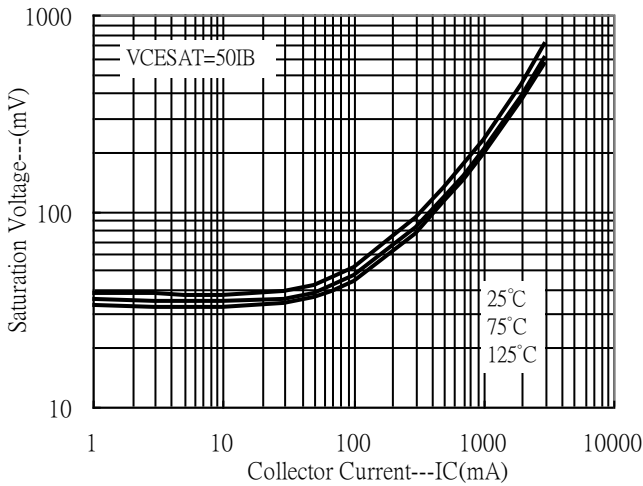
Current Gain vs Collector Current



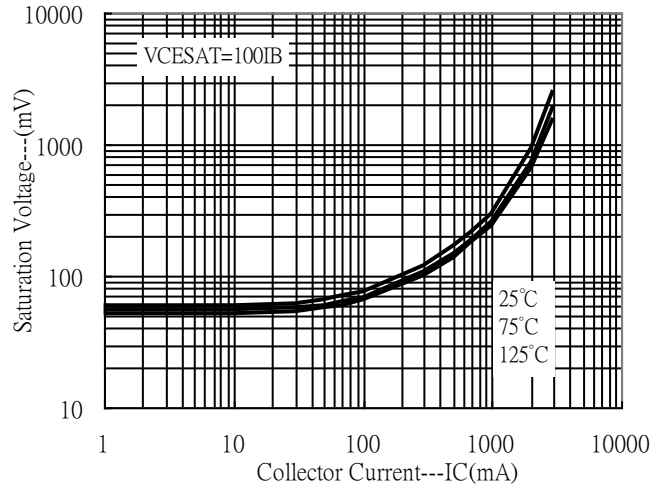
Saturation Voltage vs Collector Current



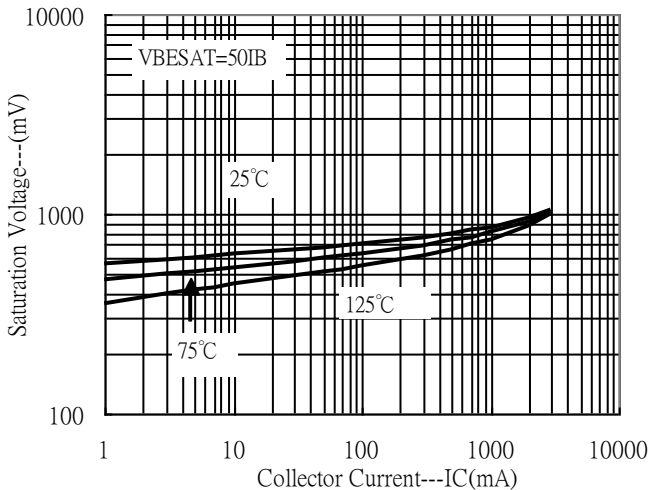
Saturation Voltage vs Collector Current



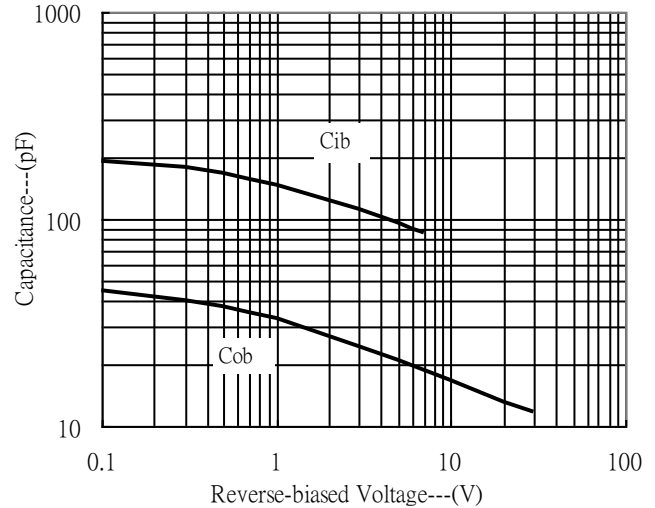
Saturation Voltage vs Collector Current



Saturation Voltage vs Collector Current

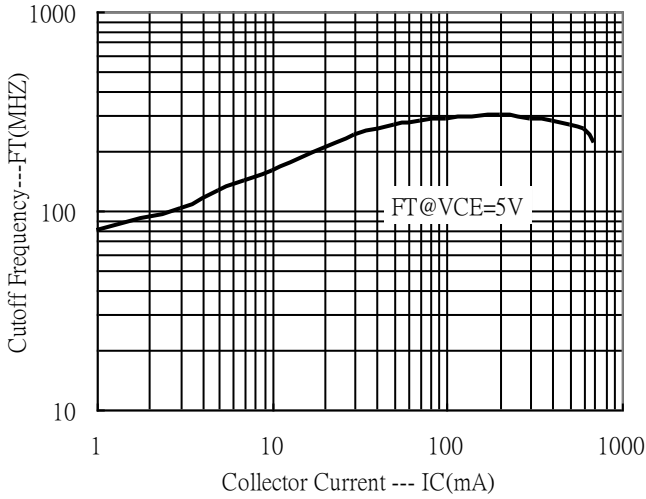


Capacitance vs Reverse-biased Voltage

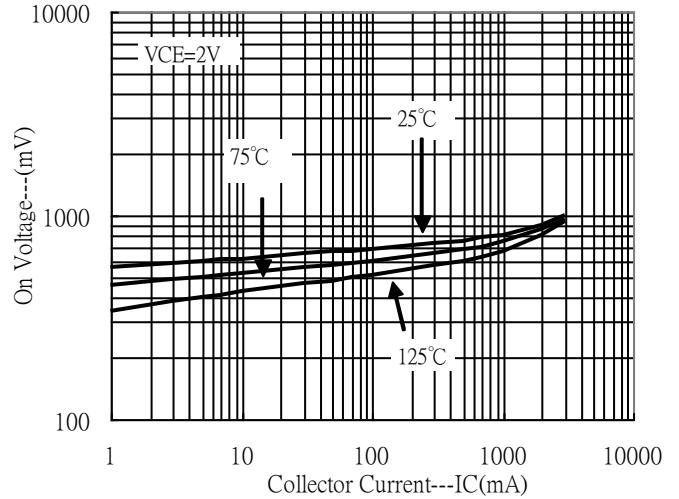


**Typical Characteristics(Cont.)**

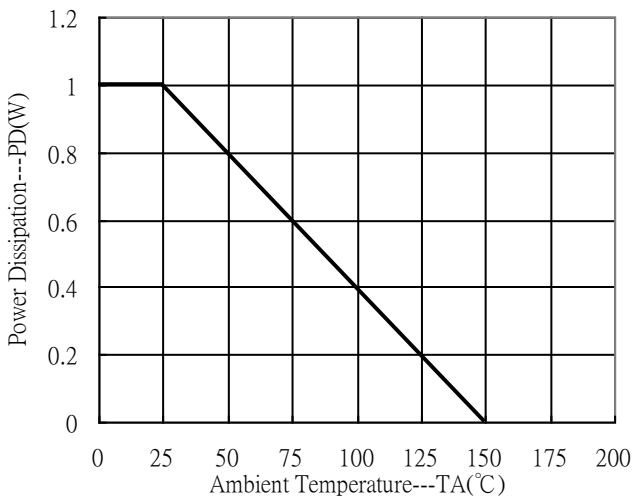
Cutoff Frequency vs Collector Current



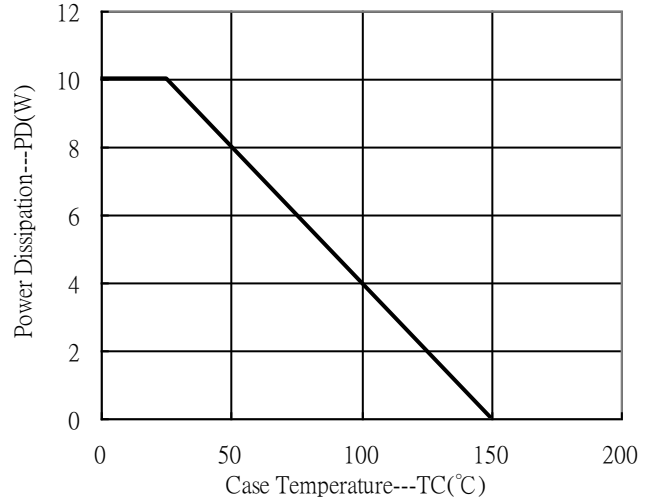
On Voltage vs Collector Current



Power Derating Curve



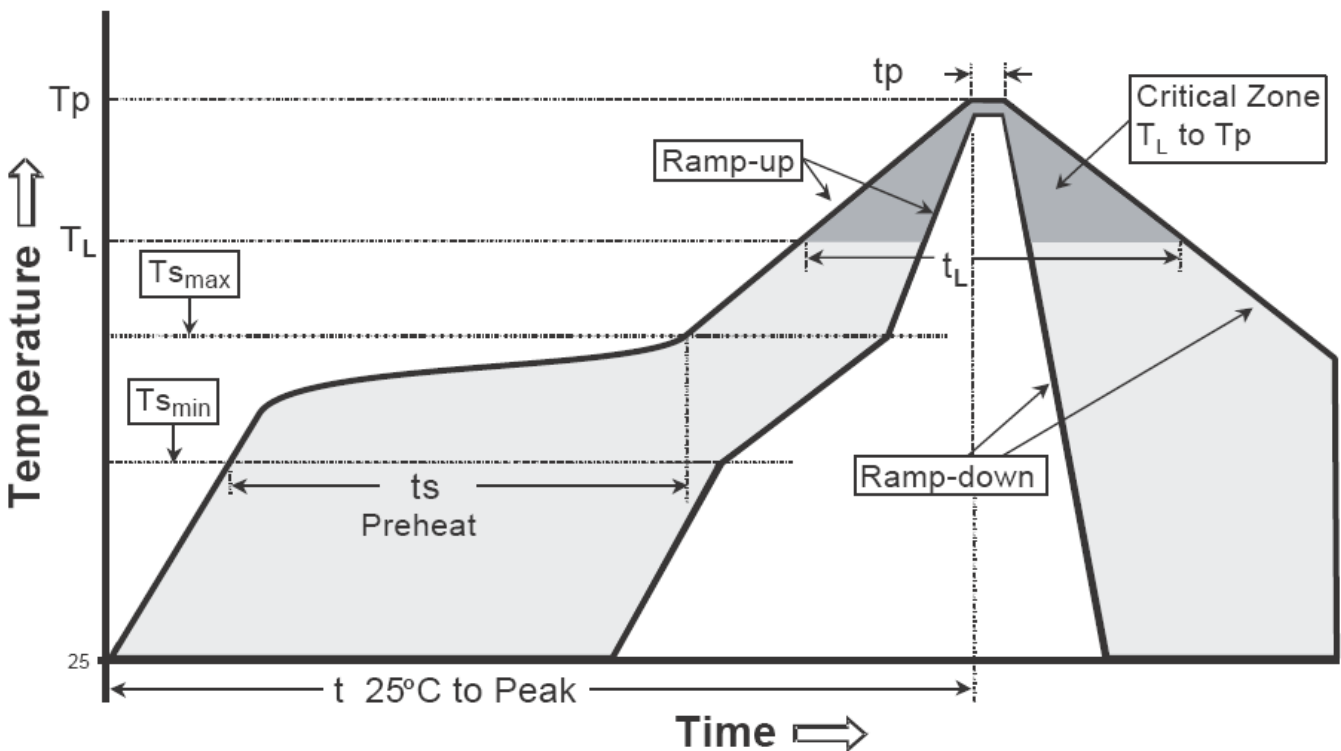
Power Derating Curve



**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

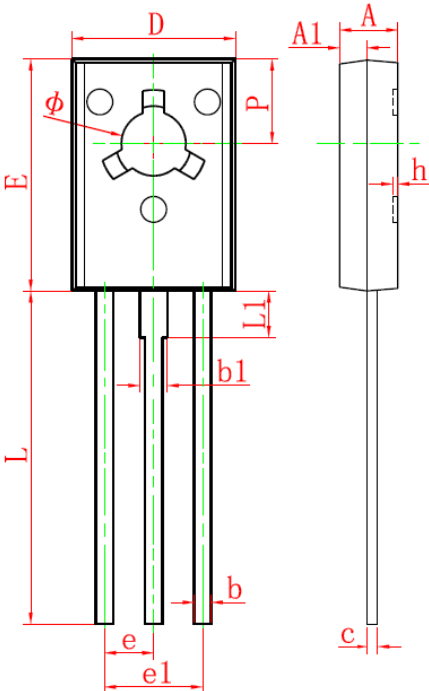
**Recommended temperature profile for IR reflow**



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

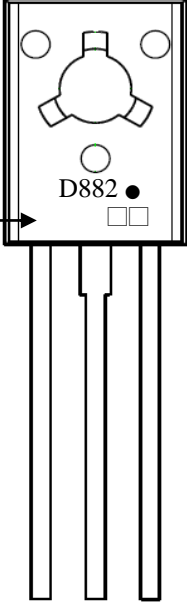
Note : All temperatures refer to topside of the package, measured on the package body surface.

**TO-126 Dimension**



The diagram shows two views of a TO-126 package. The left view is a top-down perspective showing dimensions: D (width), E (height), P (pitch),  $\phi$  (lead diameter), L (total length), L1 (lead length), b (lead width), b1 (lead thickness), e (lead spacing), and e1 (lead pitch). The right view is a side profile showing dimensions: A (width), A1 (lead thickness), h (lead height), and c (lead diameter).

Marking:



The marking diagram shows the top of the package with a central circular logo, a date code 'D882' with a dot, and two small squares. An arrow points to the date code area.

Style: Pin 1. Emitter 2. Collector 3. Base

3-Lead TO-126 Plastic Package  
 CYStek Package Code: T3

\*: Typical

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	2.500	2.900	0.098	0.114	e	*2.290		*0.090	
A1	1.100	1.500	0.043	0.059	e1	4.480	4.680	0.176	0.184
b	0.660	0.860	0.026	0.034	h	0.000	0.300	0.000	0.012
b1	1.170	1.370	0.046	0.054	L	15.300	15.700	0.602	0.618
c	0.450	0.600	0.018	0.024	L1	2.100	2.300	0.083	0.091
D	7.400	7.800	0.291	0.307	P	3.900	4.100	0.154	0.161
E	10.600	11.000	0.417	0.433	$\Phi$	3.000	3.200	0.118	0.126

- Notes:
- Controlling dimension: millimeters.
  - Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
  - If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

**Important Notice:**

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.