

Low Vcesat NPN Epitaxial Planar Transistor

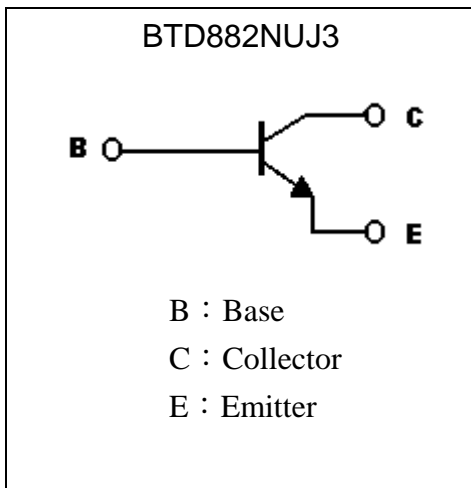
BTD882NUJ3

BV_{CEO}	30V
I_C	3A

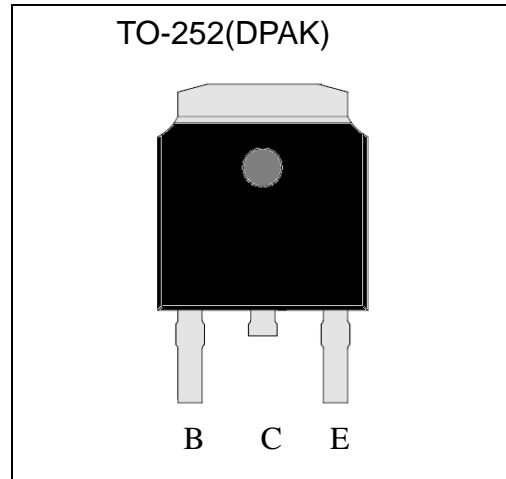
Features

- Low $V_{CE(sat)}$, 0.2V typ. at $I_C / I_B = 2A / 0.2A$
- Excellent current gain characteristics
- Complementary to BTB772NUJ3
- Pb-free lead plating and halogen-free package

Symbol

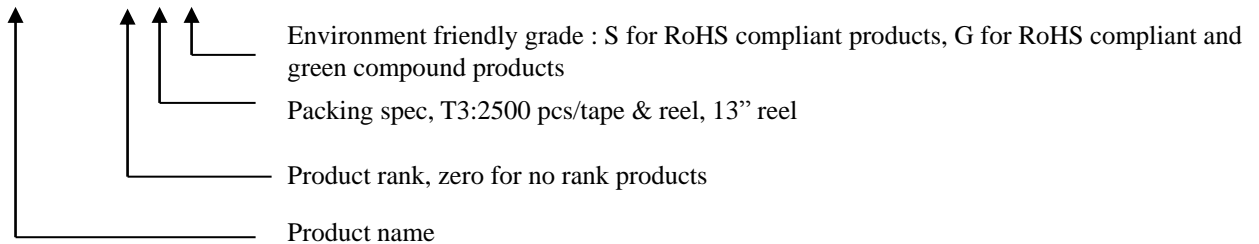


Outline



Ordering Information

Device	Package	Shipping
BTD882NUJ3-P-T3-G	TO-252 (Pb-free lead plating and halogen-free package)	2500 pcs / Tape & Reel





Absolute Maximum Ratings (Ta=25°C)

Parameter		Symbol	Limit	Unit
Collector-Base Voltage		V _{CB0}	40	V
Collector-Emitter Voltage		V _{CEO}	30	V
Emitter-Base Voltage		V _{EBO}	9	V
Collector Current	DC	I _C	3	A
	Pulse		7 *1	A
Power Dissipation	Ta=25°C	P _D	1	W
	Tc=25°C		10	
Operating Junction and Storage Temperature Range		T _j ; T _{stg}	-55~+150	°C

Note : *1. Single Pulse Pw ≤ 350μs, Duty ≤ 2%.

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance, Junction-to-Ambient, max	R _{θJA}	125	°C/W
Thermal Resistance, Junction-to-Case, max	R _{θJC}	12.5	

Characteristics (Ta=25°C)

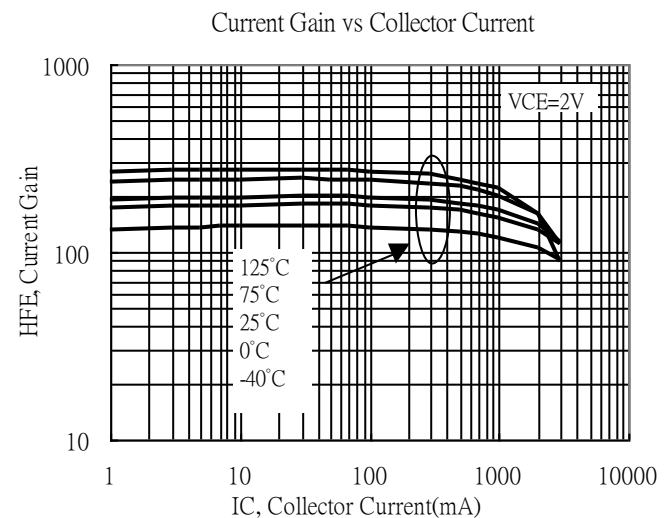
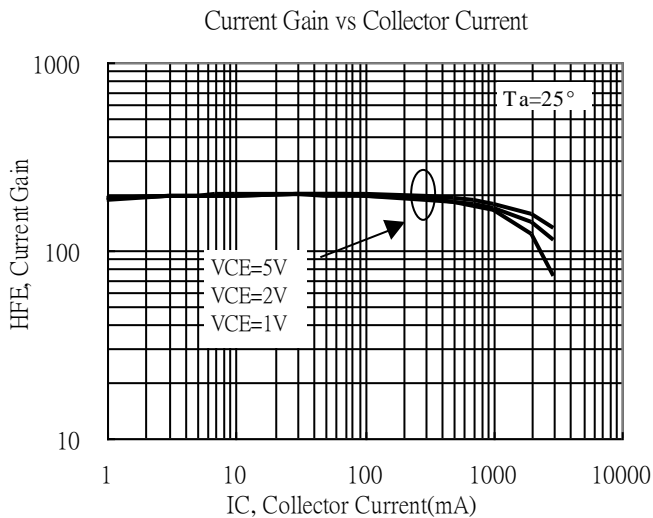
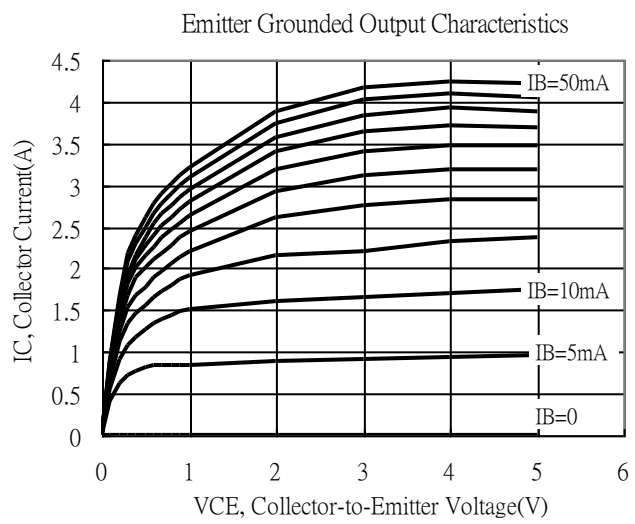
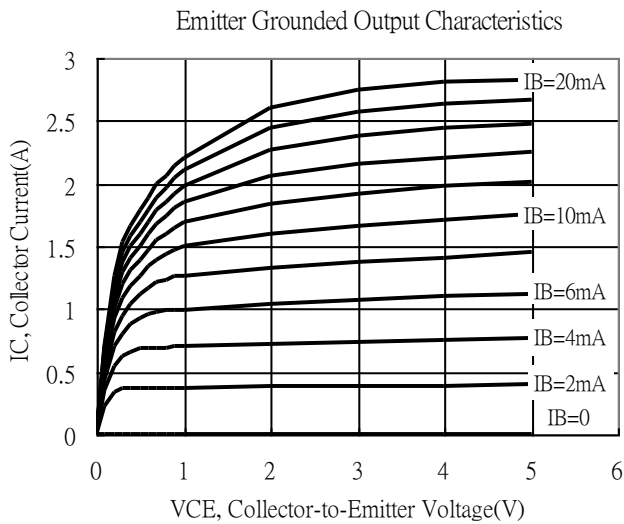
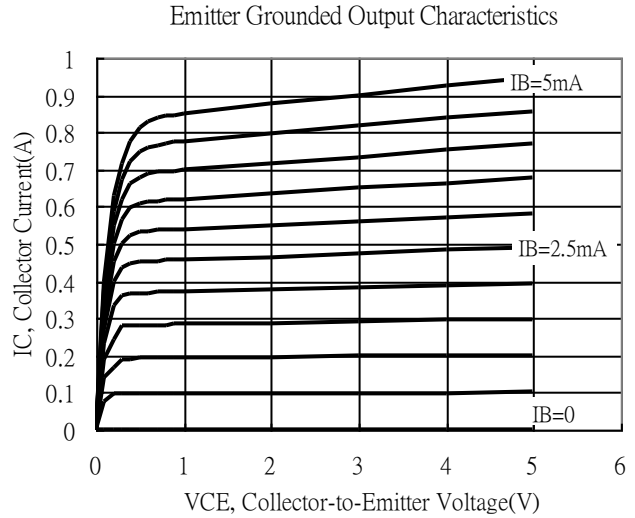
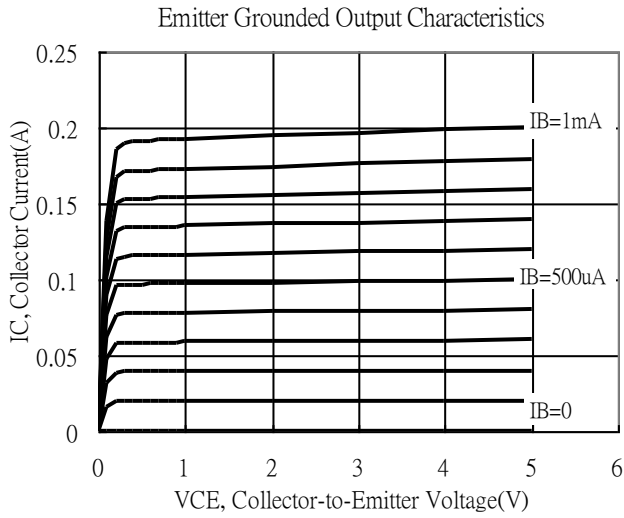
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CB0}	40	-	-	V	I _C =50μA, I _E =0
BV _{CEO}	30	-	-	V	I _C =1mA, I _B =0
BV _{EBO}	9	-	-	V	I _E =50μA, I _C =0
I _{CB0}	-	-	100	nA	V _{CB} =40V, I _E =0
I _{EBO}	-	-	100	nA	V _{EB} =6V, I _C =0
*V _{CE(sat)}	-	0.2	0.5	V	I _C =2A, I _B =0.2A
*V _{BE(sat)}	-	1	1.5	V	I _C =2A, I _B =0.2A
*h _{FE 1}	100	-	-	-	V _{CE} =2V, I _C =20mA
*h _{FE 2}	160	-	320	-	V _{CE} =2V, I _C =1A
f _T	-	90	-	MHz	V _{CE} =5V, I _C =0.1A, f=100MHz
Cob	-	17	-	pF	V _{CB} =10V, f=1MHz

*Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%

Classification Of hFE 2

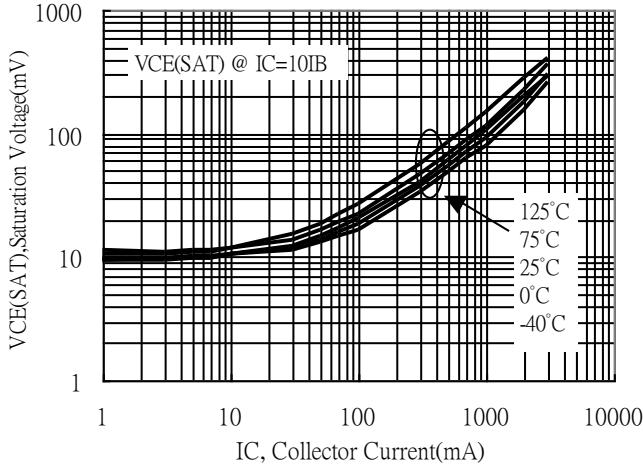
Rank	P
Range	160~320

Typical Characteristics

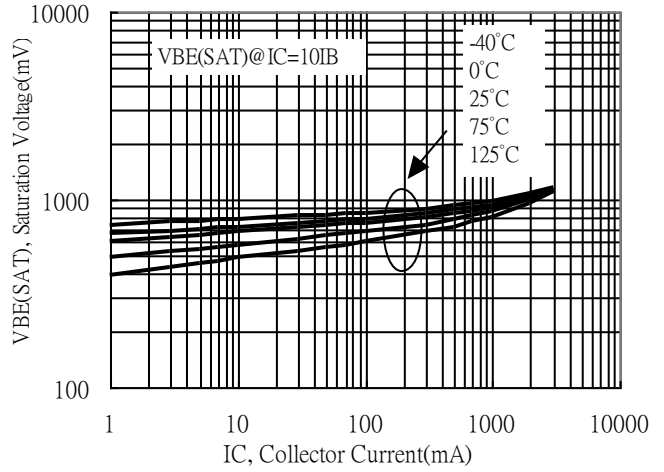


Typical Characteristics(Cont.)

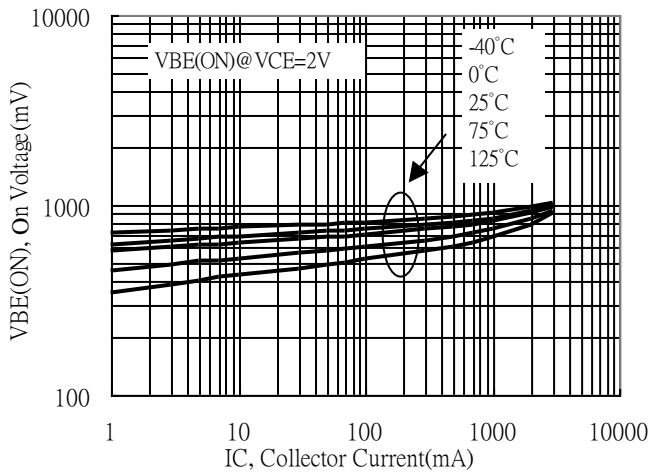
Saturation Voltage vs Collector Current



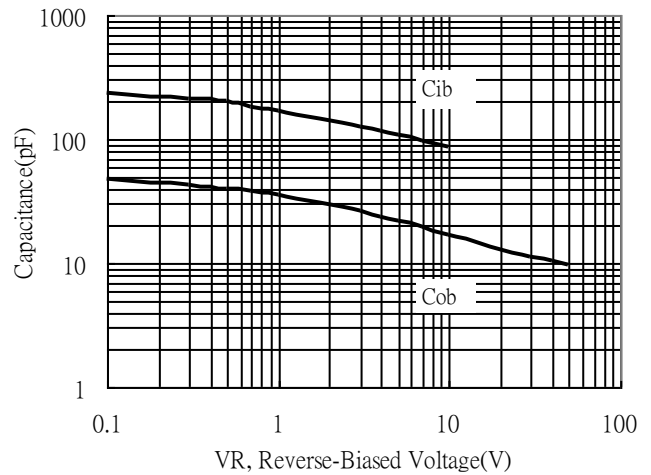
Saturation Voltage vs Collector Current



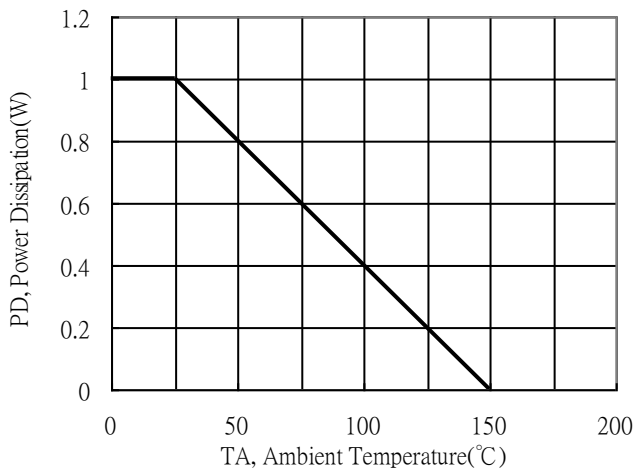
Saturation Voltage vs Collector Current



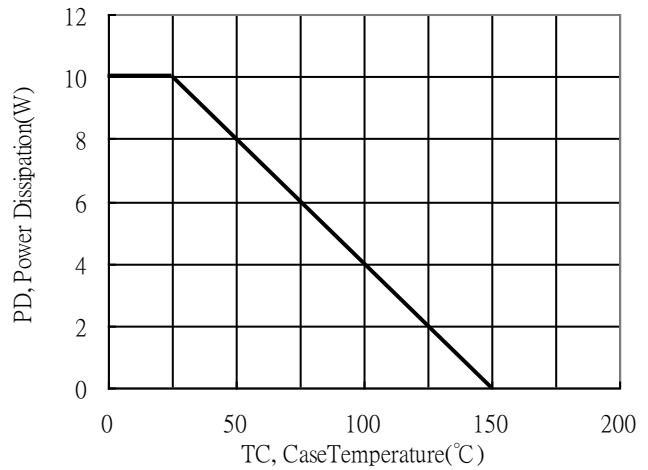
Capacitance vs Reverse-Biased Voltage



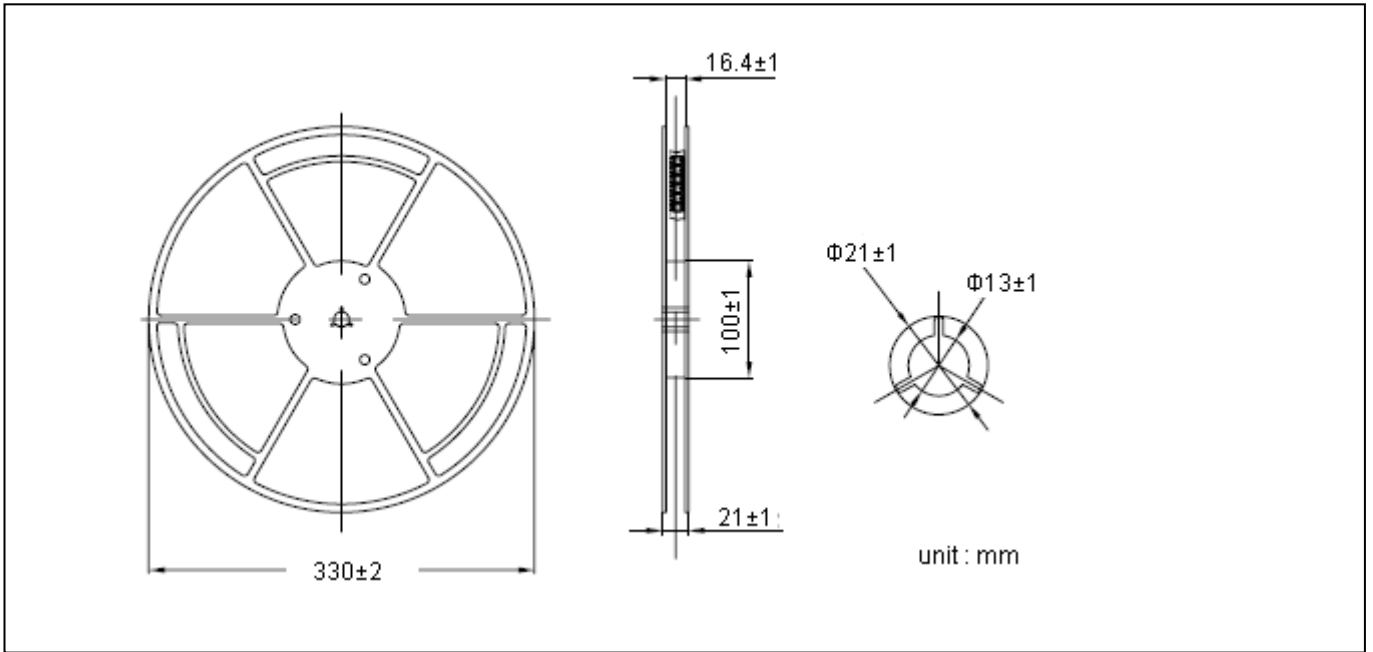
Power Derating Curve



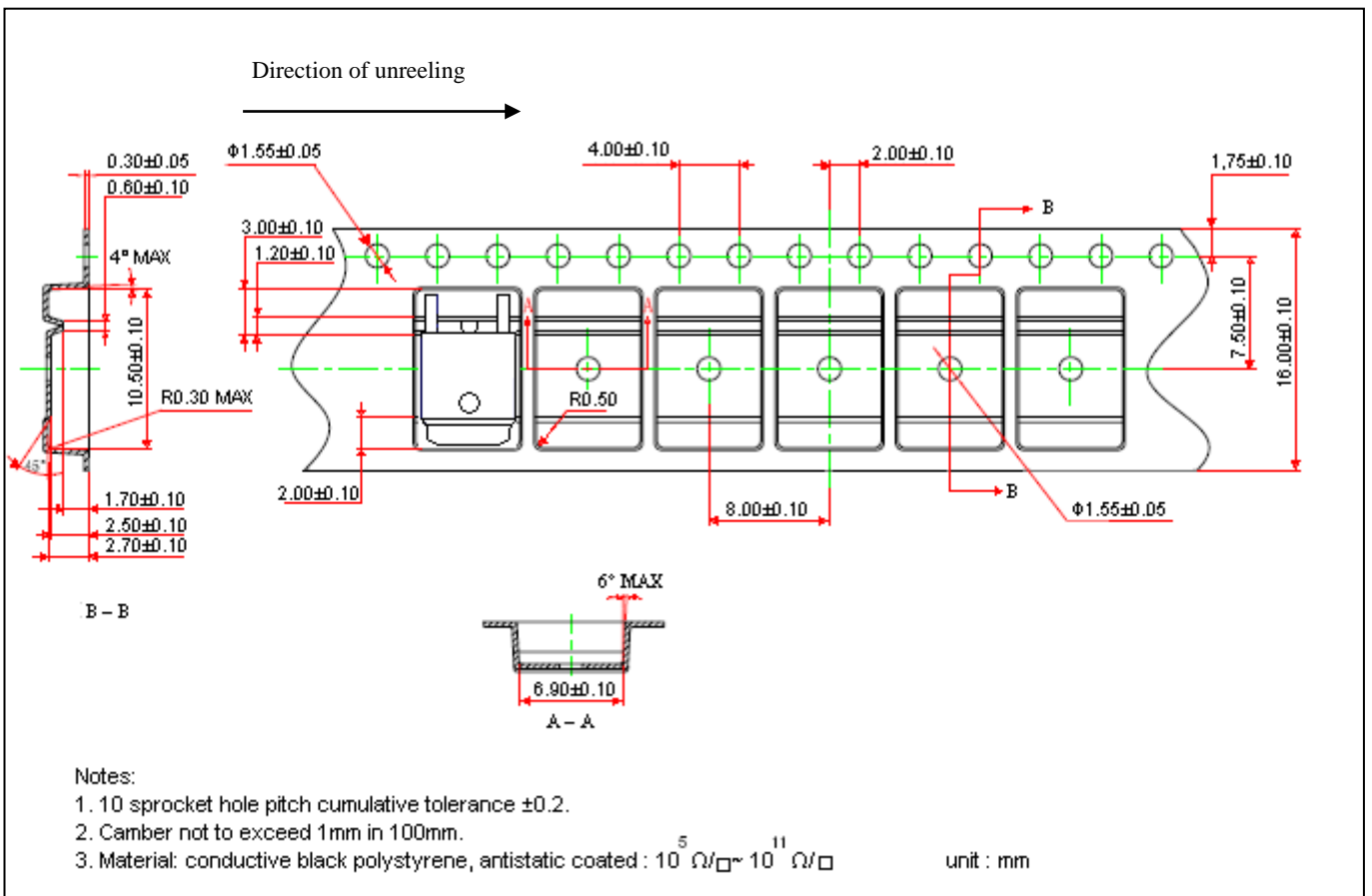
Power Derating Curve



Reel Dimension

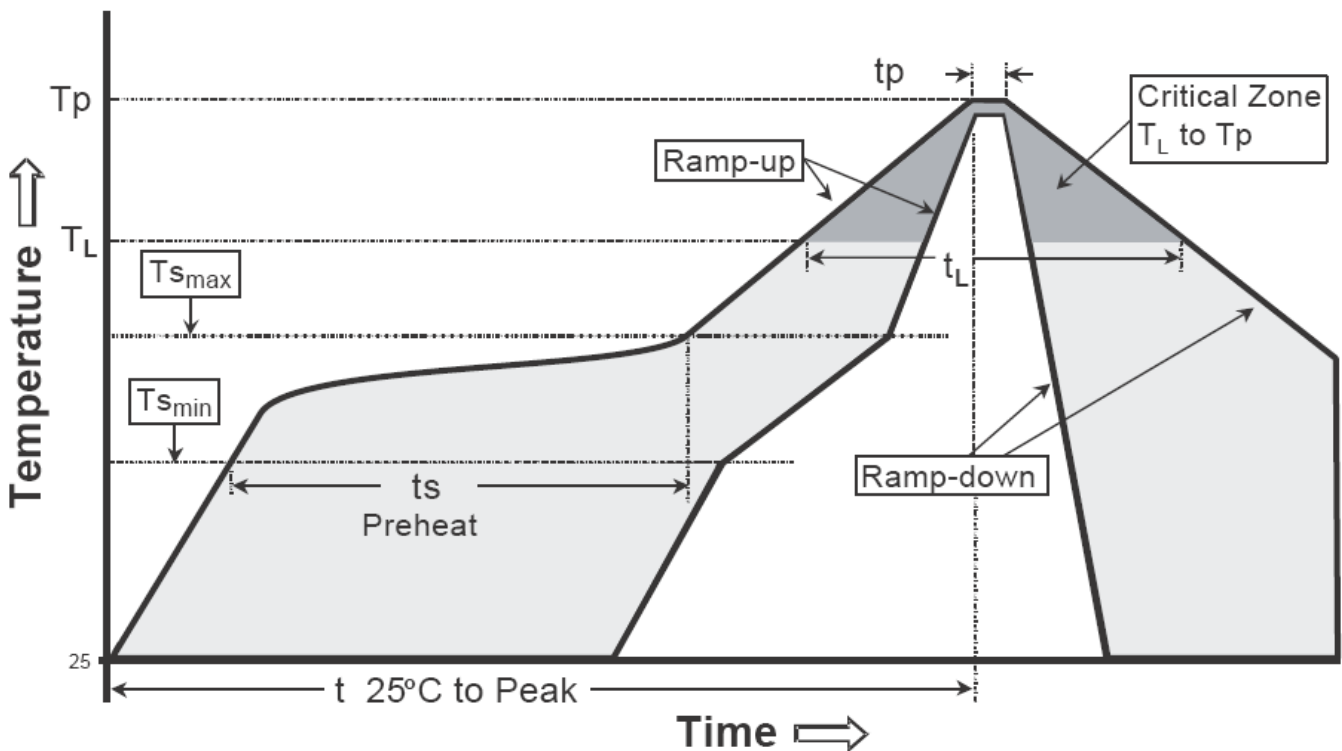


Carrier Tape Dimension



Recommended wave soldering condition

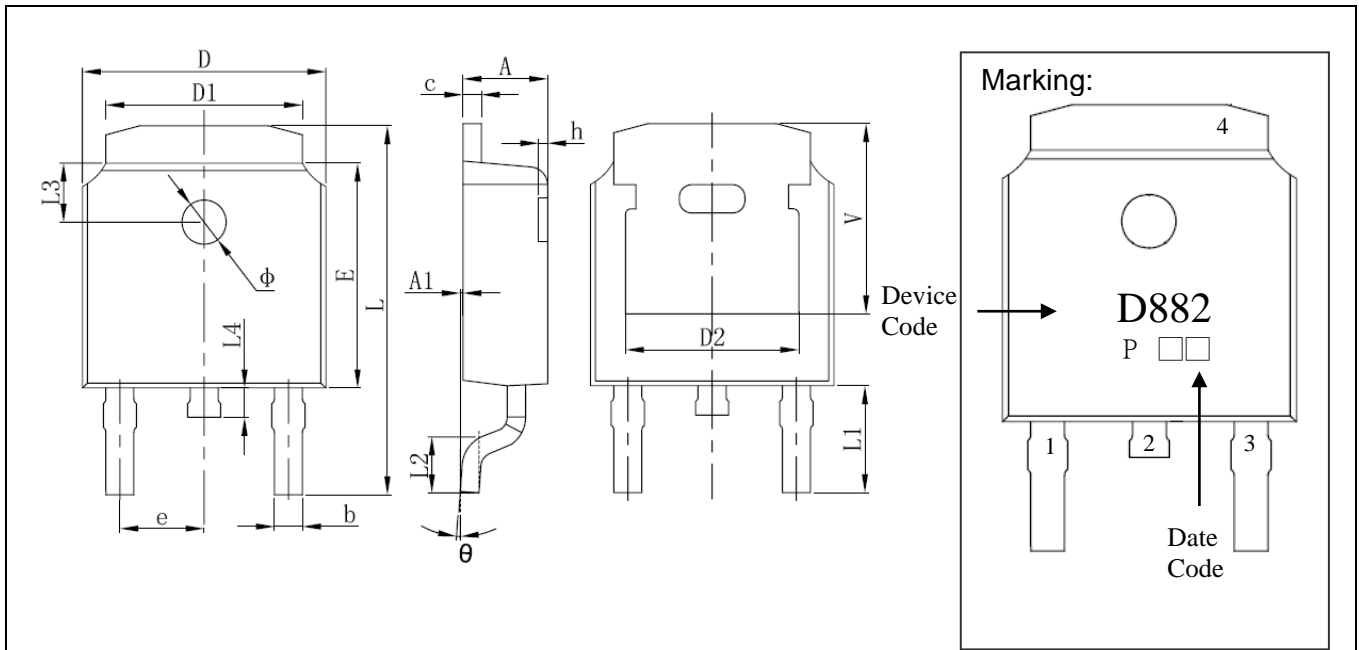
Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

Recommended temperature profile for IR reflow


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-252 Dimension



3-Lead TO-252 Plastic Surface Mount Package
 CYStek Package Code: J3

Date Code :
 First code : Year code, Last digit of Christian Year
 Second Code : Month code, 1~9, A, B, C

Style: Pin 1.Base 2.Collector 3.Emitter 4.Collector

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.087	0.094	2.200	2.400	L	0.382	0.406	9.712	10.312
A1	0.000	0.005	0.000	0.127	L1	0.114	REF	2.900	REF
b	0.025	0.030	0.635	0.770	L2	0.055	0.067	1.400	1.700
c	0.018	0.023	0.460	0.580	L3	0.063	REF	1.600	REF
D	0.256	0.264	6.500	6.700	L4	0.024	0.039	0.600	1.000
D1	0.201	0.215	5.100	5.460	Φ	0.043	0.051	1.100	1.300
D2	0.190	REF	4.830	REF	θ	0°	8°	0°	8°
E	0.236	0.244	6.000	6.200	h	0.000	0.012	0.000	0.300
e	0.086	0.094	2.186	2.386	v	0.207	REF	5.250	REF

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:
 • Lead : Pure tin plated.
 • Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:
 • All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
 • CYStek reserves the right to make changes to its products without notice.
 • CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
 • CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.