

General Purpose NPN Epitaxial Planar Transistor

BTD1768S3

BV_{CEO}	80V
I_C	1A

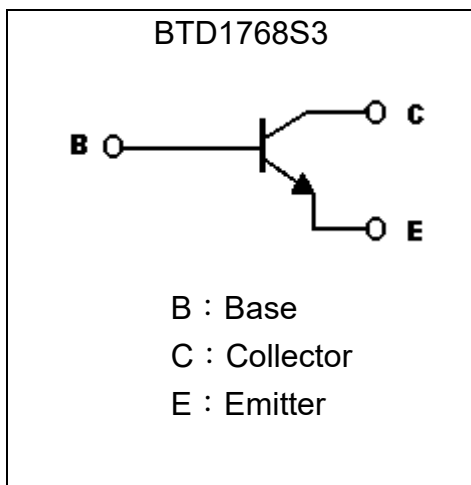
Description

The BTD1768S3 is designed for use in driver and output stages of AF amplifier and general purpose application.

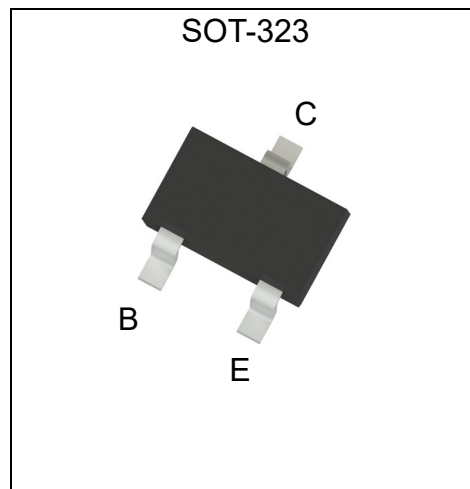
Features

- Low collector saturation voltage
- High breakdown voltage, $V_{CEO}=80V$ (min.)
- High collector current, $I_{C(max)}=1A$ (DC)
- Pb-free package

Symbol

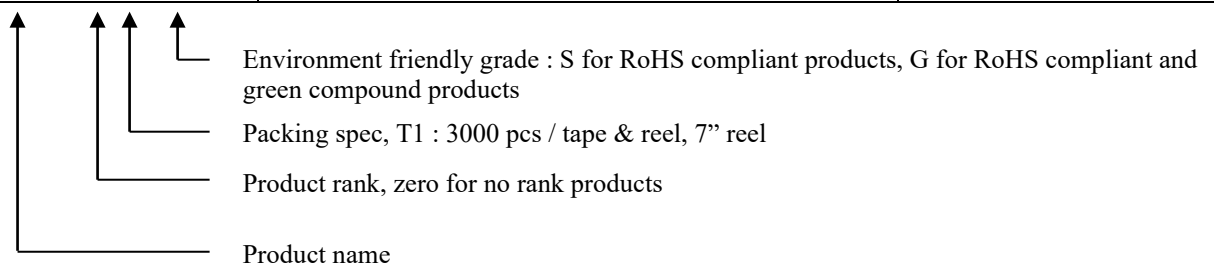


Outline



Ordering Information

Device	Package	Shipping
BTD1768S3-X-T1-G	SOT-323 (Pb-free and halogen-free package)	3000 pcs / Tape & Reel





Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V _{CB0}	180	V
Collector-Emitter Voltage	V _{CEO}	80	V
Emitter-Base Voltage	V _{EBO}	7	V
Collector Current (DC)	I _C	1	A
Collector Current (Pulse)	I _{CP}	2 (Note)	A
Power Dissipation	P _D	200	mW
Thermal Resistance, Junction to Ambient	R _{θJA}	625	°C/W
Operating Junction Temperature Range	T _j	-55~+150	°C
Storage Temperature	T _{stg}	-55~+150	°C

Note : Pulse test, P_w ≤ 10ms, Duty ≤ 2%.

Characteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CB0}	180	-	-	V	I _C =50μA
BV _{CEO}	80	-	-	V	I _C =1mA
BV _{EBO}	7	-	-	V	I _E =50μA
I _{CBO}	-	-	100	nA	V _{CB} =180V, I _E =0
I _{EBO}	-	-	100	nA	V _{EB} =7V, I _C =0
*V _{CE(SAT)} 1	-	0.15	0.3	V	I _C =500mA, I _B =20mA
*V _{CE(SAT)} 2	-	0.3	0.5	V	I _C =1A, I _B =50mA
*V _{BE(SAT)}	-	0.96	1.2	V	I _C =1A, I _B =50mA
*V _{BE(ON)}	0.5	0.66	0.9	V	V _{CE} =2V, I _C =50mA
*h _{FE} 1	180	-	560	-	V _{CE} =2V, I _C =100mA
*h _{FE} 2	60	-	-	-	V _{CE} =2V, I _C =500mA
*h _{FE} 3	20	-	-	-	V _{CE} =2V, I _C =1A
f _T	-	250	-	MHz	V _{CE} =10V, I _C =50mA, f=100MHz
C _{ob}	-	6	15	pF	V _{CB} =10V, I _E =0A, f=1MHz

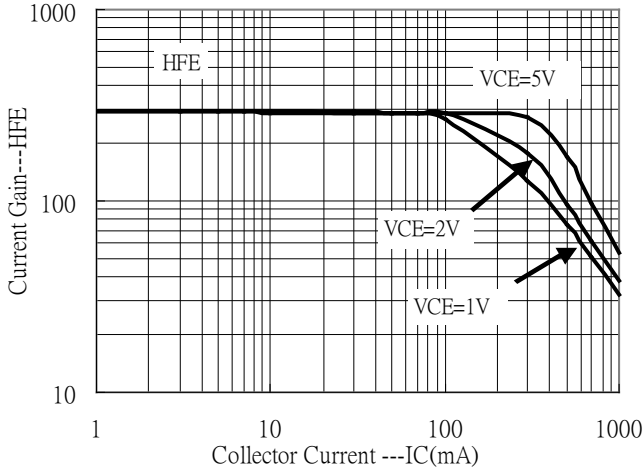
*Pulse Test: Pulse Width ≤ 380μs, Duty Cycle ≤ 2%

Classification Of h_{FE} 1

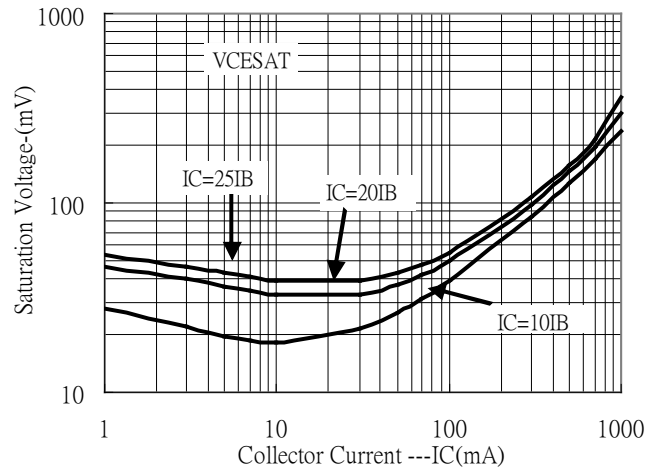
Rank	R	S
Range	180~390	270~560

Typical Characteristics

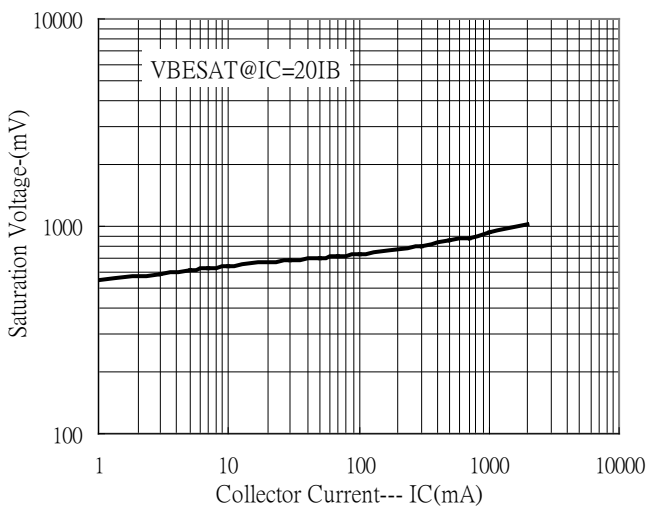
Current Gain vs Collector Current



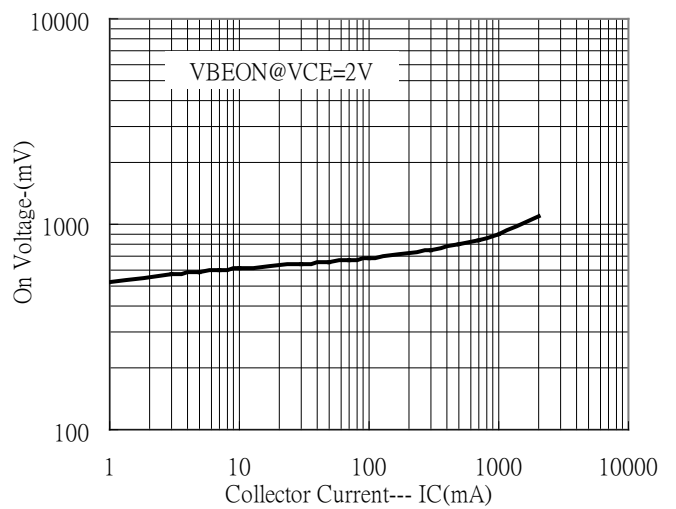
Saturation Voltage vs Collector Current



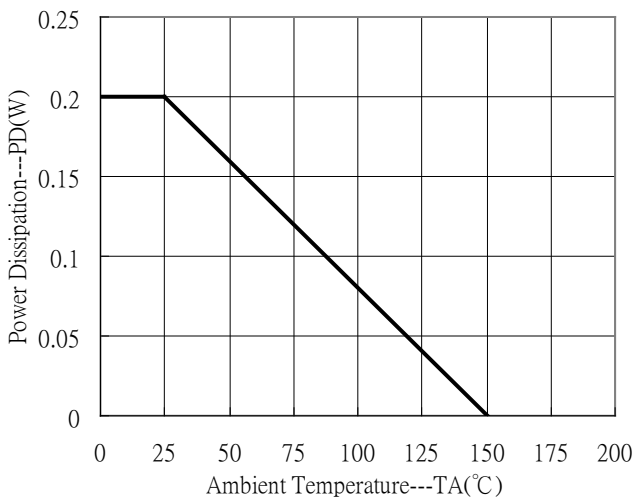
Saturation Voltage vs Collector Current



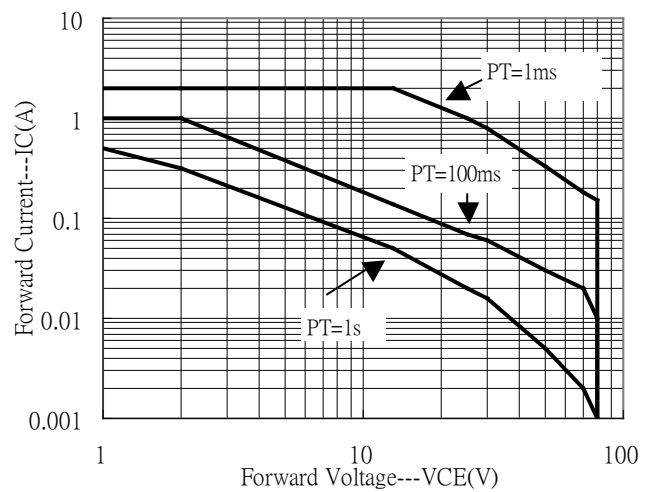
On Voltage vs Collector Current



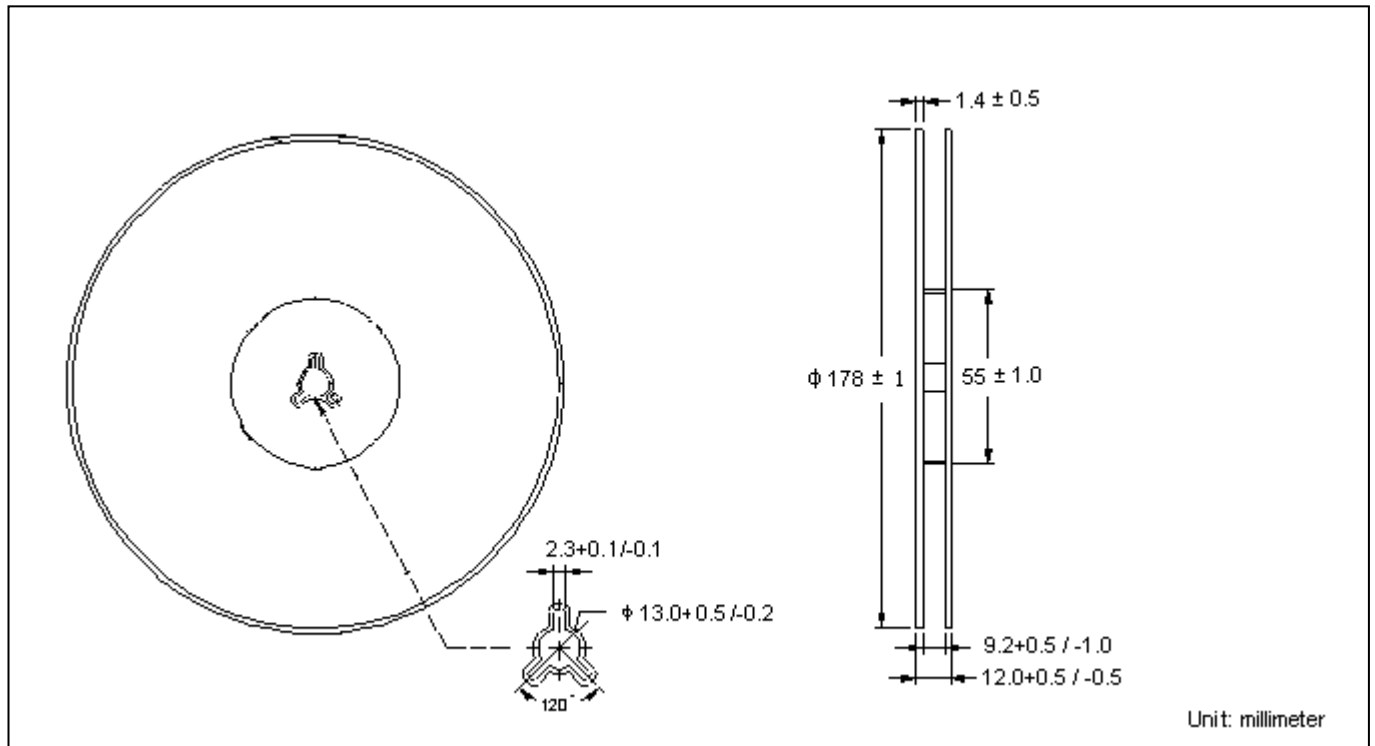
Power Derating Curve



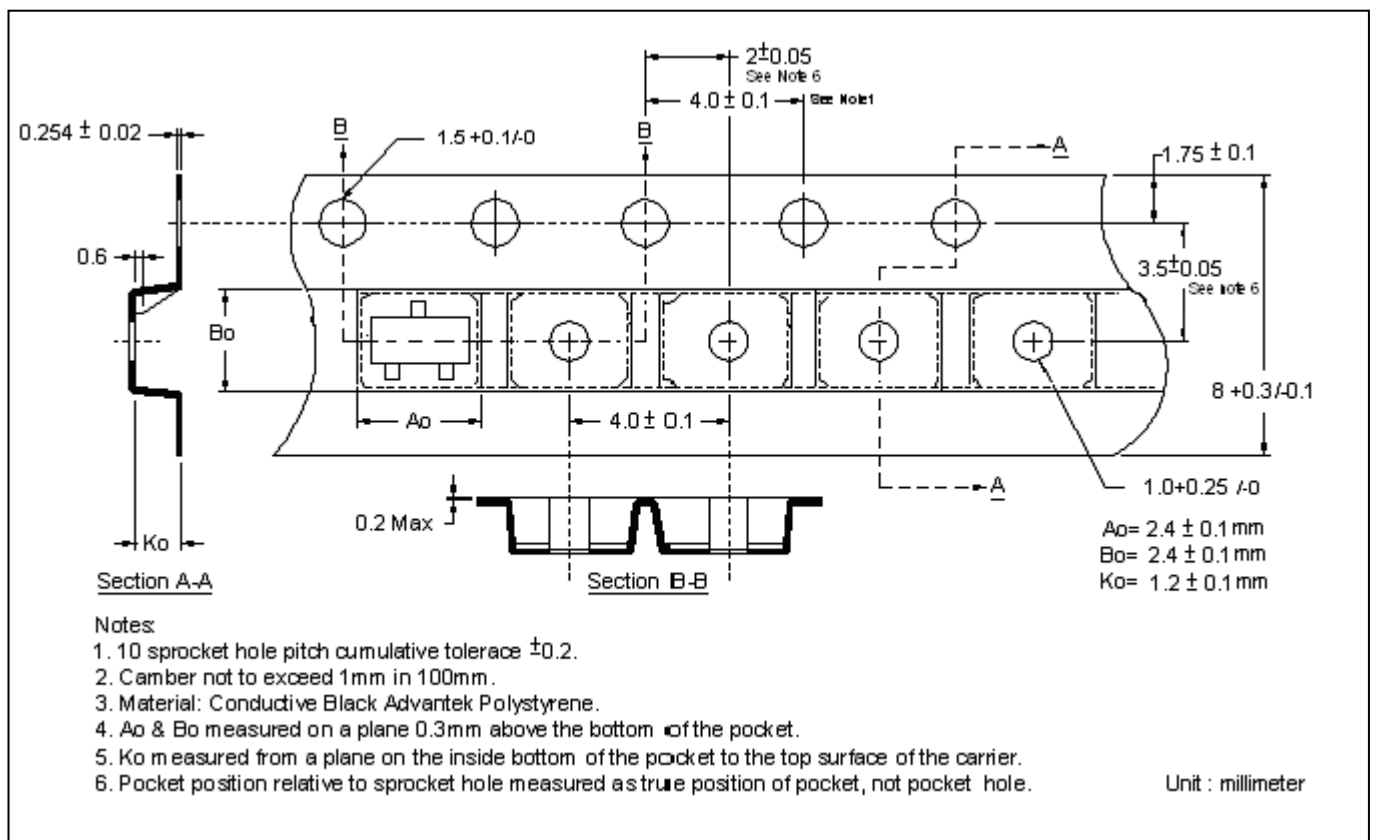
Safe Operating Area



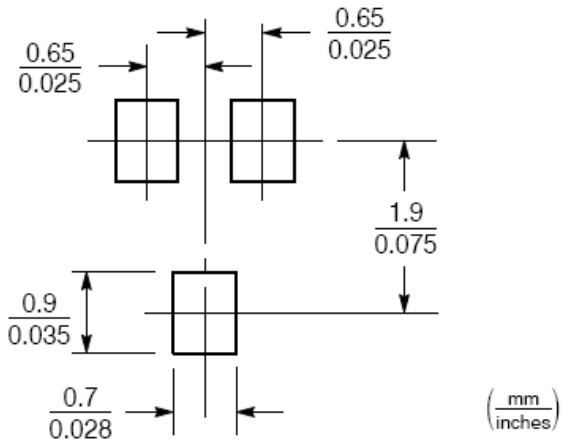
Reel Dimension



Carrier Tape Dimension



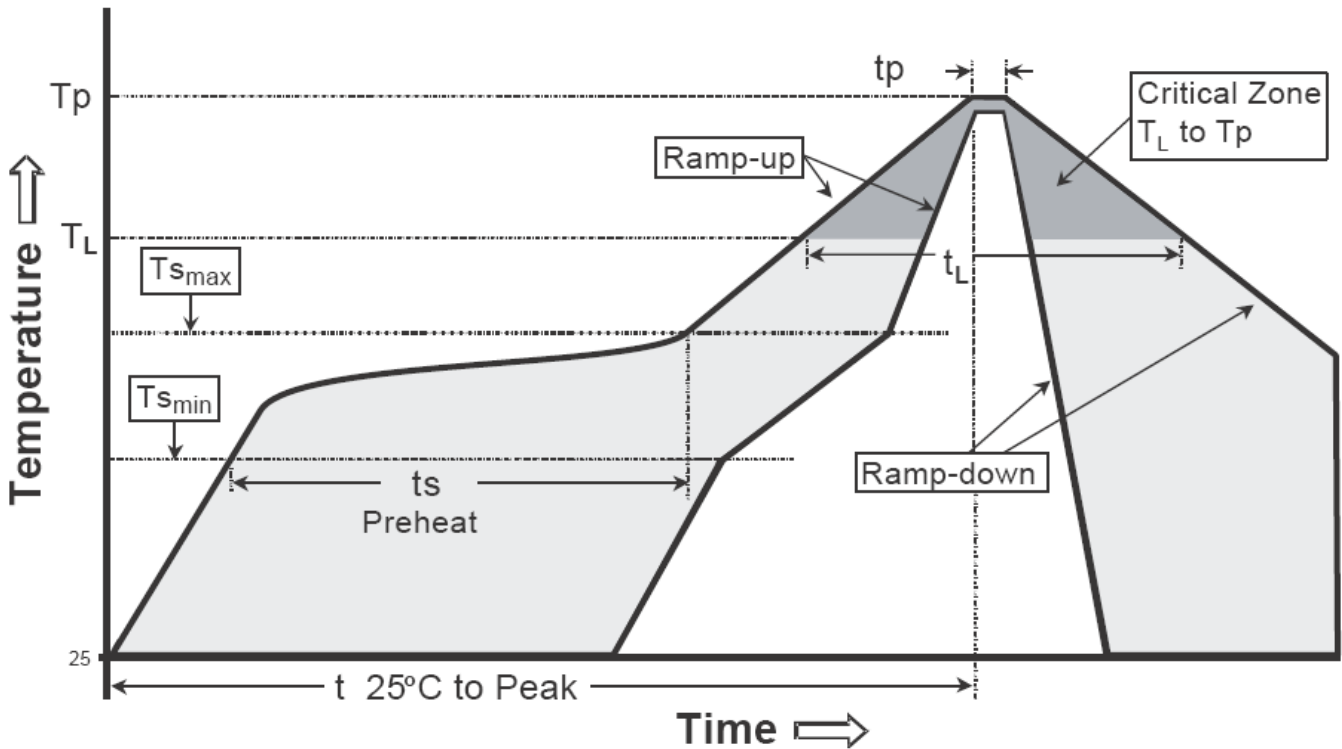
Recommended Soldering Footprint



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

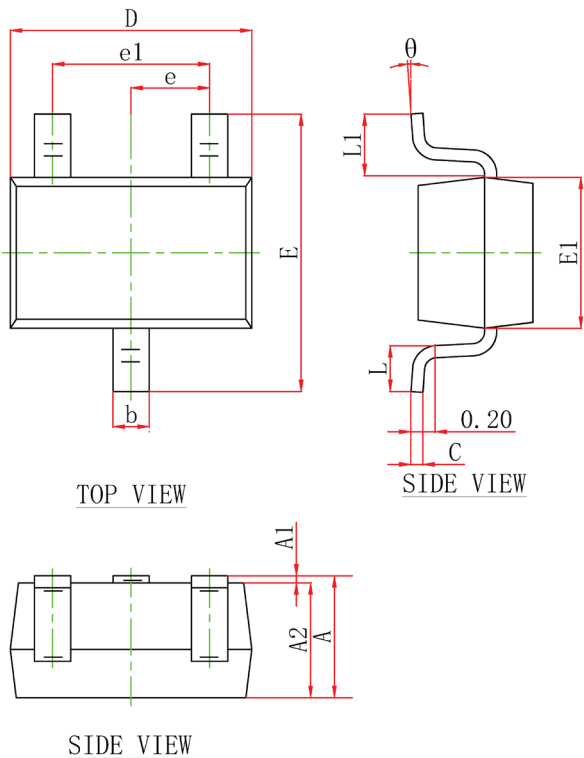
Recommended temperature profile for IR reflow



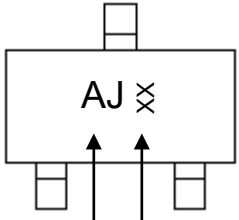
Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note :1. All temperatures refer to topside of the package, measured on the package body surface.
 2.For devices mounted on FR-4 PCB of 1.6mm or equivalent grade PCB. If other grade PCB is used, care should be taken to match the coefficients of thermal expansion between components and PCB. If they are not matched well, the solder joints may crack or the bodies of the parts may crack or shatter as the assembly cools.

SOT-323 Dimension



Marking:



Device Code Date Code

Style: Pin 1.Base 2.Emitter 3.Collector

Date Code: Year+Month
 Year: 3→2003, 4→2004
 Month: 1→1, 2→2, . . .
 9→9, A→10, B→11, C→12

3-Lead SOT-323 Plastic
 Surface Mounted Package
 CYS Package Code: S3

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.90	1.10	0.035	0.043	E1	1.15	1.35	0.045	0.053
A1	0.00	0.10	0.000	0.004	e	0.65 TYP		0.026	TYP
A2	0.90	1.00	0.035	0.039	e1	1.20	1.40	0.047	0.055
b	0.20	0.40	0.008	0.016	L	0.26	0.46	0.010	0.018
c	0.08	0.15	0.003	0.006	L1	0.525 REF		0.021	REF
D	2.00	2.20	0.079	0.087	θ	0°	8°	0°	8°
E	2.15	2.45	0.085	0.096					

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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