

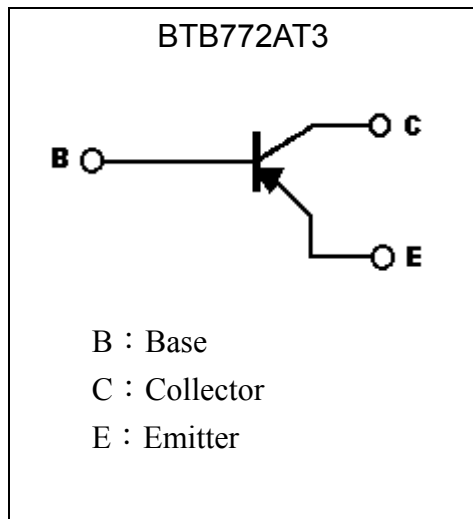
Low Vcesat PNP Epitaxial Planar Transistor

BTB772AT3

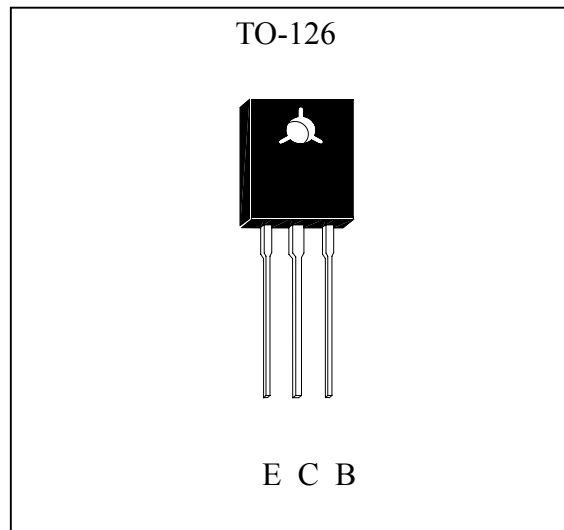
Features

- Low $V_{CE(sat)}$, $V_{CE(sat)} = -0.3\text{ V (max)}$, at $I_C / I_B = -2\text{A} / -0.1\text{A}$
- Excellent current gain characteristics
- Pb-free lead plating package

Symbol

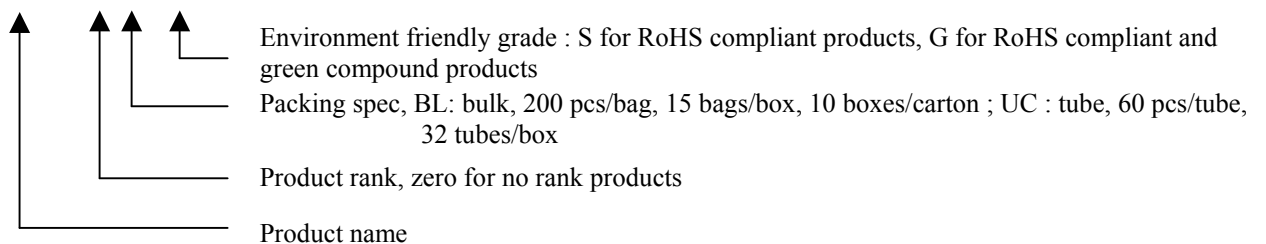


Outline



Ordering Information

Device	Package	Shipping
BTB772AT3-0-BL-X	TO-126 (Pb-free lead plating and halogen-free package)	200 pcs / bag, 3,000 pcs/box 30,000 pcs/carton
BTB772AT3-0-UC-X		60 pcs/ tube, 32 tubes/box



**Absolute Maximum Ratings** (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V _{CB0}	-50	V
Collector-Emitter Voltage	V _{CEO}	-30	V
Emitter-Base Voltage	V _{EBO}	-7	V
Collector Current (DC)	I _C	-3	A
Collector Current (Pulse)	I _{CP}	-5 (Note 1)	A
Power Dissipation @T _A =25°C	P _D	1	W
Power Dissipation @T _C =25°C		10	W
Operating Junction and Storage Temperature Range	T _j ; T _{stg}	-55~+150	°C

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	R _{θJC}	12.5	°C/W
Thermal Resistance, Junction-to-ambient, max	R _{θJA}	125	°C/W

Note : 1. Single Pulse , P_w=10ms**Characteristics** (Ta=25°C)

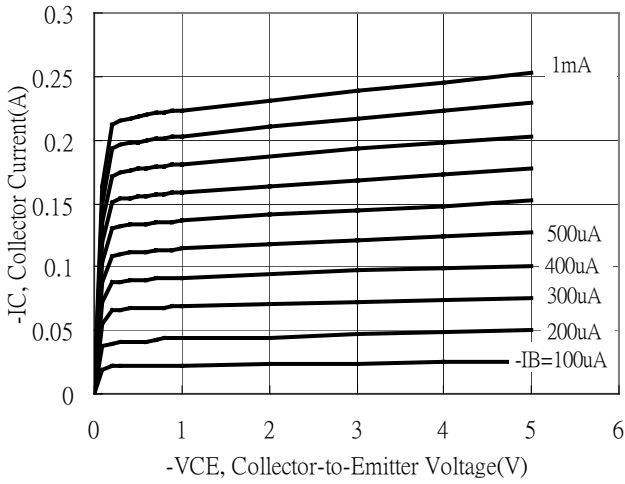
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CB0}	-50	-	-	V	I _C =-50μA, I _E =0
BV _{CEO}	-30	-	-	V	I _C =-1mA, I _B =0
BV _{EBO}	-7	-	-	V	I _E =-50μA, I _C =0
I _{CB0}	-	-	-100	nA	V _{CB} =-50V, I _E =0
I _{EBO}	-	-	-100	nA	V _{EB} =-7V, I _C =0
*V _{CE(sat)}	-	-0.05	-0.2	V	I _C =-400mA, I _B =-20mA
*V _{CE(sat)}	-	-0.2	-0.3	V	I _C =-2A, I _B =-100mA
*V _{BE(sat)}	-	-1	-1.2	V	I _C =-2A, I _B =-200mA
*h _{FE 1}	160	-	-	-	V _{CE} =-2V, I _C =-100mA
*h _{FE 2}	180	-	390	-	V _{CE} =-2V, I _C =-500mA
*h _{FE 3}	150	-	-	-	V _{CE} =-2V, I _C =-1A
f _T	-	190	-	MHz	V _{CE} =-10V, I _C =-0.5A, f=100MHz
C _{ob}	-	33	-	pF	V _{CB} =-10V, f=1MHz

*Pulse Test : Pulse Width ≤380μs, Duty Cycle ≤2%

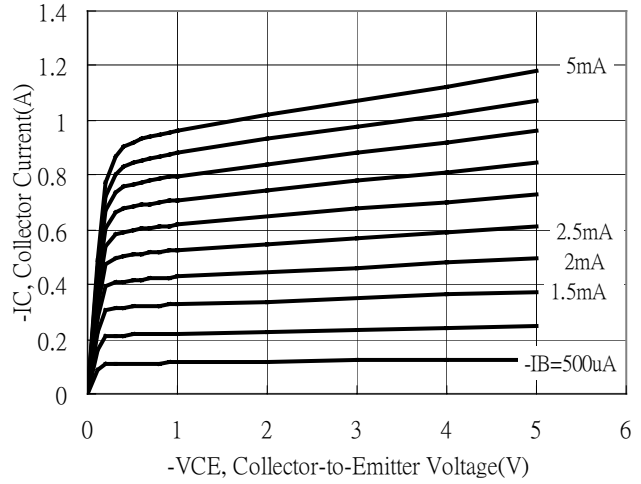


Typical Characteristics

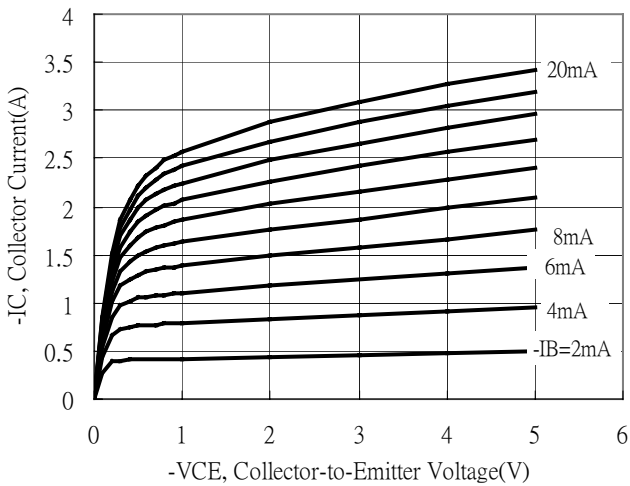
Emitter Grounded Output Characteristics



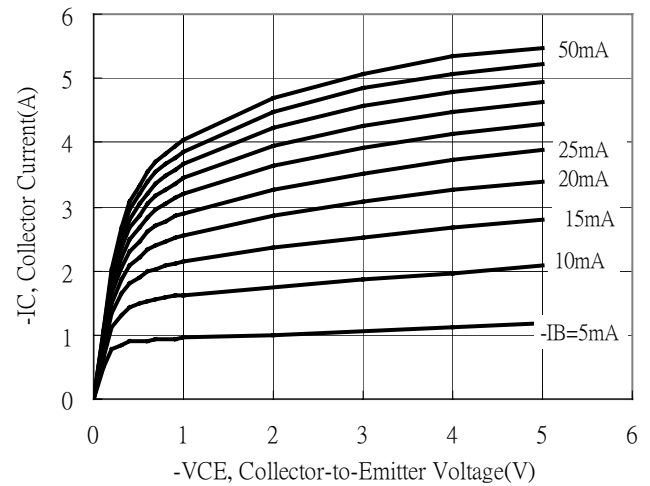
Emitter Grounded Output Characteristics



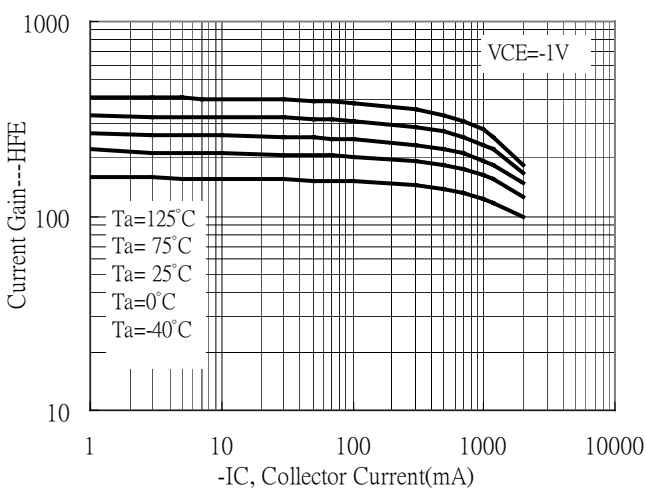
Emitter Grounded Output Characteristics



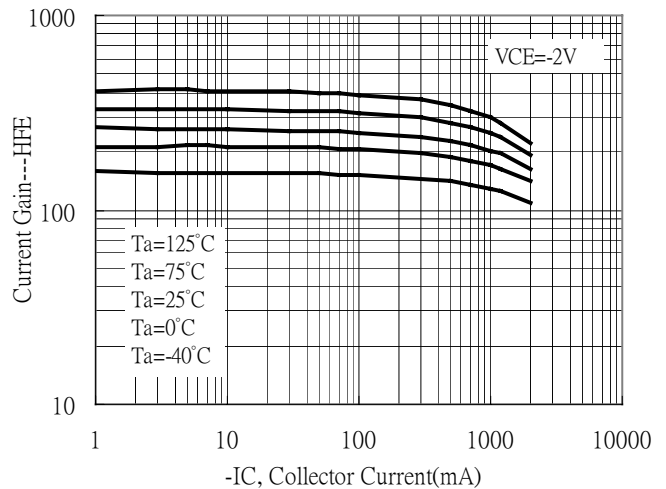
Emitter Grounded Output Characteristics



Current Gain vs Collector Current



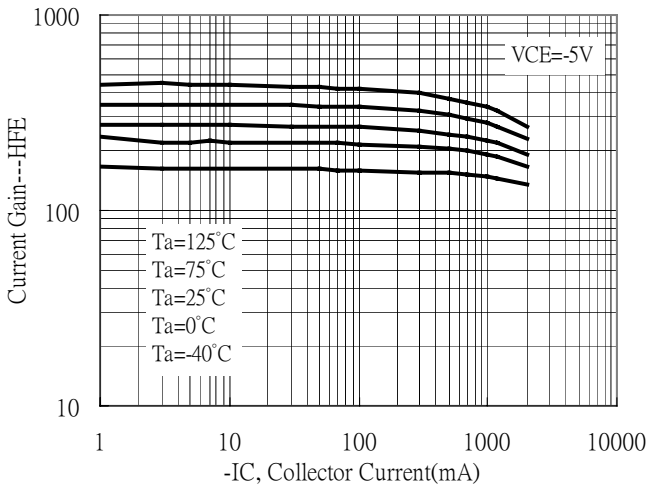
Current Gain vs Collector Current



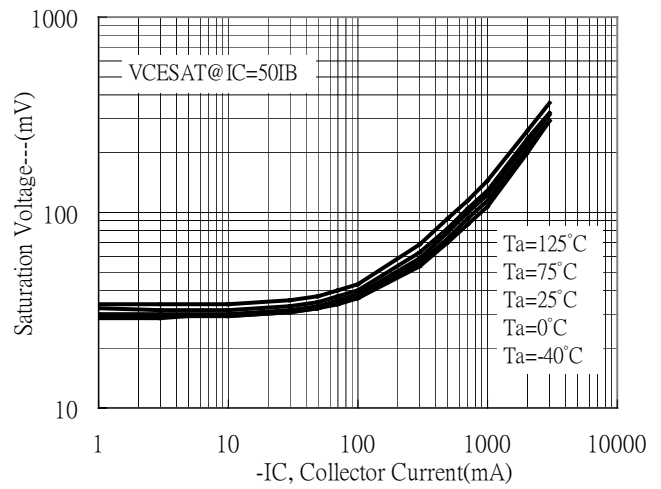


Typical Characteristics(Cont.)

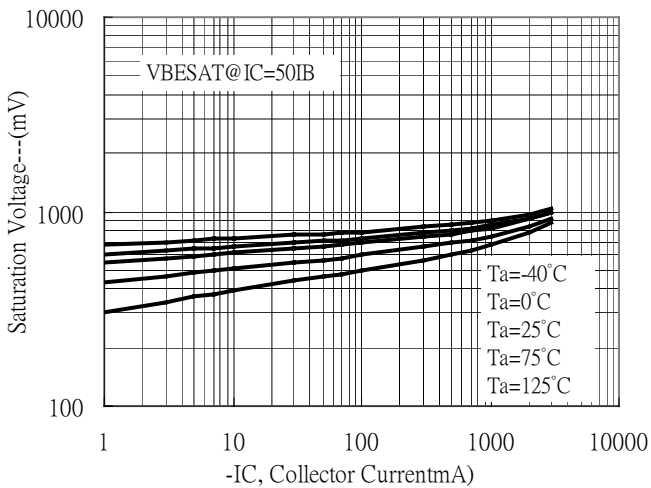
Current Gain vs Collector Current



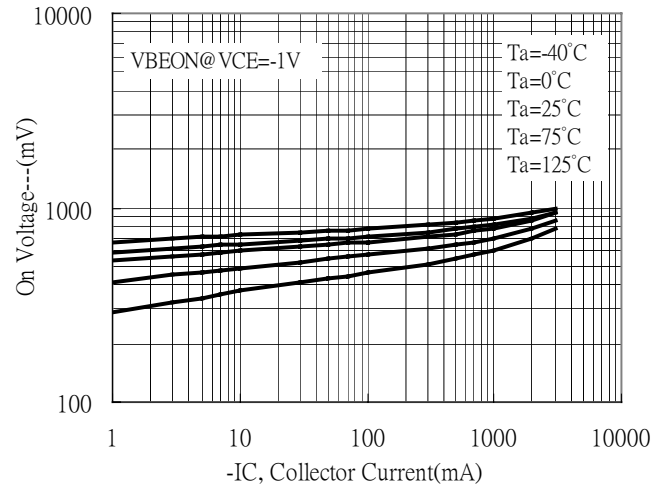
Saturation Voltage vs Collector Current



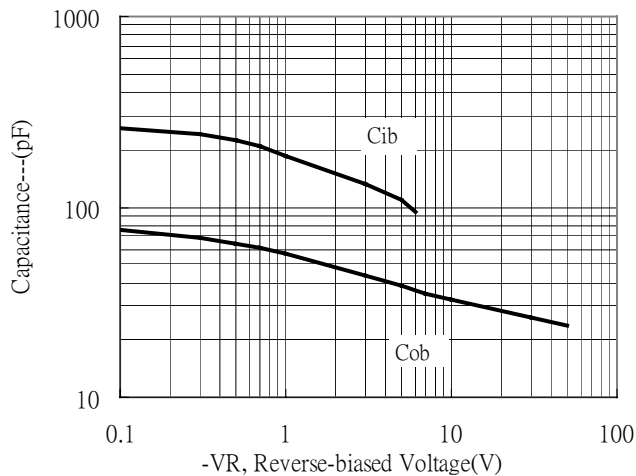
Saturation Voltage vs Collector Current



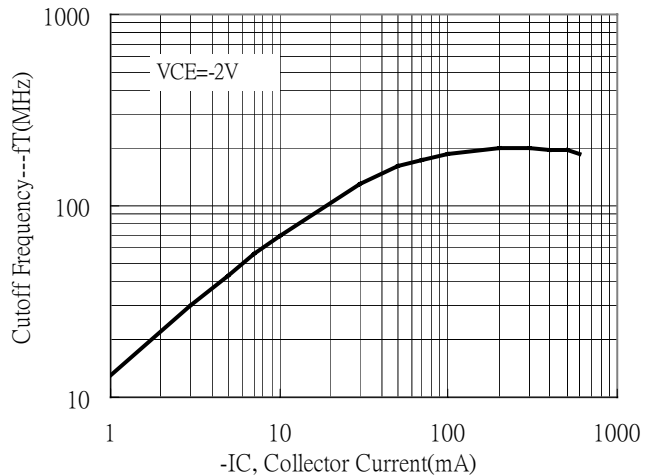
On Voltage vs Collector Current



Capacitance vs Reverse-biased Voltage



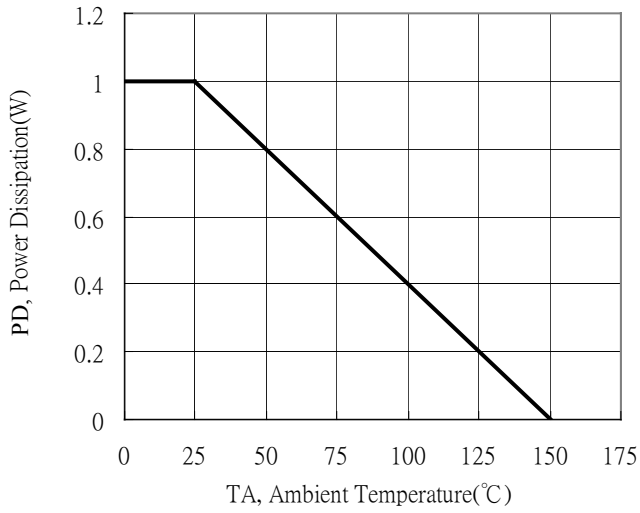
Cutoff Frequency vs Collector Current



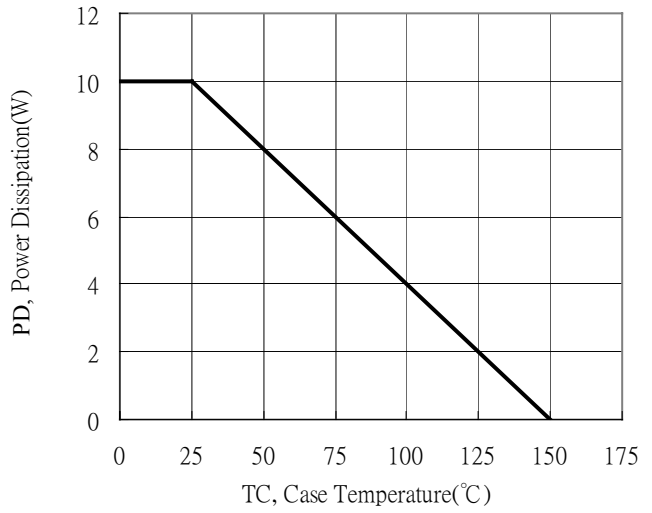


Typical Characteristics(Cont.)

Power Derating Curve



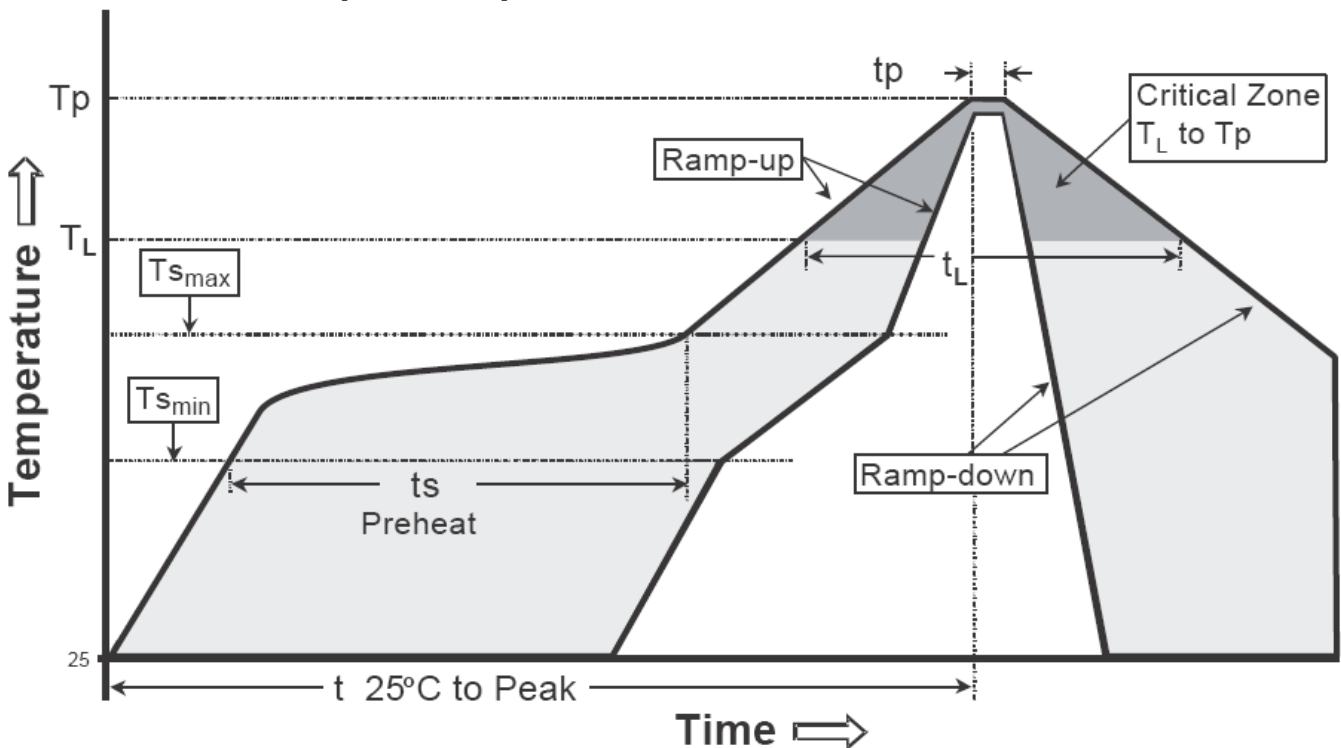
Power Derating Curve



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

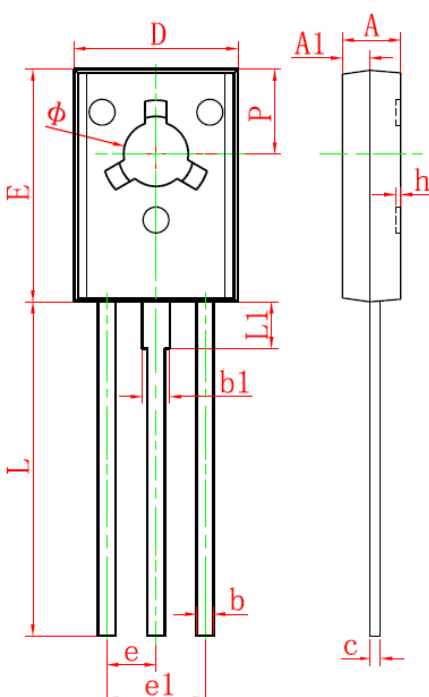
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

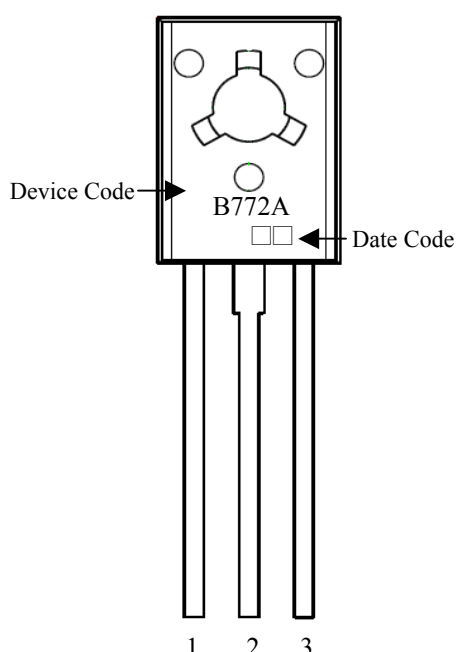
Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-126 Dimension



The diagram shows two views of a TO-126 package. The left view is a top-down perspective showing dimensions: D (width), E (height), P (pitch), L (total length), L1 (lead length), b (lead width), b1 (lead thickness), e (lead spacing), and e1 (lead width at base). The right view is a side profile showing dimensions: A (height), A1 (height to top of leads), h (lead thickness), and c (lead thickness at base).

Marking:



The marking diagram shows the top of the package with a circular window containing the device code 'B772A' and a date code window. The pins are numbered 1, 2, and 3 from left to right.

Style: Pin 1. Emitter 2. Collector 3. Base

3-Lead TO-126 Plastic Package
 CYStek Package Code: T3

Date Code : Year Code + Month Code
 Year Code : 2011→1, 2012→2, ..., 2020→0,
 2021→1, 2022→2, ..., etc
 Month Code : Jan →1, Feb → 2, ..., Sep→9,
 Oct→A, Nov→B, Dec→C

*: Typical

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	2.500	2.900	0.098	0.114	e	*2.290		*0.090	
A1	1.100	1.500	0.043	0.059	e1	4.480	4.680	0.176	0.184
b	0.660	0.860	0.026	0.034	h	0.000	0.300	0.000	0.012
b1	1.170	1.370	0.046	0.054	L	15.300	15.700	0.602	0.618
c	0.450	0.600	0.018	0.024	L1	2.100	2.300	0.083	0.091
D	7.400	7.800	0.291	0.307	P	3.900	4.100	0.154	0.161
E	10.600	11.000	0.417	0.433	Φ	3.000	3.200	0.118	0.126

Notes: 1. Controlling dimension: millimeters.
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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