

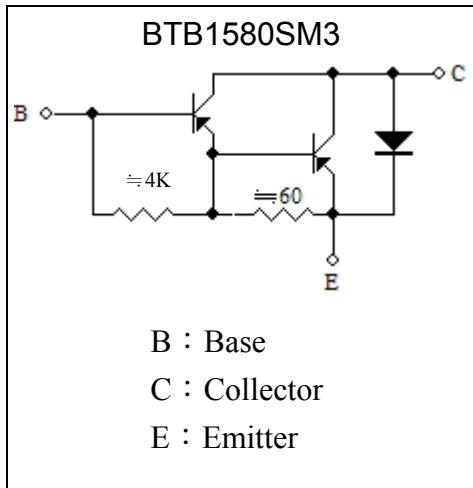
# PNP Epitaxial Planar Transistor

## BTB1580SM3

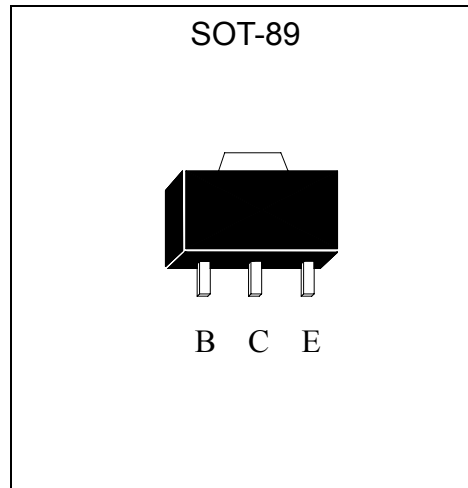
### Description

The BTB1580SM3 is a PNP Darlington transistor, designed for use in general purpose amplifier and low speed switching application. Pb-free package process is adopted.

### Equivalent Circuit

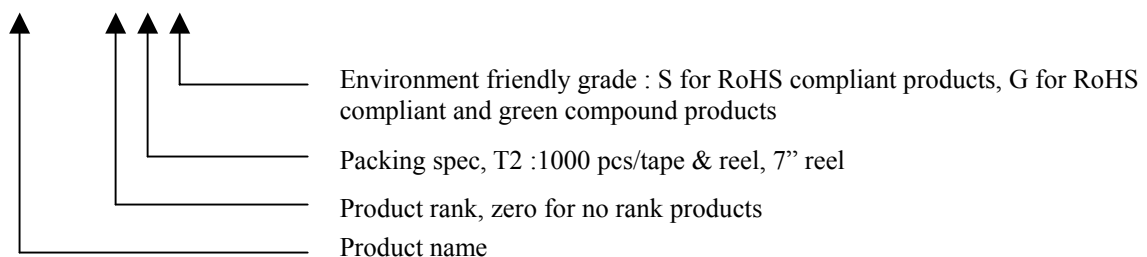


### Outline



### Ordering Information

Device	Package	Shipping
BTB1580SM3-0-T2-G	SOT-89 (Pb-free lead plating and halogen-free package)	1000 pcs / Tape & Reel





**Absolute Maximum Ratings (Ta=25°C)**

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V <sub>CB0</sub>	-120	V
Collector-Emitter Voltage	V <sub>CEO</sub>	-120	
Emitter-Base Voltage	V <sub>EBO</sub>	-5	
Collector Current (DC)	I <sub>C</sub>	-4	A
Collector Current (Pulse)	I <sub>CP</sub>	-6 (Note 1)	
Thermal Resistance, Junction to Ambient	R <sub>θJA</sub>	208	°C/W
		125 (Note 2)	
		62.5 (Note 3)	
		85 (Note 4)	
Thermal Resistance, Junction to Case	R <sub>θJC</sub>	43	
Power Dissipation	P <sub>D</sub>	0.7	W
		1.2 (Note 2)	
		2.4 (Note 3)	
		1.8 (Note 4)	
Power Dissipation @ T <sub>C</sub> =25°C		3.5	
Operating Junction Temperature Range	T <sub>J</sub>	-55~+175	°C
Storage Temperature Range	T <sub>stg</sub>	-55~+175	

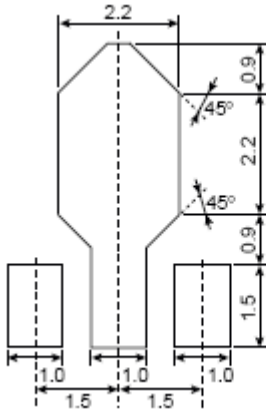
- Note : 1. Single Pulse P<sub>w</sub> ≤ 350μs, Duty ≤ 2%.  
 2. When mounted on a FR-4 PCB with area measuring 10×10×1 mm.  
 3. When mounted on a ceramic board with area measuring 40×40×1mm.  
 4. When mounted on a FR-4 PCB with area measuring 30×30×1 mm.

**Characteristics (Ta=25°C)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV <sub>CEO</sub>	-120	-	-	V	I <sub>C</sub> =-1mA, I <sub>B</sub> =0
BV <sub>CB0</sub>	-120	-	-	V	I <sub>C</sub> =-100μA, I <sub>E</sub> =0
I <sub>CB0</sub>	-	-	-100	nA	V <sub>CB</sub> =-120V, I <sub>E</sub> =0
I <sub>CEO</sub>	-	-	-1	μA	V <sub>CE</sub> =-120V, I <sub>B</sub> =0
I <sub>EBO</sub>	-	-	-2	mA	V <sub>EB</sub> =-5V, I <sub>C</sub> =0
*V <sub>CE(sat)</sub>	-	-	-1.8	V	I <sub>C</sub> =-2A, I <sub>B</sub> =-2mA
*V <sub>BE(on)</sub>			-2.2	V	V <sub>CE</sub> =-4V, I <sub>C</sub> =-2A
*h <sub>FE1</sub>	1000	-	-	-	V <sub>CE</sub> =-4V, I <sub>C</sub> =-1A
*h <sub>FE2</sub>	1000	-	-	-	V <sub>CE</sub> =-4V, I <sub>C</sub> =-2A
C <sub>ob</sub>	-		200	pF	V <sub>CB</sub> =-10V, I <sub>E</sub> =0A, f=1MHz

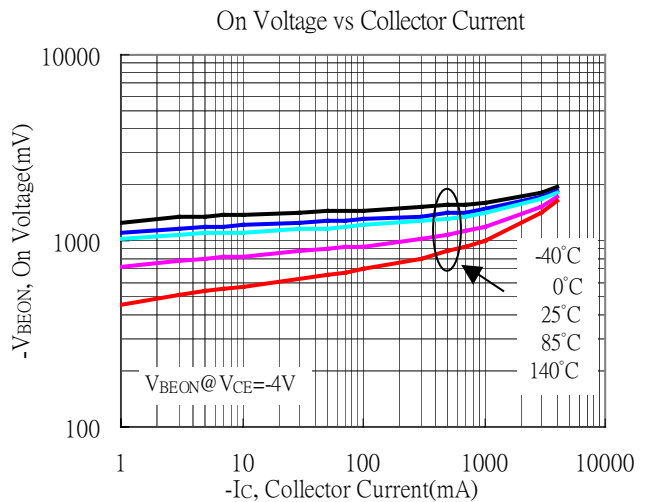
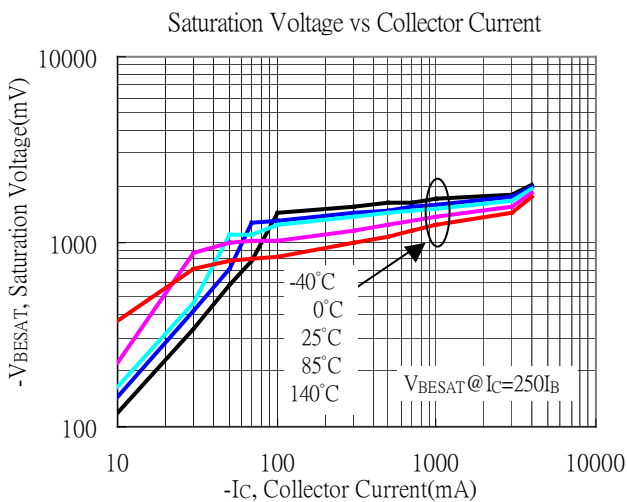
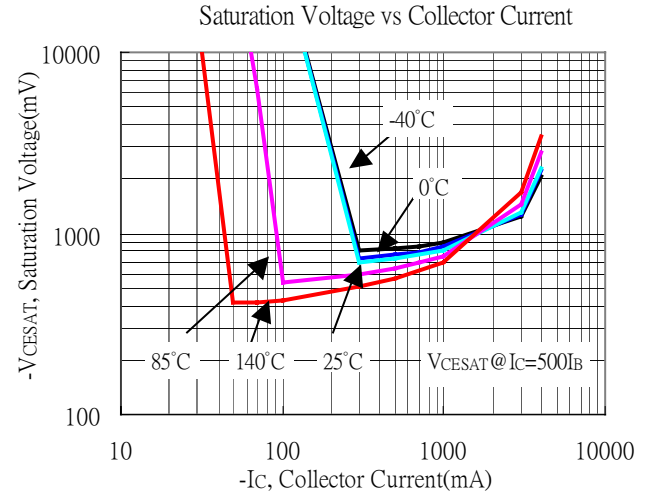
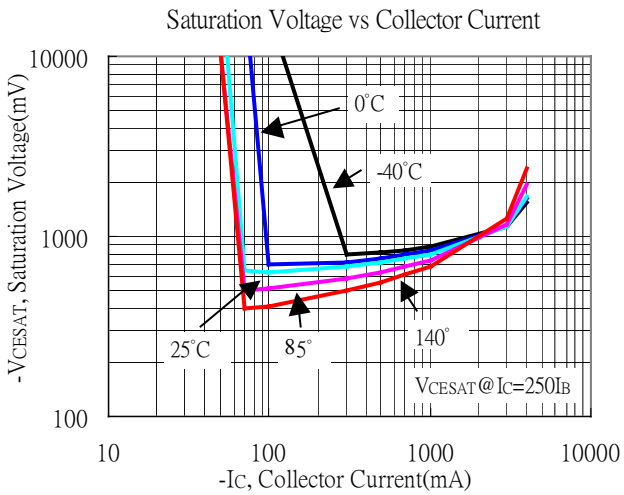
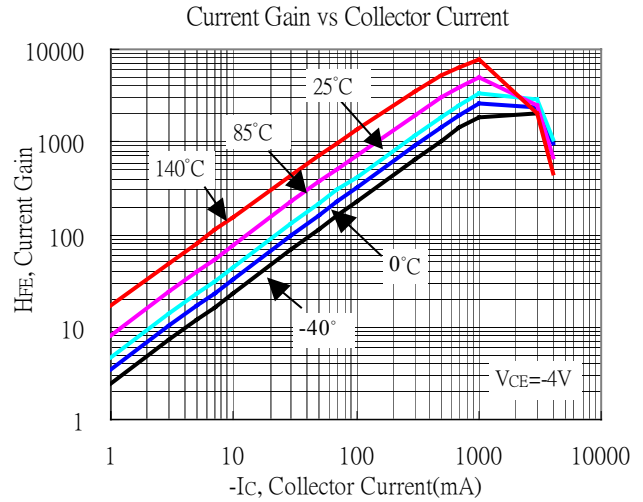
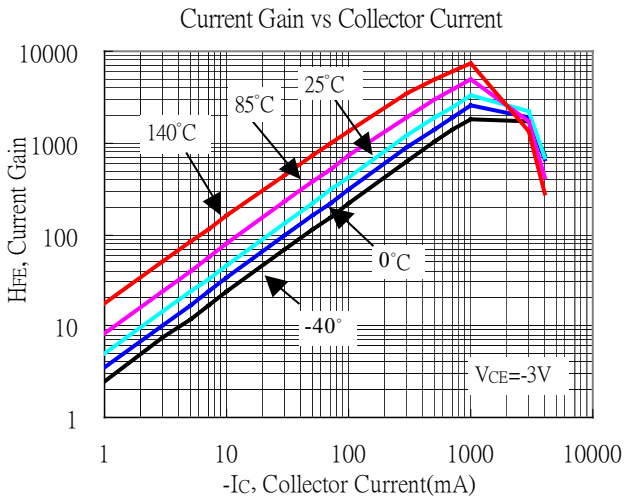
\*Pulse Test : Pulse Width ≤ 380μs, Duty Cycle ≤ 2%

### Recommended soldering footprint



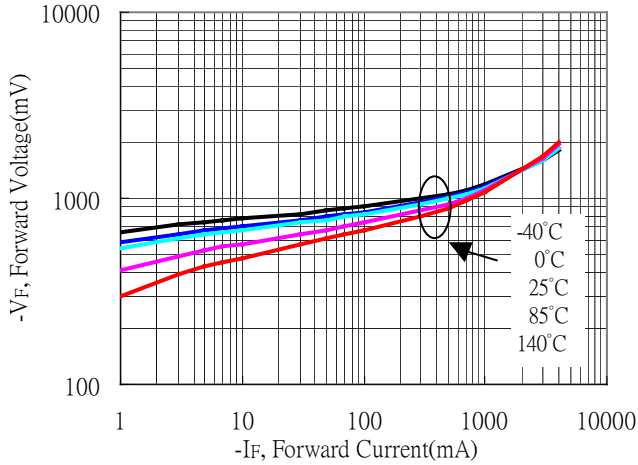
unit : mm

**Typical Characteristics**

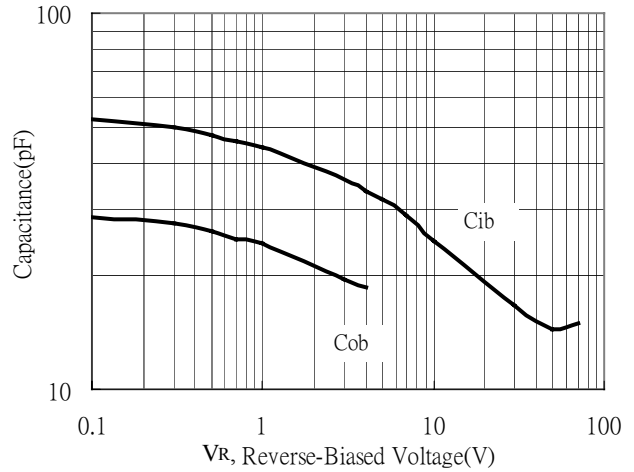


## Typical Characteristics(Cont.)

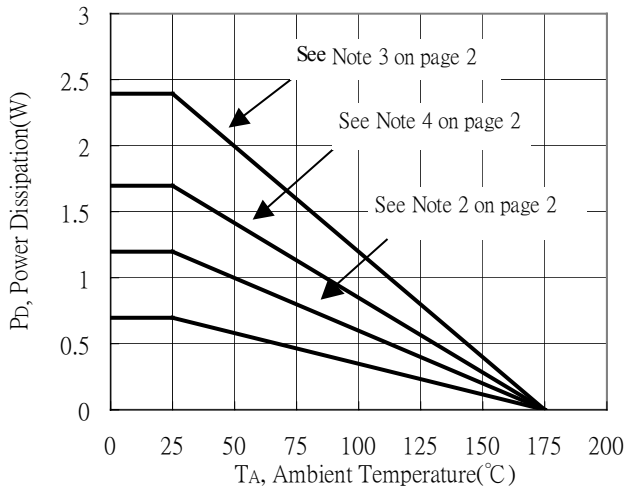
Built-in Diode Characteristics



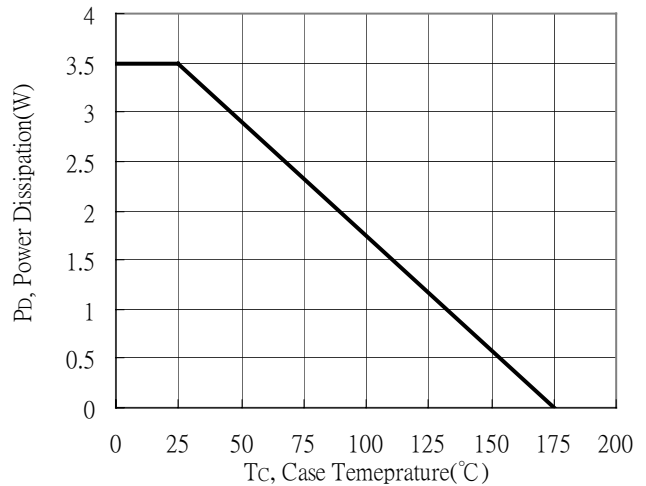
Capacitance vs Reverse-Biased Voltage



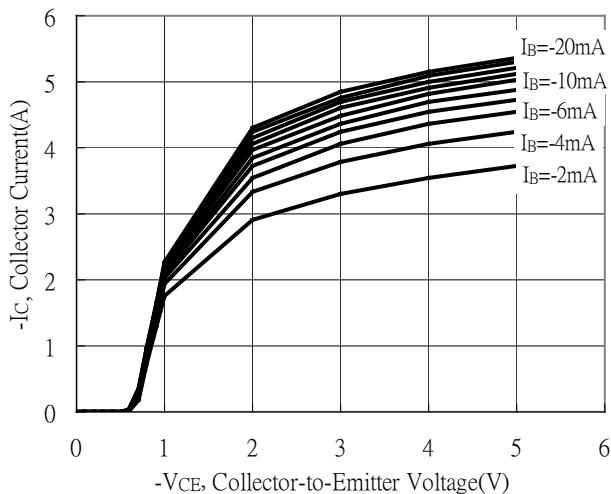
Power Derating Curves



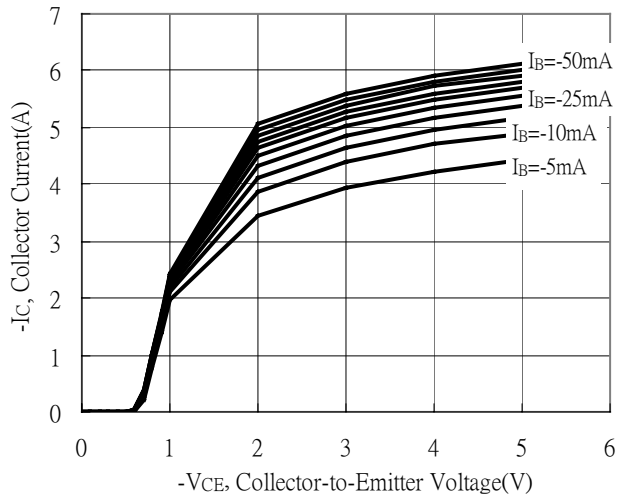
Power Derating Curve



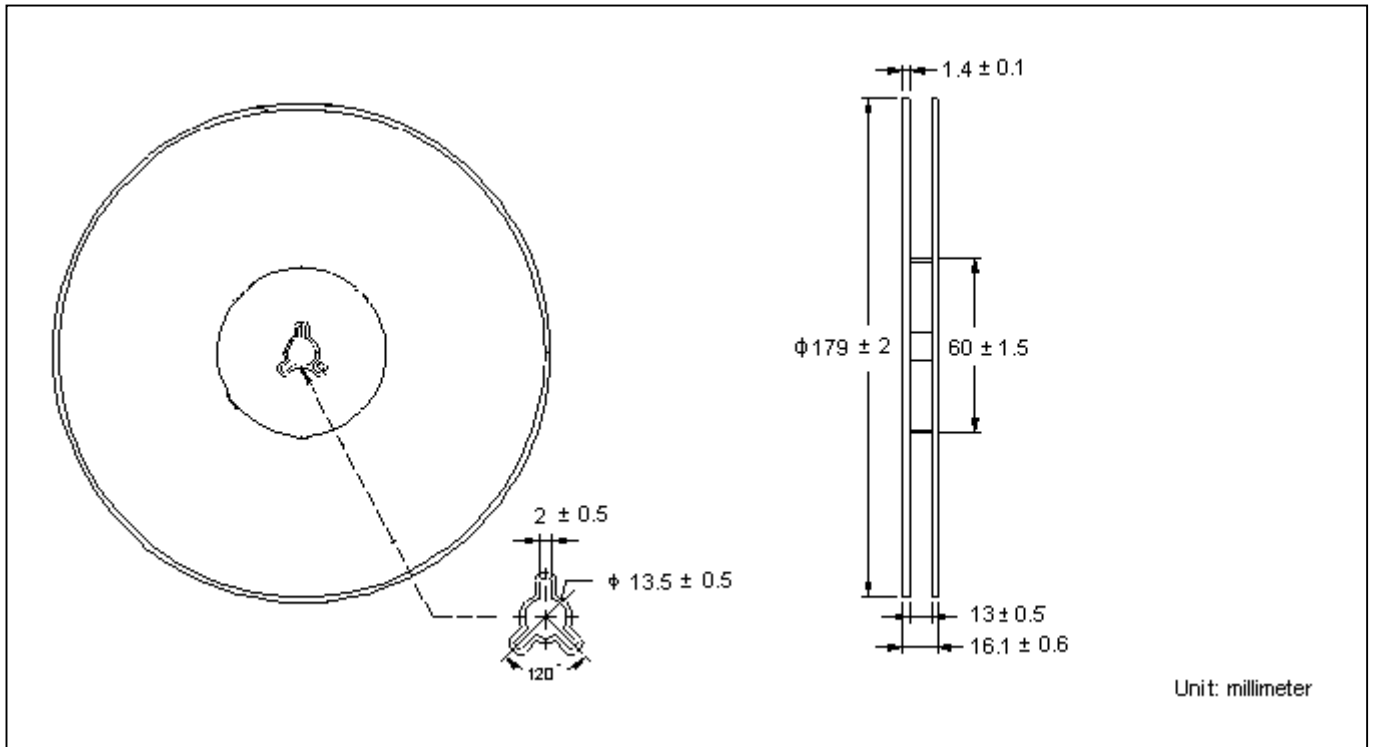
Emitter Grounded Output Characteristics



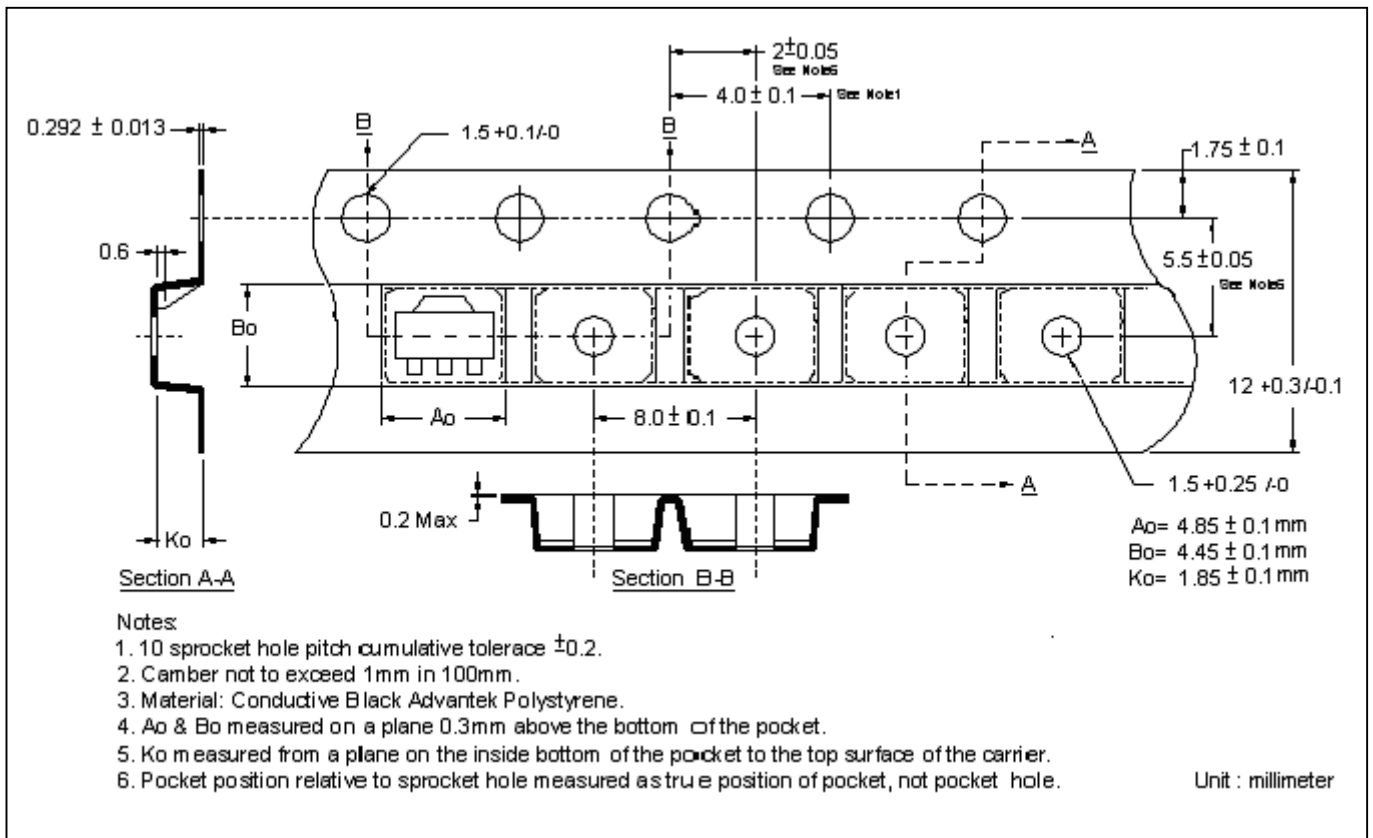
Emitter Grounded Output Characteristics



**Reel Dimension**



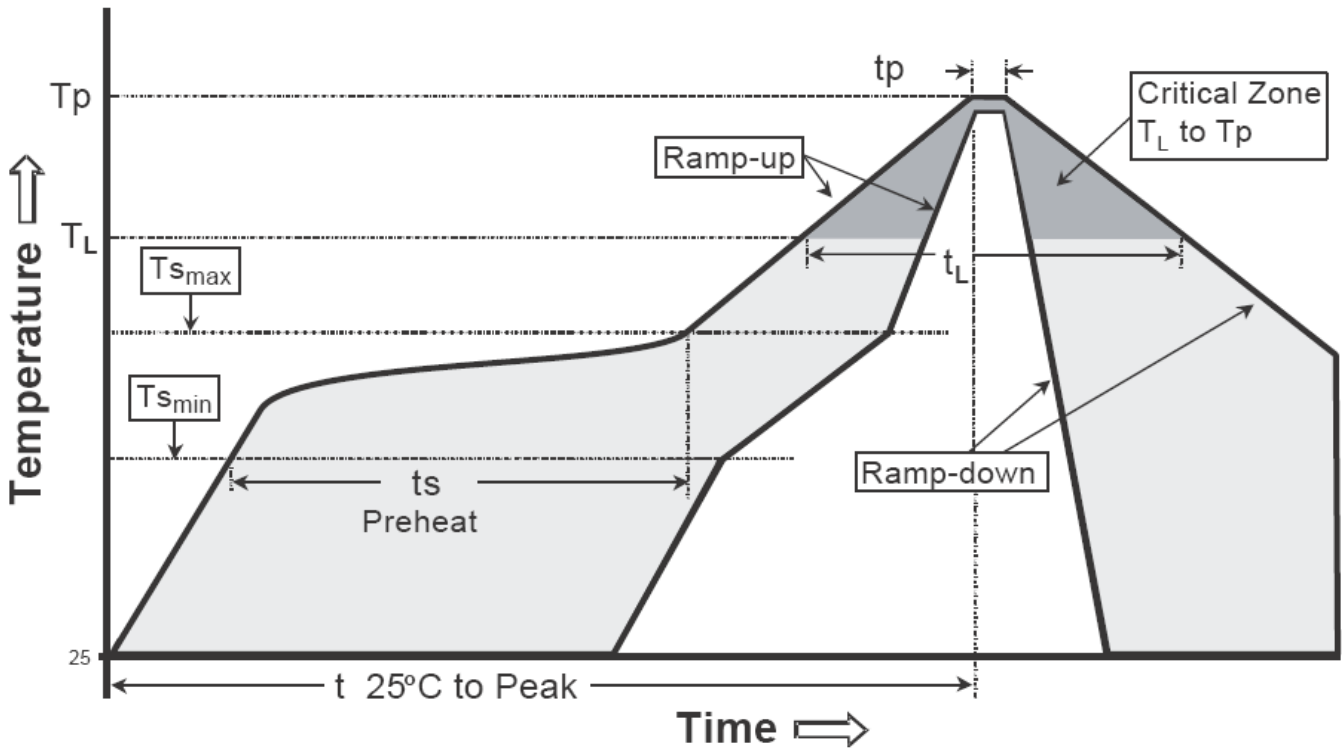
**Carrier Tape Dimension**



**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

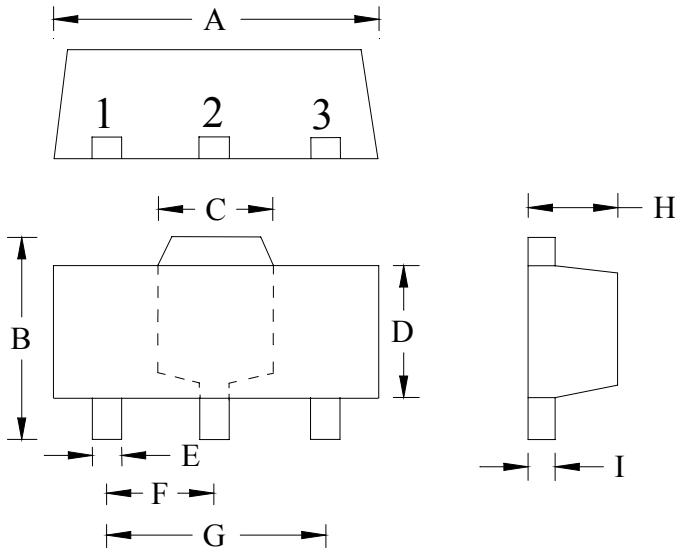
**Recommended temperature profile for IR reflow**



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T <sub>s min</sub> )	100°C	150°C
-Temperature Max(T <sub>s max</sub> )	150°C	200°C
-Time(t <sub>s min</sub> to t <sub>s max</sub> )	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T <sub>L</sub> )	183°C	217°C
- Time (t <sub>L</sub> )	60-150 seconds	60-150 seconds
Peak Temperature(T <sub>P</sub> )	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

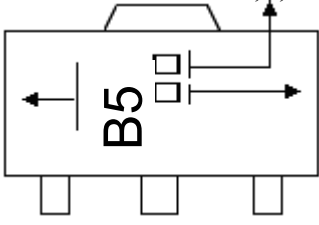
Note :1. All temperatures refer to topside of the package, measured on the package body surface.  
 2. For devices mounted on FR-4 PCB of 1.6mm or equivalent grade PCB. If other grade PCB is used, care should be taken to match the coefficients of thermal expansion between components and PCB. If they are not matched well, the solder joints may crack or the bodies of the parts may crack or shatter as the assembly cools.

**SOT-89 Dimension**



The diagram shows three views of the SOT-89 package: a top view with dimensions A, C, and lead positions 1, 2, 3; a front view with dimensions B, D, E, F, G; and a side view with dimensions H and I.

**Marking:**



month code: 1~9, A,B,C  
 Year code : 6→2006, 7→2007,...

Product Code ← B5 →

Style: Pin 1. Base 2. Collector 3. Emitter

3-Lead SOT-89 Plastic  
 Surface Mounted Package  
 CYStek Package Code: M3

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1732	0.1811	4.40	4.60	F	0.0591	TYP	1.50	TYP
B	0.1551	0.1673	3.94	4.25	G	0.1181	TYP	3.00	TYP
C	0.0610	REF	1.55	REF	H	0.0551	0.0630	1.40	1.60
D	0.0906	0.1024	2.30	2.60	I	0.0138	0.0173	0.35	0.44
E	0.0126	0.0205	0.32	0.52					

- Notes:**
- Controlling dimension: millimeters.
  - Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
  - If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

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