Adjustable shunt regulator

TL432A3/N3/M3/K3

Description

TheTL432 is a three terminal adjustable shunt regulator with thermal stability guaranteed over temperature. The output voltage can be adjusted to any value from 1.24V(V_{REF}) to 18V with two external resistors. The TL432 has a typical dynamic output impedance of 0.2Ω. Active output circuitry provides a very sharp turn on characteristic, making the TL432 an excellent replacement for zener diodes. The TL432 shunt regulator is available with two voltage tolerances(0.5%, and 1%), and four package options(TO-92, SOT-23, SOT-89 and TO-92L). This allows the designer the opportunity to select the optimum combination of cost and performance for their application.

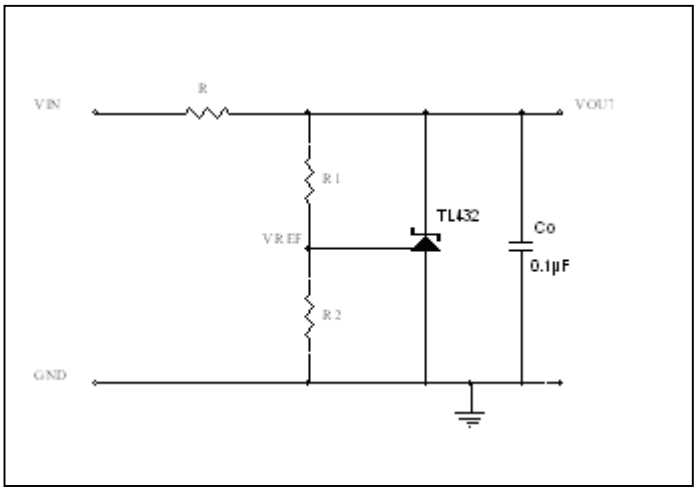
Features

- ◆Low voltage operation(down to 1.24V)
- ◆Fast turn on response
- ◆Low dynamic output impedance 0.2Ω typ.
- ◆Trimmed bandgap design : ±0.5%
- ◆Sink current capability : 100mA
- ◆Available in TO-92, SOT-23, SOT-89, and TO-92L packages

Applications

- ◆Linear Regulators
- ◆Adjustable Supplies
- ◆Switching Power Supplies
- ◆Battery Operated Computers
- ◆Instrumentation
- ◆Computer Disk Drives

Typical Application Circuit(Note 1,2)



Notes:

1) Set V_{OUT} according to the following equation:
$V_{OUT}=V_{REF}(1+R1/R2)+I_{REF}R1$

2) Choose the value for R as follows:
- The maximum limit for R should be such that the cathode current, Iz, is greater than the minimum operating current(80 μA) at $V_{IN(MIN)}$.
- The minimum limit for R should be as such that Iz does not exceed 100mA under all load conditions, and the instantaneous turn-on value for Iz does not exceed 150mA. Both of the following conditions must be met:

$R_{min}\geq V_{IN(max)}/150mA$(to limit instantaneous turn-on Iz)

$R_{min}\geq \frac{V_{IN(max)}-V_{OUT}}{I_{OUT(min)}+100mA}$ (to limit Iz under normal operating conditions)

Absolute Maximum Ratings

Parameter	Symbol	Maximum	Units
Cathode Voltage	V_Z	18	V
Continuous Cathode Current	I_Z	100	mA
Reference Input Current	I_{REF}	3	mA
Power Dissipation at T_A=25℃ SOT-23 SOT-89 TO-92 TO-92L	P_D	 0.225 0.5 0.625 0.9	W
Thermal Resistance SOT-23 SOT-89 TO-92 TO-92L	θ_{JA}	 556 250 200 139	℃/W
Operating Ambient Temperature Range	T_A	-40 to +85	℃
Operating Junction Temperature Range	T_J	-40 to +150	℃
Storage Temperature Range	Tstg	-65 to +150	℃

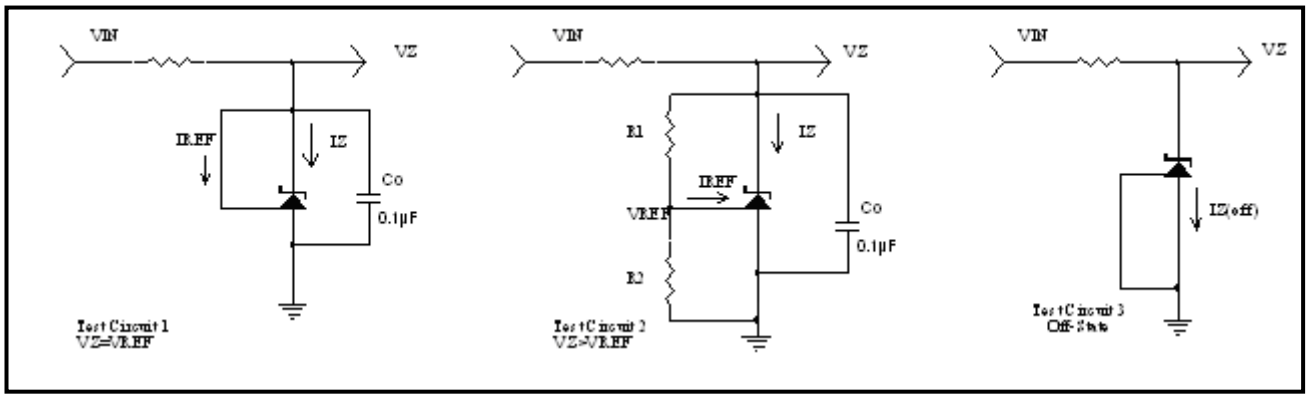
Electrical Characteristics

Unless otherwise specified, TA=25℃. Values in bold apply over full operating ambient temperature range.

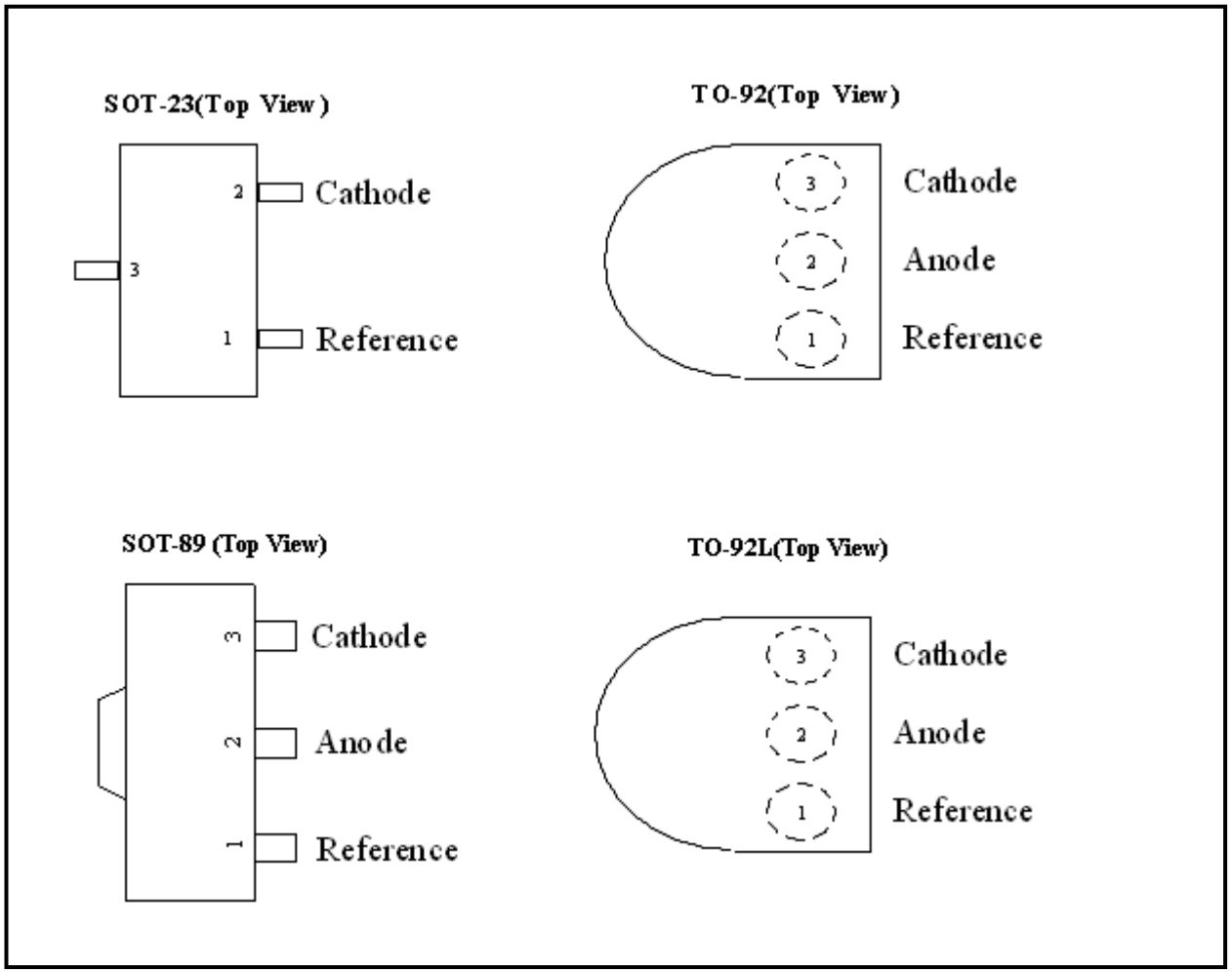
			TL432 A-rank(±0.5%)			TL432 B-rank(±1%)			
Parameter	Symbol	Condition	Min	Typ	Max	Min	Typ	Max	Unit
Reference Voltage	V_{REF}	V_Z=V_{REF},I_Z=10mA(Note 1)	1.234	1.240	1.246	1.228	1.240	1.252	V
V_{REF} Temperature Deviation	V_{DEV}	V_Z=V_{REF},I_Z=10mA,T_A=-40~105℃(Note 1)	-	10	20	-	10	20	mV
Ratio of Change in V_{REF} to change in V_Z	$\frac{\Delta V_{REF}}{\Delta V_Z}$	I_Z=10mA, ΔV_Z=18V to V_{REF}	-	-1	-2.0	-	-1	-2.0	mV/V
Reference Input Current	I_{REF}	R1=10kΩ,R2=∞, I_Z=10mA(Note2)	-	0.25	0.5	-	0.25	0.5	μA
I_{REF} Temperature Deviation	$I_{REF(DEV)}$	R1=10kΩ,R2=∞, I_Z=10mA(Note 2)	-	0.05	0.3	-	0.05	0.3	μA
Off-state Cathode Current	$I_{Z(OFF)}$	V_{REF}=0V,V_Z=18V(Note 3)	-	0.04	0.5	-	0.04	0.5	μA
Dynamic Output Impedance	r_z	f <1kHz,V_Z=V_{REF} I_Z=1mA to 100mA(Note 1)	-	0.2	0.4	-	0.2	0.4	Ω
Minimum Operating Current	$I_{Z(MIN)}$	V_Z=V_{REF}(Note 1)	-	60	80	-	60	80	μA

Notes:
(1) See Test Circuit 1.
(2) See Test Circuit 2.
(3) See Test Circuit 3.

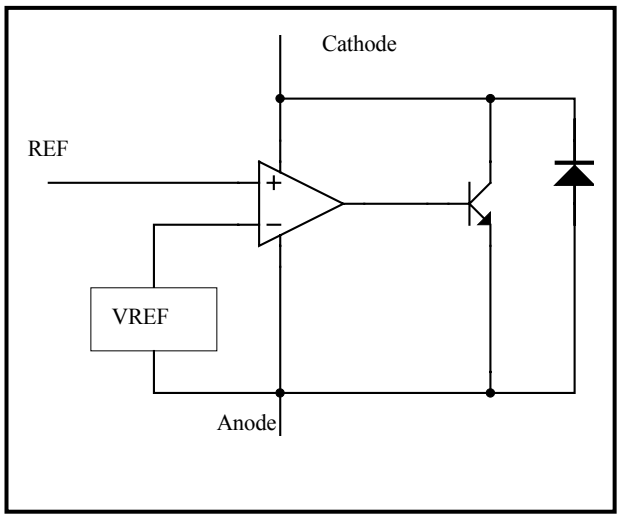
Test Circuits



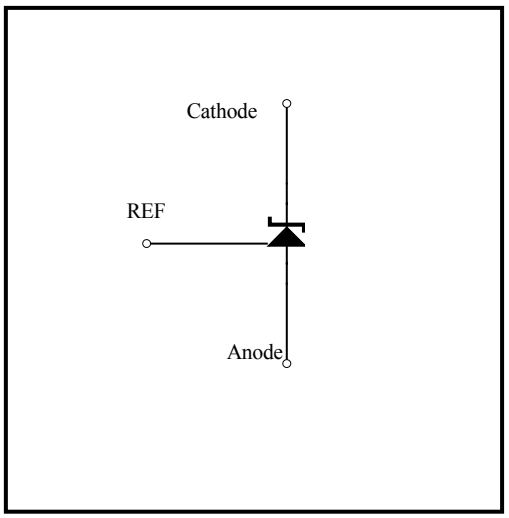
Pin Configurations



Block Diagram



Symbol

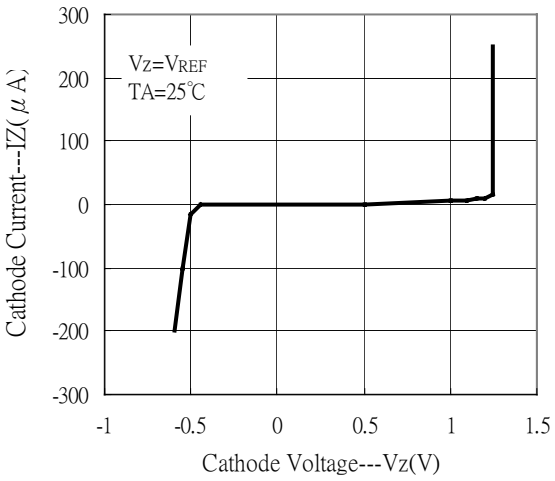


Ordering Information

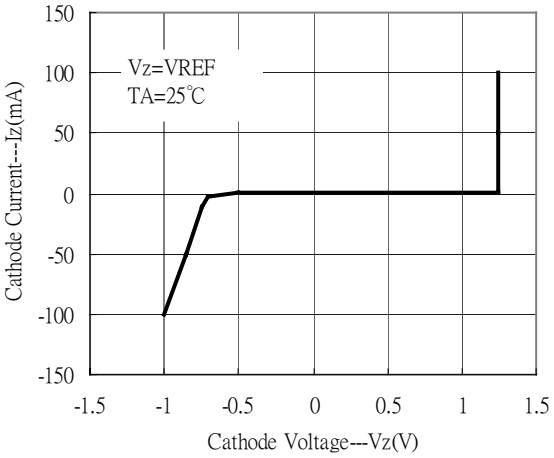
Device	Package	Rank	Tolerance	Shipping
TL432A3-A-TB-G	TO-92 (Pb-free lead plating and halogen-free package)	A	±0.5%	2000 pcs / Tape & Box
TL432A3-B-TB-G		B	±1%	
TL432A3-A-BK-G		A	±0.5%	1000 pcs/ bag, 10 bags/box, 10boxes/carton
TL432A3-B-BK-G		B	±1%	
TL432K3-A-TB-G	TO-92L (Pb-free lead plating and halogen-free package)	A	±0.5%	2000 pcs / Tape & Box
TL432K3-B-TB-G		B	±1%	
TL432K3-A-BK-G		A	±0.5%	500 pcs/ bag, 10 bags/box, 10boxes/carton
TL432K3-B-BK-G		B	±1%	
TL432N3-A-T1-G	SOT-23 (Pb-free lead plating and halogen-free package)	A	±0.5%	3000 pcs / Tape & Reel
TL432N3-B-T1-G		B	±1%	
TL432M3-A-T1-G	SOT-89 (Pb-free lead plating and halogen-free package)	A	±0.5%	1000 pcs / Tape & Reel
TL432M3-B-T1-G		B	±1%	

Typical Characteristics

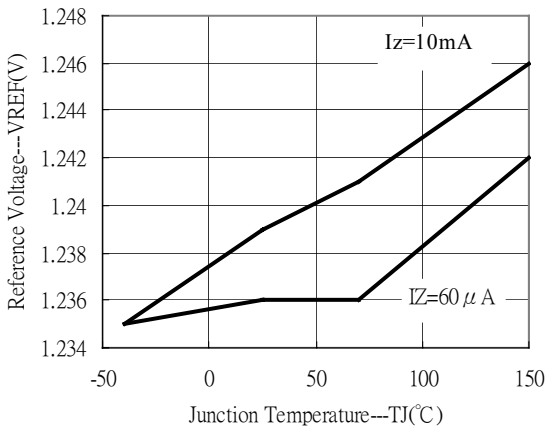
Cathode Current vs Cathode Voltage



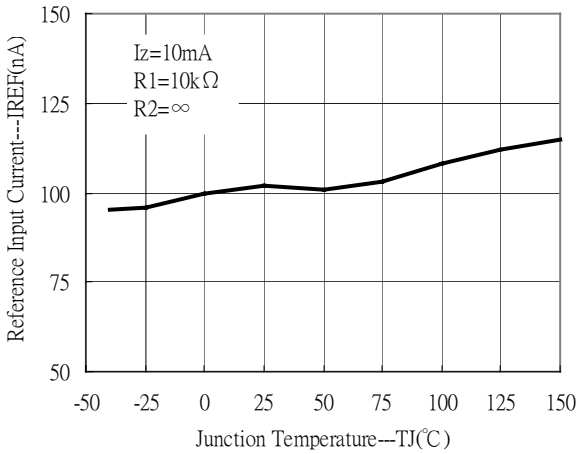
Cathode Current vs Cathode Voltage



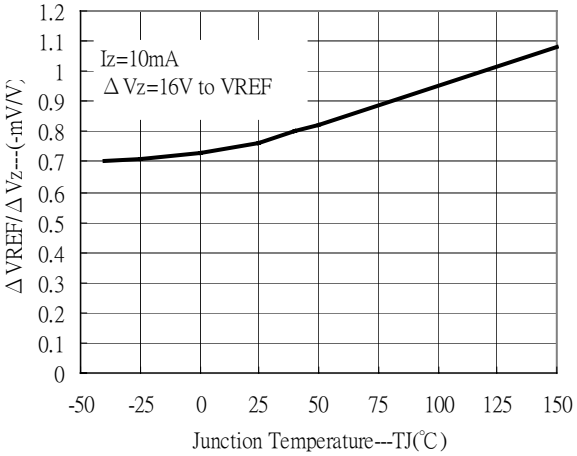
Reference Voltage vs Junction Temperature



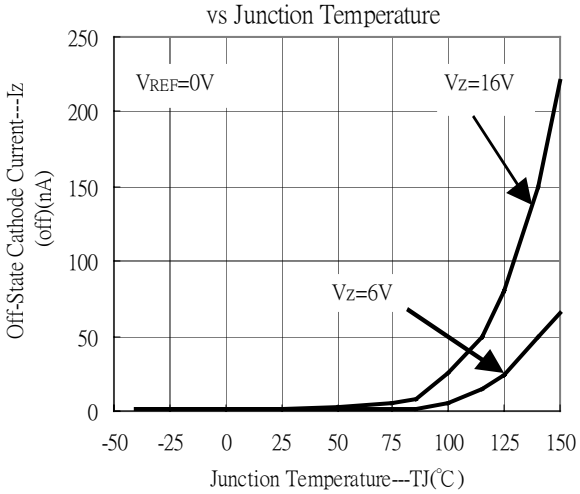
Reference Input Current vs Junction Temperature



Ratio of Delta Reference Voltage to Delta Cathode Voltage vs Junction Temperature

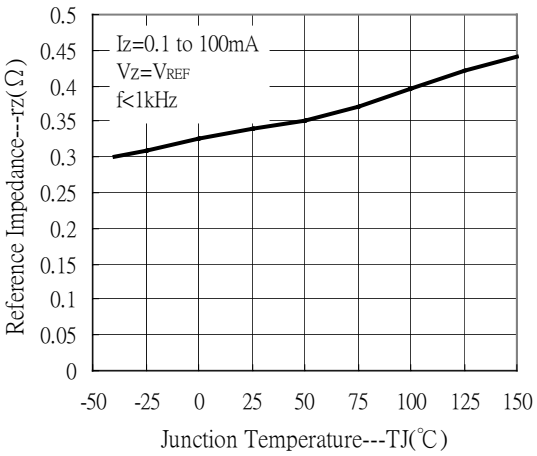


Off-State Cathode Current vs Junction Temperature

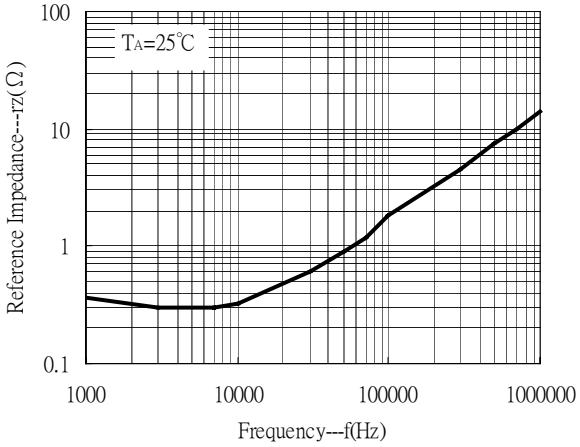


Typical Characteristics (Cont.)

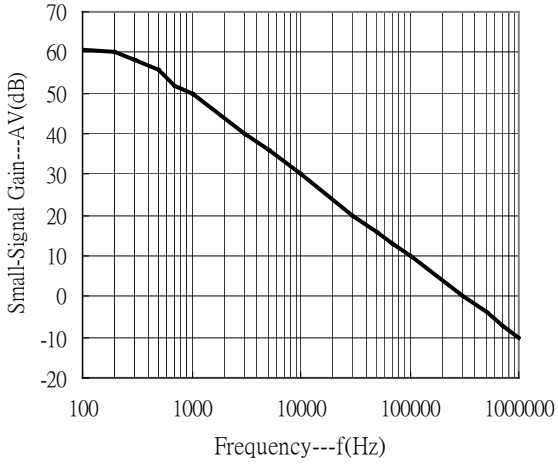
Reference Impedance vs Junction Temperature



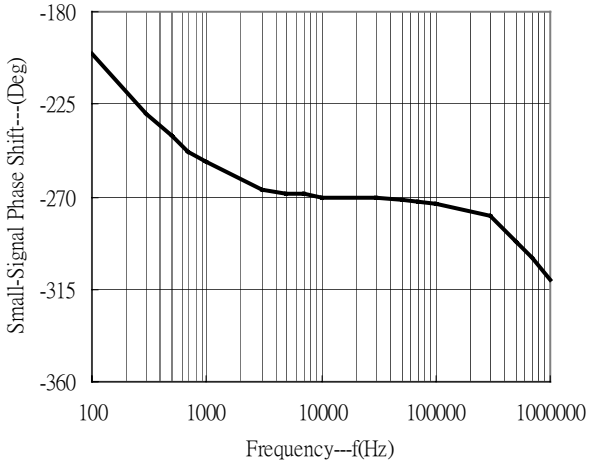
Reference Impedance vs Frequency



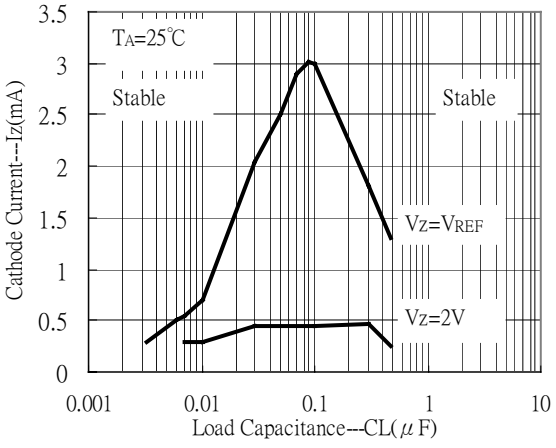
Small-Signal Gain vs Frequency



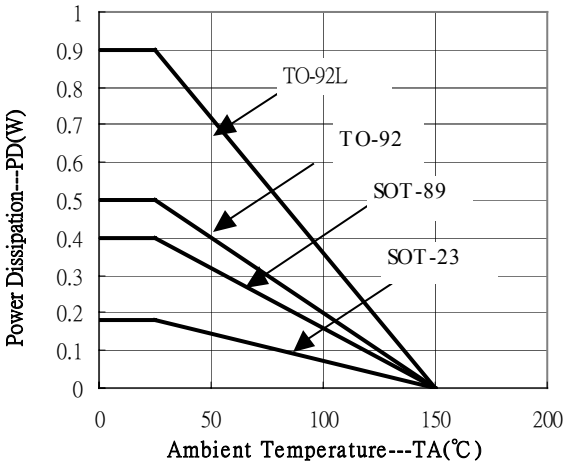
Small-Signal Phase Shift vs Frequency



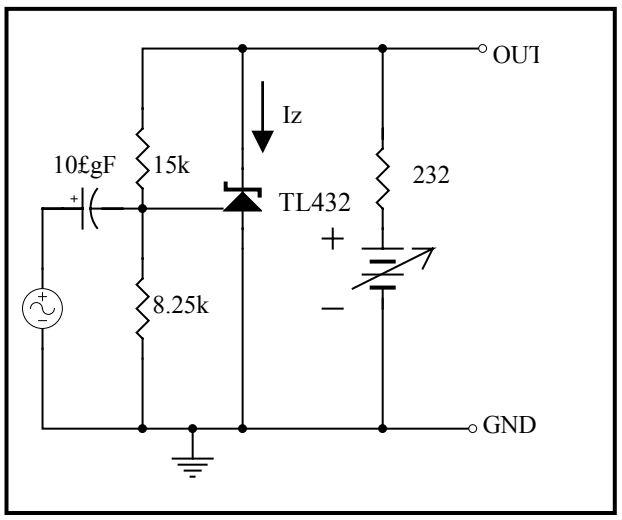
Stability Boundary Condition For Shunt Regulation
vs Cathode Current and Load Capacitance



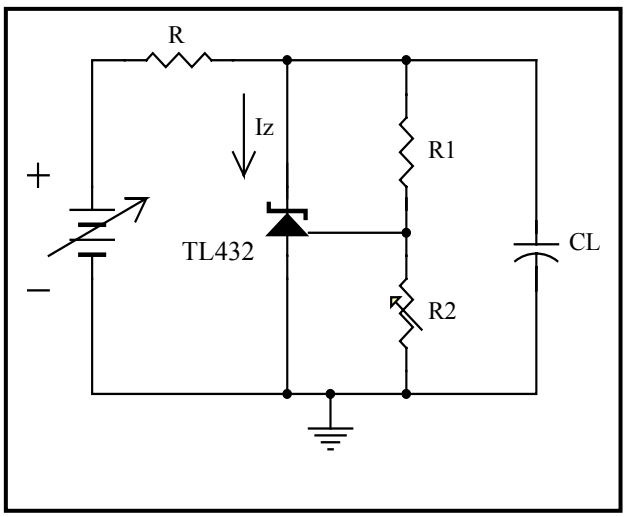
Power Derating Curves



Test Circuit-Small-Signal Gain and Phase



Test Circuit-Stability

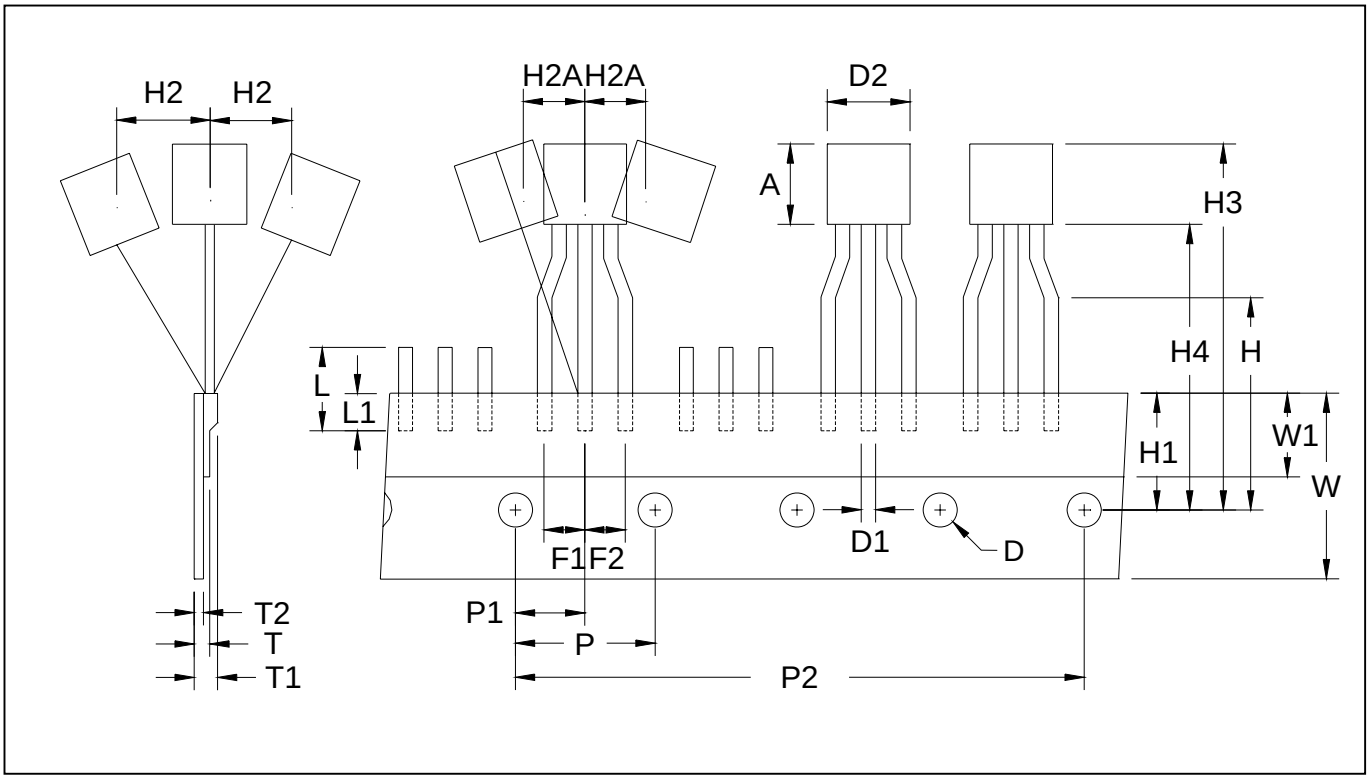


Applications Information - Stability

Selection of load capacitance when using TL432 as a shunt regulator

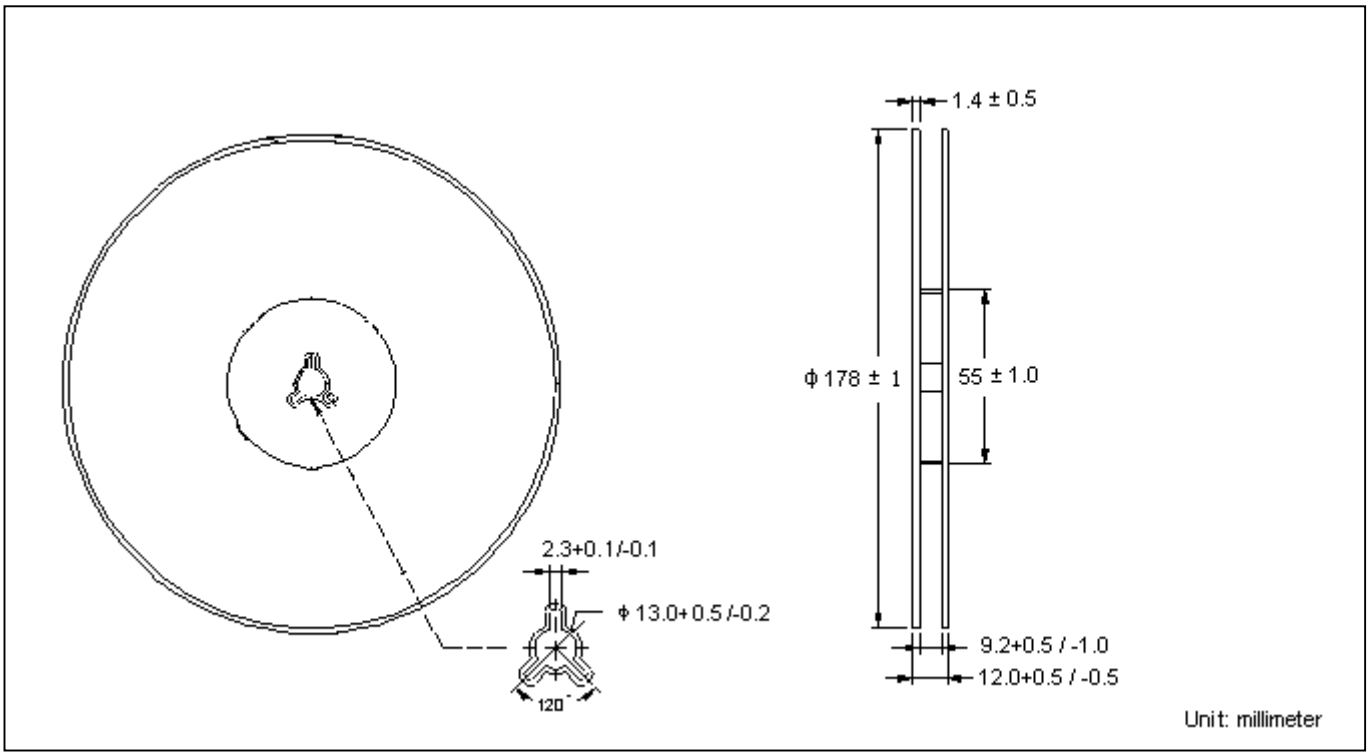
When the TL432 is used as a shunt regulator, two options for selection of C_L(see diagram on page 6) are recommended for optimal stability:
1) No load capacitance across the device, decouple at the load.
2) Large capacitance across the device, optimal decoupling at the load.
The reason for this is that TL432 exhibits instability with capacitances in the range of 10nF to 1μF (approx.) at light cathode currents(up to 3mA typical). The device is less stable the lower the cathode voltage has been set for. Therefore while the device will be perfectly stable operating at a cathode current of (say) 10mA with a 0.1μF capacitor across it, it will oscillate transiently during start-up as the cathode current passes through the instability region. Selecting a very low (or preferably, no) capacitance, or alternatively a high capacitance(such as 10μF) will avoid this issue altogether. Since the user will probably wish to have local decoupling at the load anyway, the most cost effective method is to use no capacitance at all directly across the device. PCB trace/via resistance and inductance prevent the local load decoupling from causing the oscillation during the transient start-up phase.
Note : if the TL432 is located right at the load, so the load decoupling capacitor is directly across it, then this capacitor will have to be ≤1nF or ≥10μF.

TO-92 Taping Outline

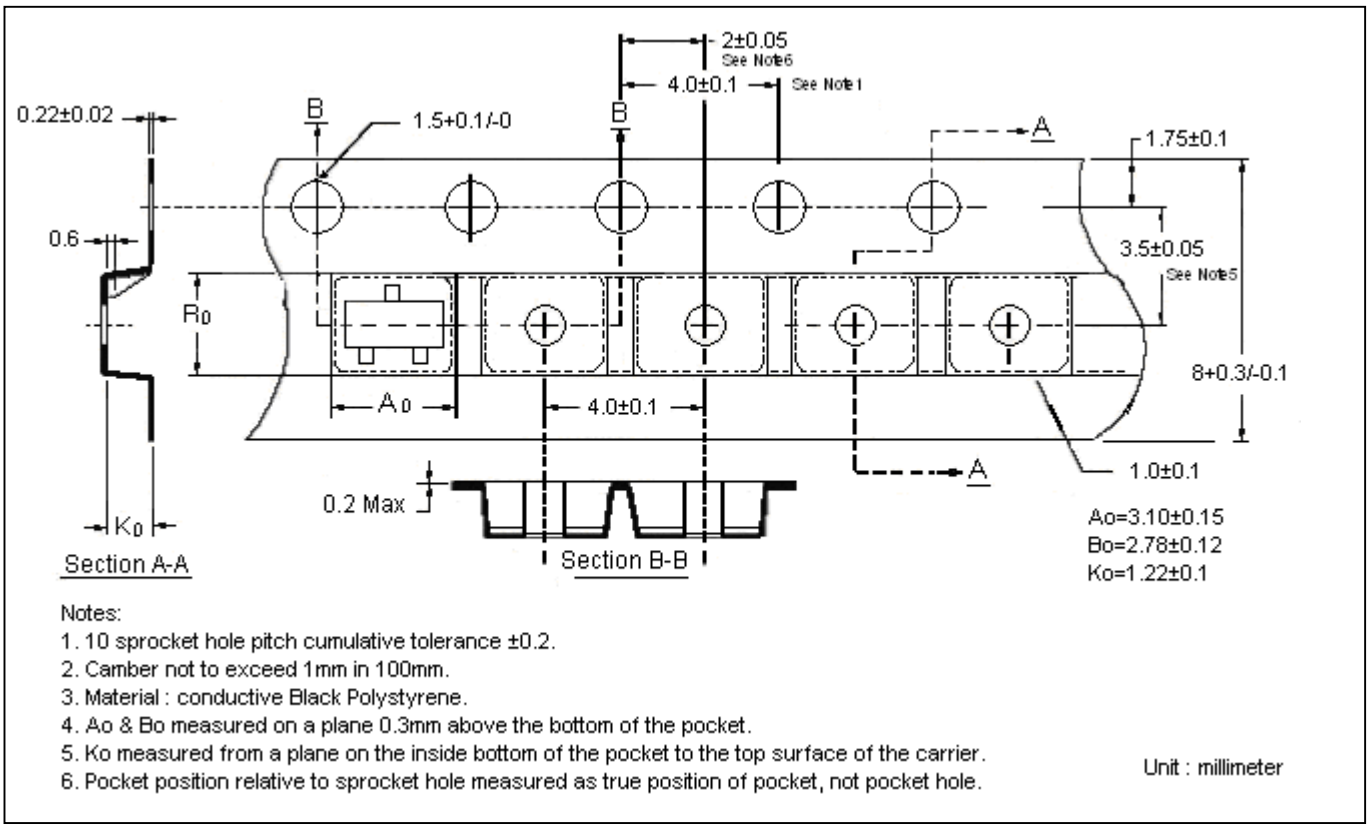


DIM	Item	Millimeters	
		Min.	Max.
A	Component body height	4.33	4.83
D	Tape Feed Diameter	3.80	4.20
D1	Lead Diameter	0.36	0.53
D2	Component Body Diameter	4.33	4.83
F1,F2	Component Lead Pitch	2.40	2.90
F1,F2	F1-F2	-	±0.3
H	Height Of Seating Plane	15.50	16.50
H1	Feed Hole Location	8.50	9.50
H2	Front To Rear Deflection	-	1
H2A	Deflection Left Or Right	-	1
H3	Component Height	-	27
H4	Feed Hole To Bottom Of Component	-	21
L	Lead Length After Component Removal	-	11
L1	Lead Wire Enclosure	2.50	-
P	Feed Hole Pitch	12.50	12.90
P1	Center Of Seating Plane Location	5.95	6.75
P2	4 Feed Hole Pitch	50.30	51.30
T	Over All Tape Thickness	-	0.55
T1	Total Taped Package Thickness	-	1.42
T2	Carrier Tape Thickness	0.36	0.68
W	Tape Width	17.50	19.00
W1	Adhesive Tape Width	5.00	7.00
-	20 pcs Pitch	253	255

SOT-23 Reel Dimension



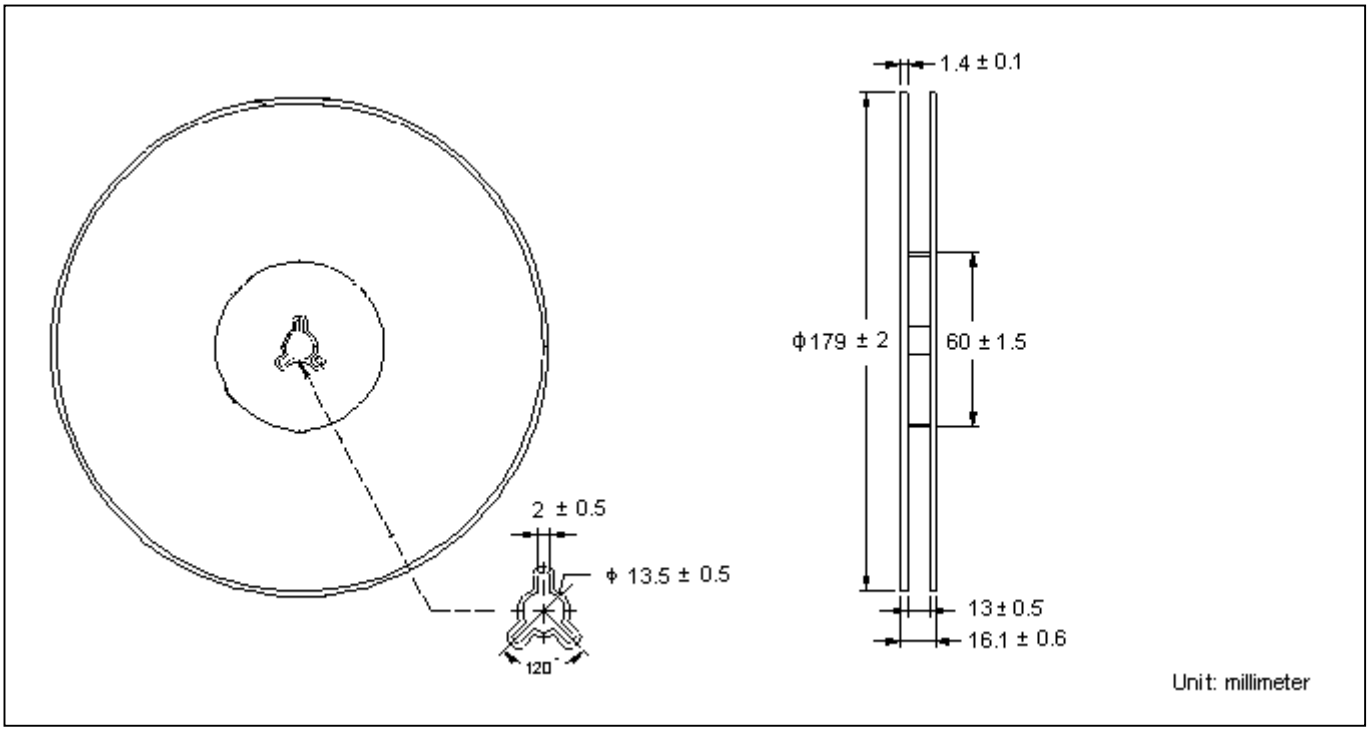
SOT-23 Carrier Tape Dimension



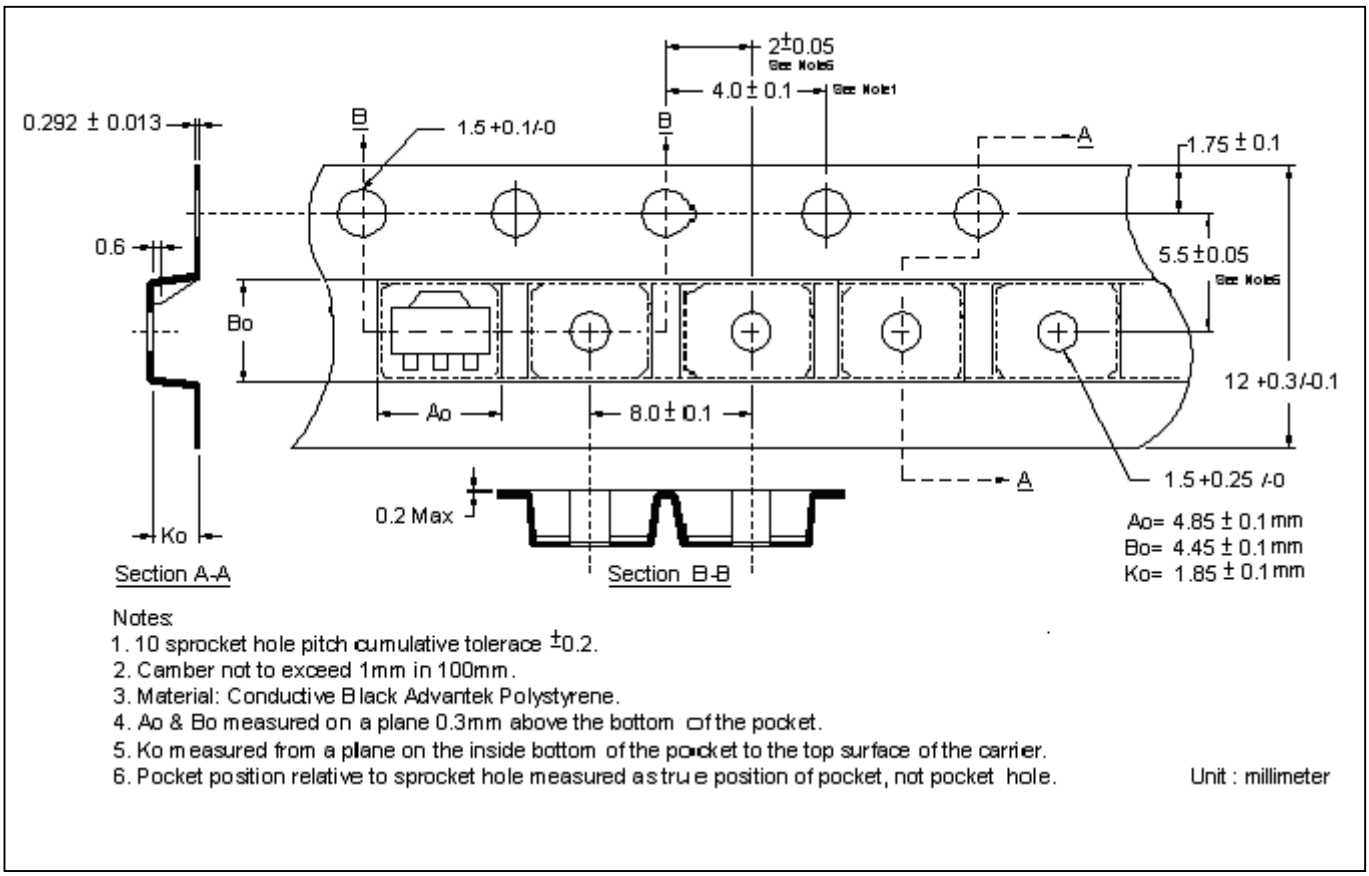
Notes:
1. 10 sprocket hole pitch cumulative tolerance ±0.2.
2. Camber not to exceed 1mm in 100mm.
3. Material : conductive Black Polystyrene.
4. Ao & Bo measured on a plane 0.3mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Unit : millimeter

SOT-89 Reel Dimension



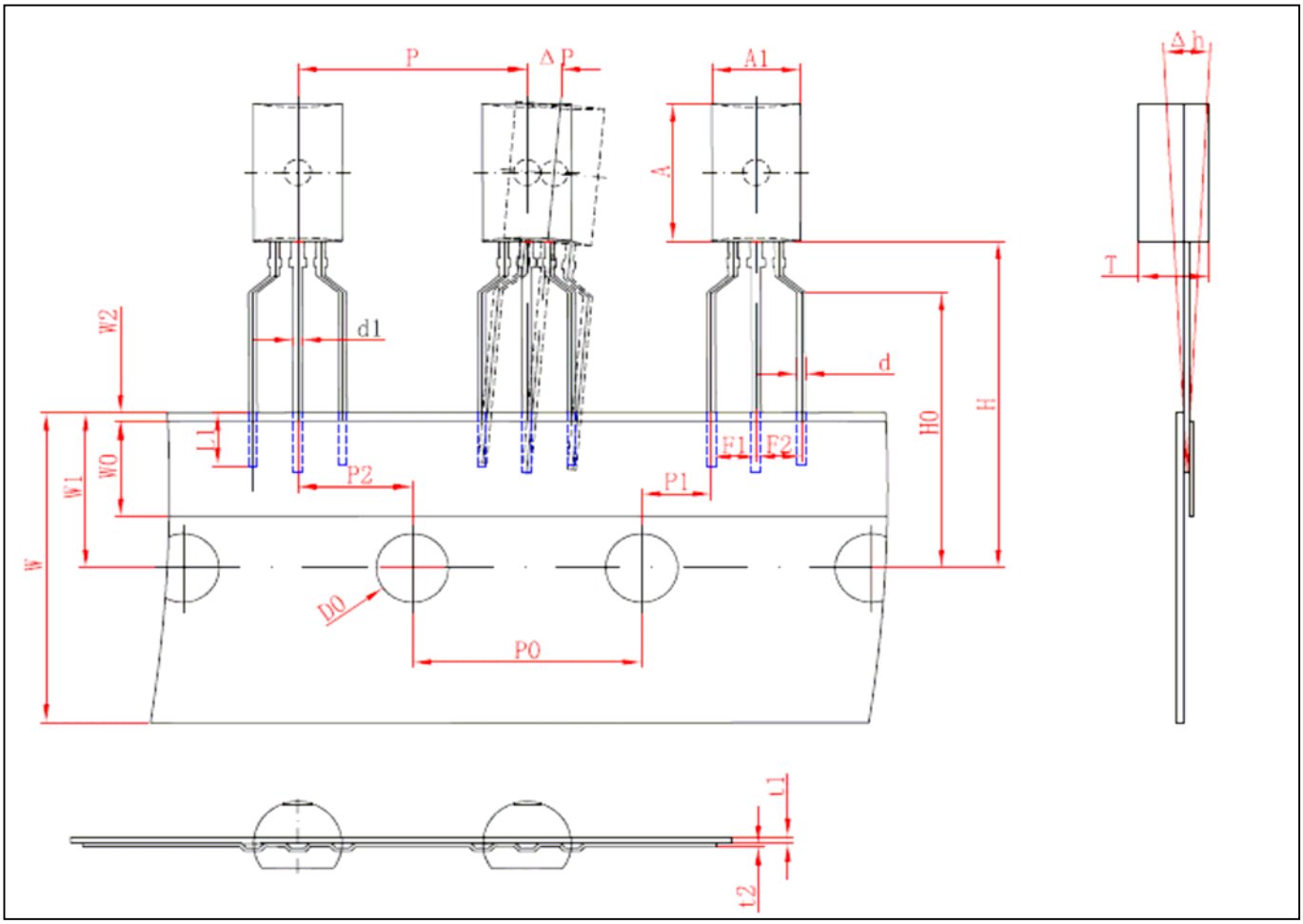
SOT-89 Carrier Tape Dimension



Notes:
1. 10 sprocket hole pitch cumulative tolerace ±0.2.
2. Camber not to exceed 1mm in 100mm.
3. Material: Conductive Black Advantek Polystyrene.
4. Ao & Bo measured on a plane 0.3mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

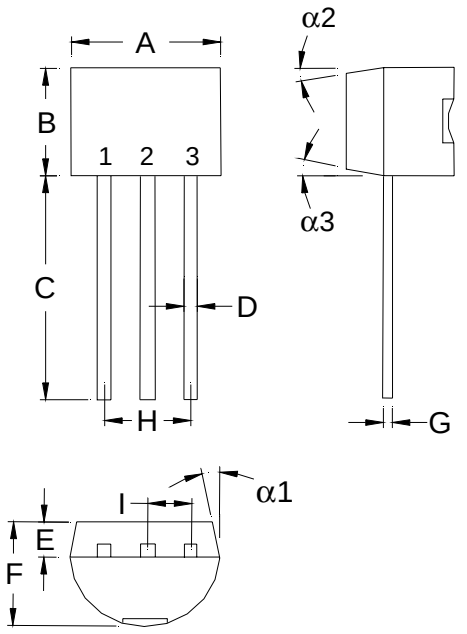
Unit : millimeter

TO-92L Taping Outline

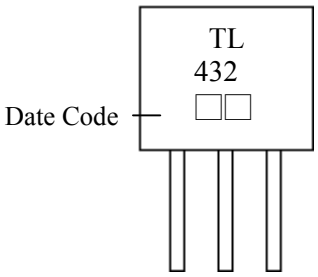


DIM	Item	Millimeters	
		Min.	Max.
A1	Component body width	4.70	5.10
A	Component body height	7.80	8.20
T	Component body thickness	3.70	4.10
d	Lead wire diameter	0.40	0.50
d1	Lead wire diameter 1	0.62	0.78
P	Pitch of component	12.40	13.00
P0	Feed hole pitch	12.50	12.90
P2	Hole center to component center	6.05	6.65
F1, F2	Lead to lead distance	2.20	2.80
△h	Component alignment, F-R	-1.00	1.00
W	Tape width	17.50	19.00
W0	Hole down tape width	5.50	6.50
W1	Hole position	8.50	9.50
W2	Hole down tape position	-	1.00
H	Height of component from tape center	19.00	21.00
H0	Lead wire clinch height	15.50	16.50
L1	Lead wire (tape portion)	2.50	-
D0	Feed hole diameter	3.80	4.20
t1	Taped lead thickness	0.35	0.45
t2	Carrier tape thickness	0.15	0.25
P1	Position of hole	3.55	4.15
△P	Component alignment	-1.00	1.00

TO-92 Dimension



Marking:



Style: Pin 1.Reference 2.Anode 3.Cathode

3-Lead TO-92 Plastic Package
CYStek Package Code: A3

*: Typical

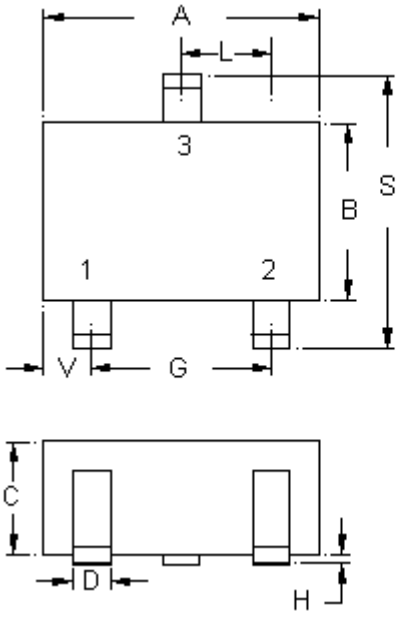
DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1704	0.1902	4.33	4.83	G	0.0142	0.0220	0.36	0.56
B	0.1704	0.1902	4.33	4.83	H	-	*0.1000	-	*2.54
C	0.5000	-	12.70	-	I	-	*0.0500	-	*1.27
D	0.0142	0.0220	0.36	0.56	α1	-	*5°	-	*5°
E	-	*0.0500	-	*1.27	α2	-	*2°	-	*2°
F	0.1323	0.1480	3.36	3.76	α3	-	*2°	-	*2°

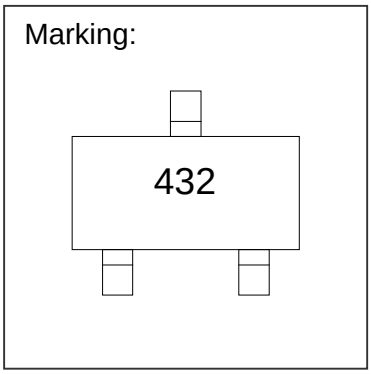
Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

SOT-23 Dimension





3-Lead SOT-23 Plastic
Surface Mounted Package
CYStek Package Code: N3

Style: Pin 1.Reference 2.Cathode
3.Anode

*: Typical

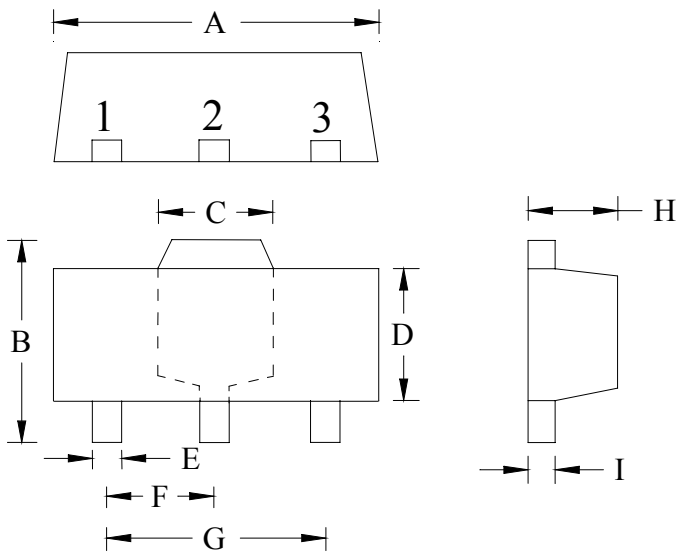
DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1102	0.1204	2.80	3.04	J	0.0032	0.0079	0.08	0.20
B	0.0472	0.0669	1.20	1.70	K	0.0118	0.0266	0.30	0.67
C	0.0335	0.0512	0.89	1.30	L	0.0335	0.0453	0.85	1.15
D	0.0118	0.0197	0.30	0.50	S	0.0830	0.1161	2.10	2.95
G	0.0669	0.0910	1.70	2.30	V	0.0098	0.0256	0.25	0.65
H	0.0000	0.0040	0.00	0.10	L1	0.0118	0.0197	0.30	0.50

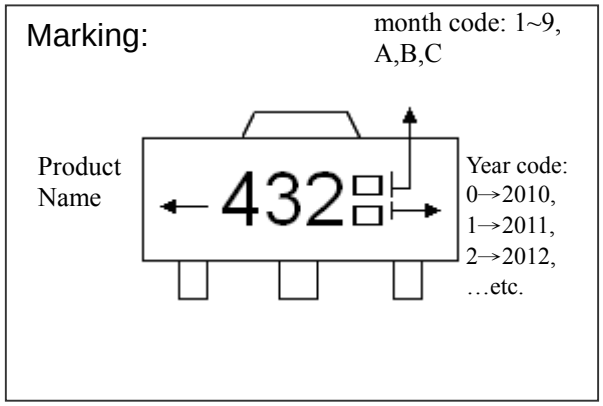
Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYCtek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

SOT-89 Dimension





Style: Pin 1. Reference 2. Anode

3. Cathode

3-Lead SOT-89 Plastic
Surface Mounted Package
CYStek Package Code: M3

*: Typical

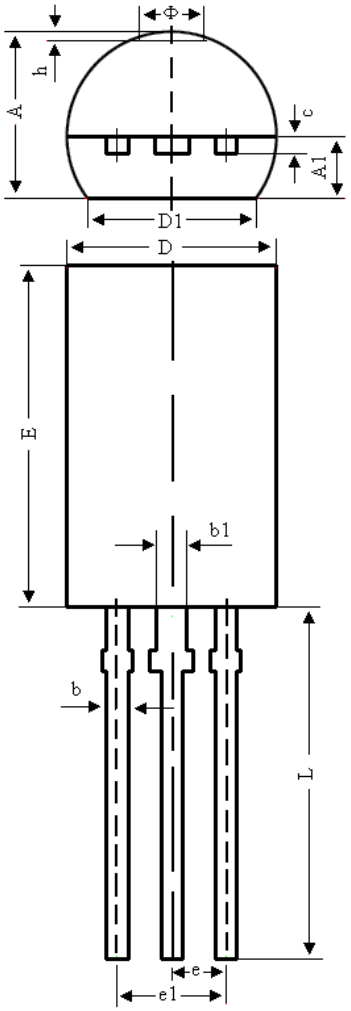
DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1732	0.1811	4.40	4.60	F	0.0583	0.0598	1.48	1.527
B	0.1594	0.1673	4.05	4.25	G	0.1165	0.1197	2.96	3.04
C	0.0591	0.0663	1.50	1.70	H	0.0551	0.0630	1.40	1.60
D	0.0945	0.1024	2.40	2.60	I	0.0138	0.0161	0.35	0.41
E	0.01417	0.0201	0.36	0.51					

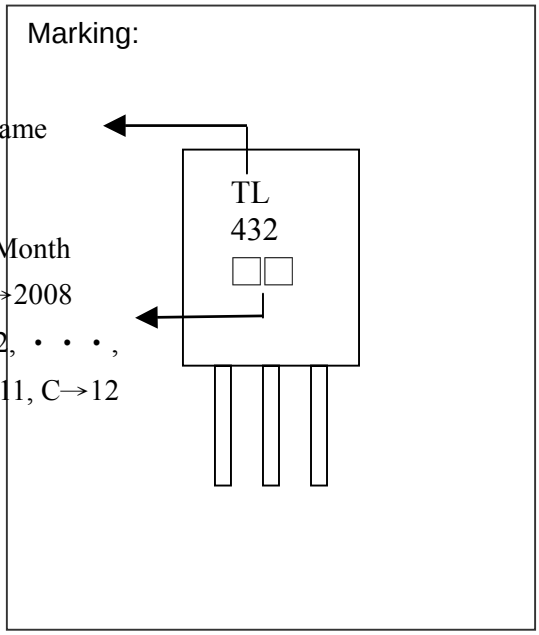
Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

TO-92L Dimension





Date Code: Year+Month

Year: 7→2007, 8→2008

Month: 1→1, 2→2, ・・・,
9→9, A→10, B→11, C→12

Style: Pin 1. Reference 2. Anode
3. Cathode

3-Lead TO-92L Plastic Package
CYStek Package Code: K3

*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.146	0.161	3.700	4.100	E	0.307	0.323	7.800	8.200
A1	0.050	0.062	1.280	1.580	e	*0.05		*1.270	
b	0.014	0.022	0.350	0.550	e1	0.096	0.104	2.440	2.640
b1	0.024	0.031	0.600	0.800	L	0.543	0.559	13.800	14.200
c	0.014	0.018	0.350	0.450	φ	-	0.063	-	1.600
D	0.185	0.201	4.700	5.100	h	0.000	0.012	0.000	0.300
D1	0.157	-	4.000	-					

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.