

1A /200V Snubber Damping Rectifier

QE

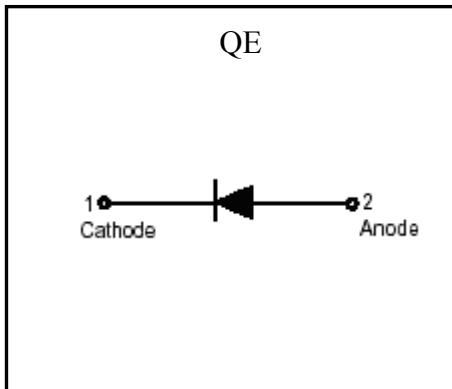
Features

- High current capability
- Smoothly soft reverse recovery time (trr)
- Low profile surface mounted package in order to minimize board space
- Pb-free lead plating and halogen-free package

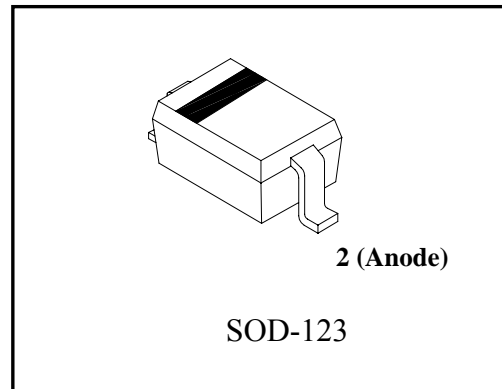
Mechanical data

- Case : Molded plastic, JEDEC SOD-123.
- Epoxy : UL94-V0 rated flame retardant
- Terminals : Plated terminals, solderable per MIL-STD-202 method 208
- Polarity : Indicated by cathode band
- Mounting position : Any
- Weight : approx. 0.009 gram

Symbol

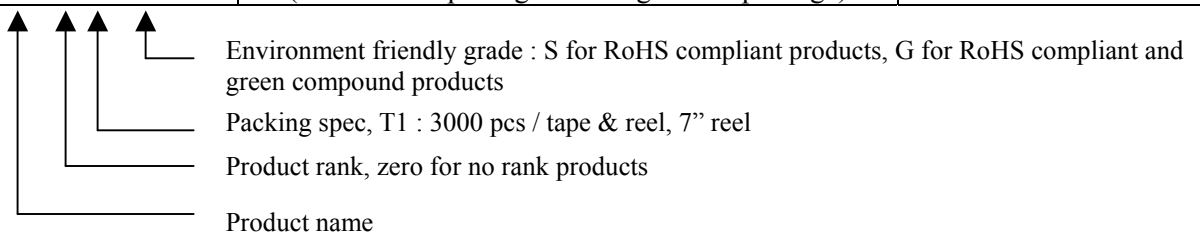


Outline



Ordering Information

Device	Package	Shipping
QE-0-T1-G	SOD-123 (Pb-free lead plating and halogen-free package)	3000 pcs / tape & reel



**Absolute Maximum Ratings** ($T_A=25^\circ\text{C}$, unless otherwise noted)

Parameters	Conditions	Symbol	Value	Units
Repetitive peak reverse voltage		V_{RRM}	200	V
RMS voltage		V_{RMS}	140	V
Continuous reverse voltage		V_R	200	V
Forward rectified current	Single phase half wave, 60Hz @ $T_J=25^\circ\text{C}$	$I_{F(AV)}$	1	A
Repetitive Peak Forward Current	Single phase half wave, 60Hz @ $T_J=25^\circ\text{C}$	I_{FRM}	1.57	A
Forward surge current	8.3ms single half sine-wave superimposed on rated load (JEDEC method)	I_{FSM}	6	A
	$t_p \leq 1\mu\text{s}$		20	
Maximum reverse recovery time	$I_F=1\text{A}$, $dI_F/dt=100\text{A}/\mu\text{s}$	t_{rr}	500	ns
Storage temperature range		T_{stg}	-55~+150	$^\circ\text{C}$
Operating junction temperature range		T_J	-55~+150	$^\circ\text{C}$

Thermal Data

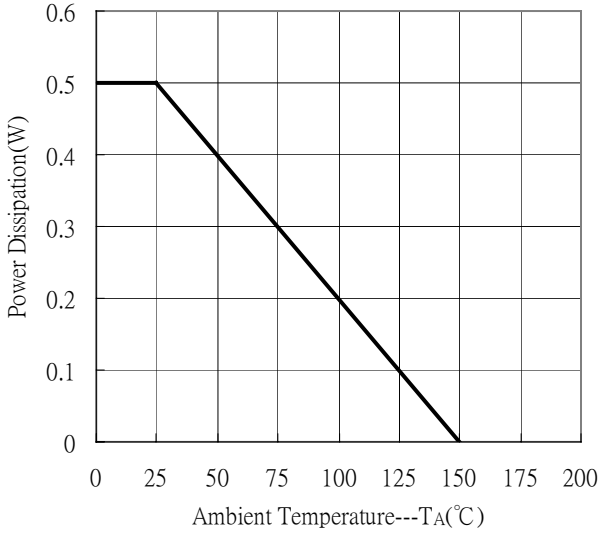
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{th,j-c}$	50	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-ambient, max (Note)	$R_{th,j-a}$	250	

Note: When mounted on FR-4 PCB with area measuring 10×10 mm**Characteristics** ($T_A=25^\circ\text{C}$, unless otherwise noted)

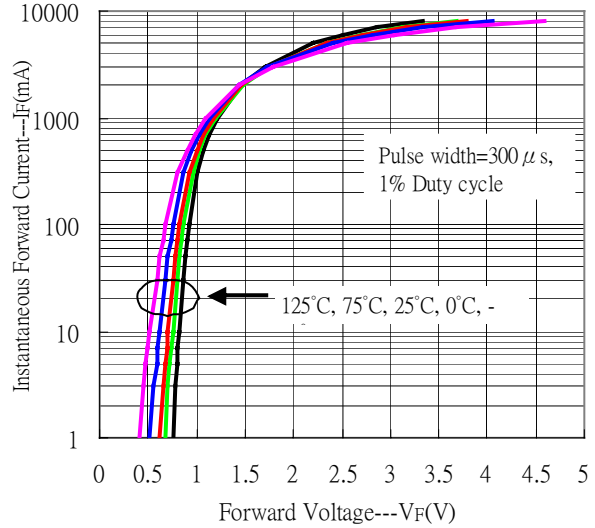
Characteristic	Symbol	Condition	Min.	Typ	Max.	Unit
Reverse Voltage	V_R	$I_R=100\mu\text{A}$	200	-	-	V
Forward Voltage	$V_F 1$	$I_F=100\text{mA}$	-	-	0.95	V
	$V_F 2$	$I_F=500\text{mA}$	-	-	1.2	
Reverse Leakage Current	I_R	$V_R=200\text{V}$	-	-	100	nA
	I_R	$V_R=200\text{V}$, $T_A=125^\circ\text{C}$	-	-	1	μA
Junction Capacitance	C_J	$V_R=1\text{V}$, $f=1\text{MHz}$	-	2.9	-	pF

Typical Characteristics

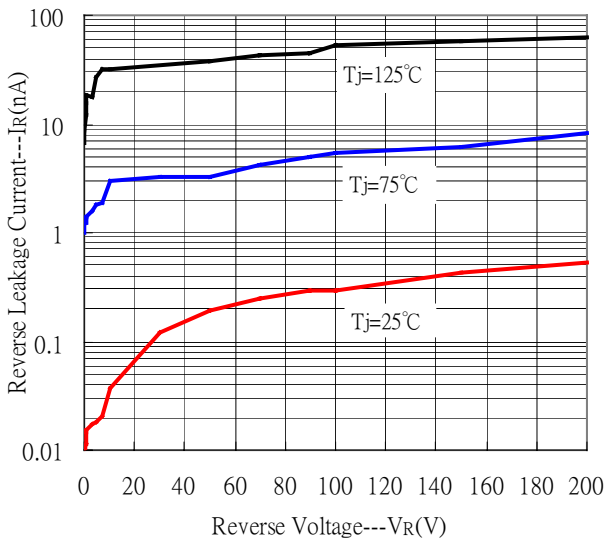
Power Derating Curve



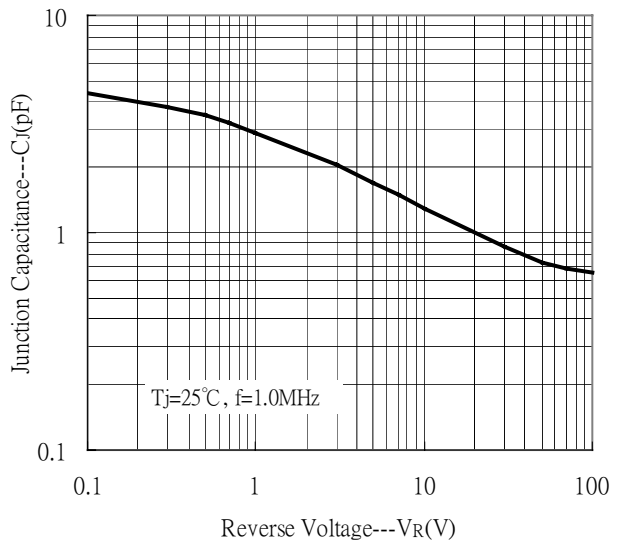
Forward Current vs Forward Voltage



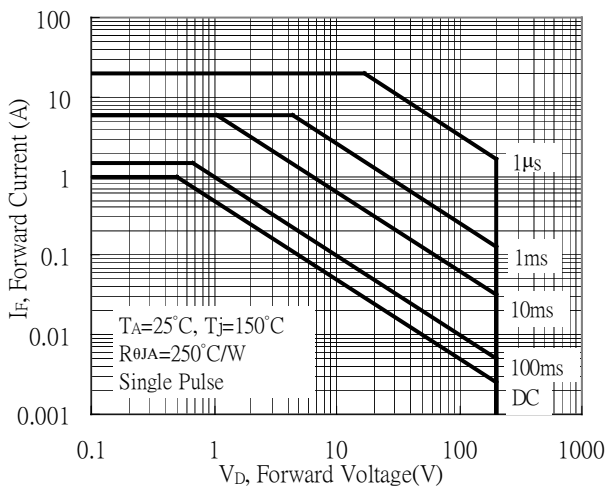
Reverse Leakage Current vs Reverse Voltage



Junction Capacitance vs Reverse Voltage

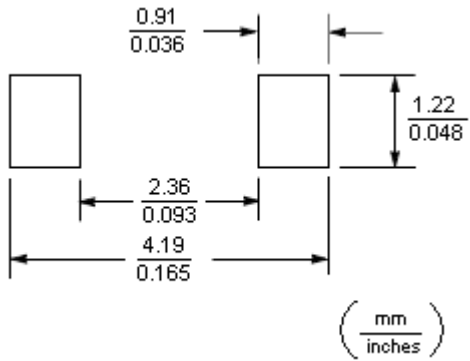


Maximum Safe Operating Area

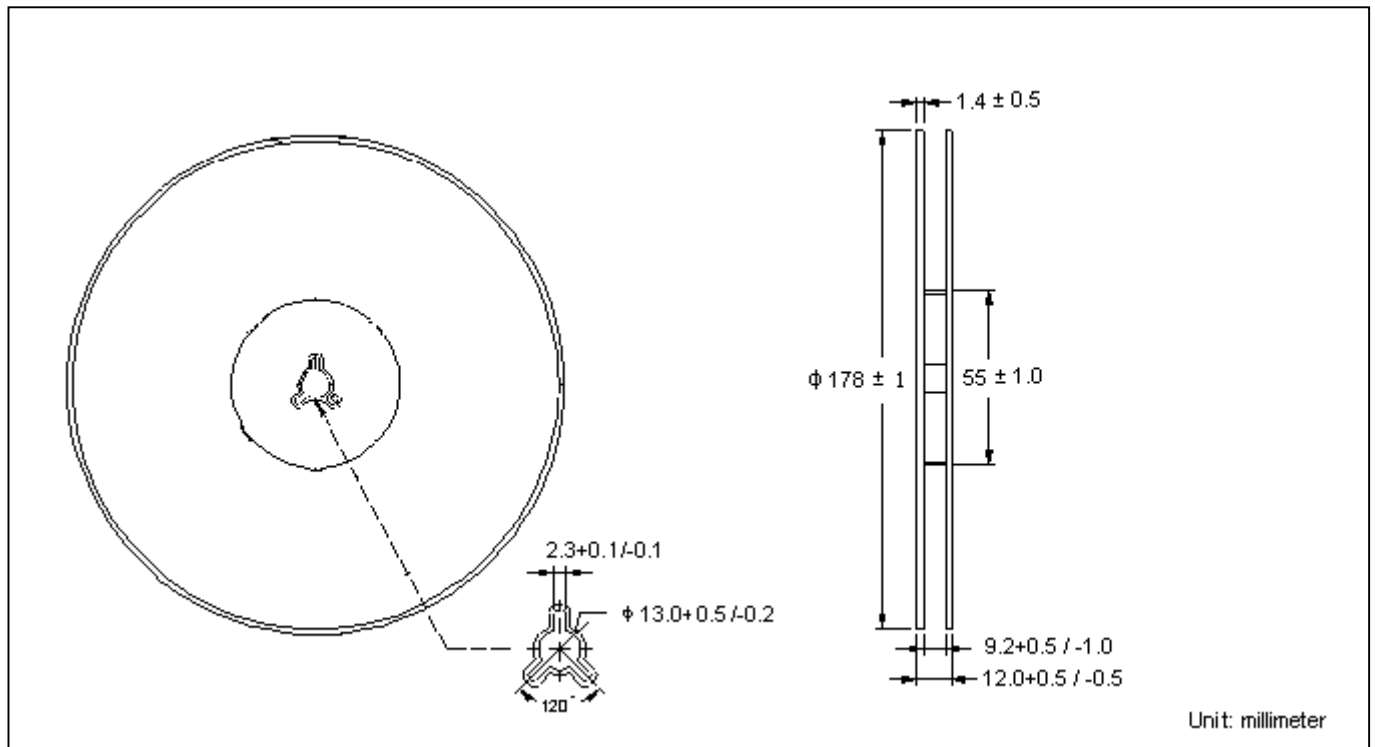




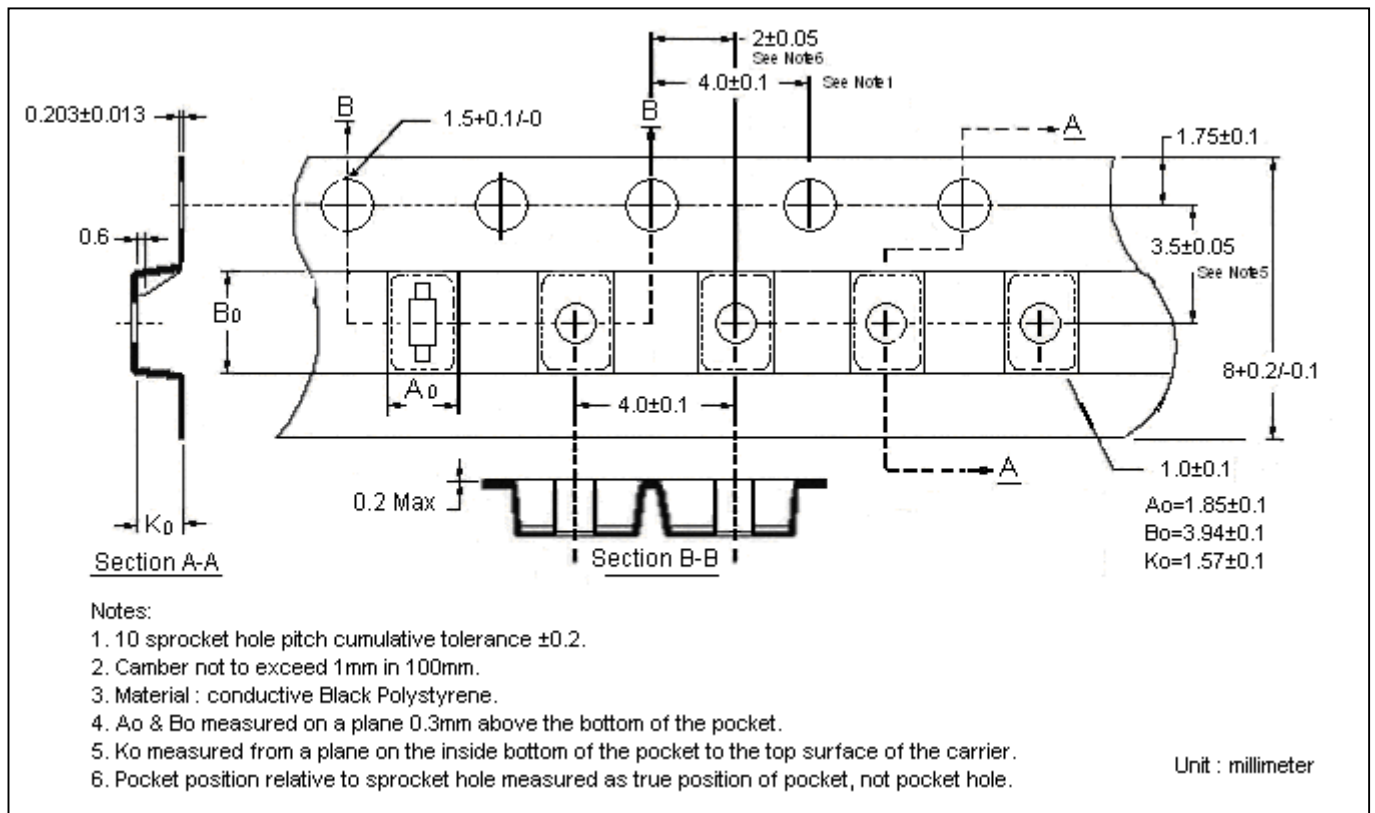
Recommended Soldering Footprint



Reel Dimension



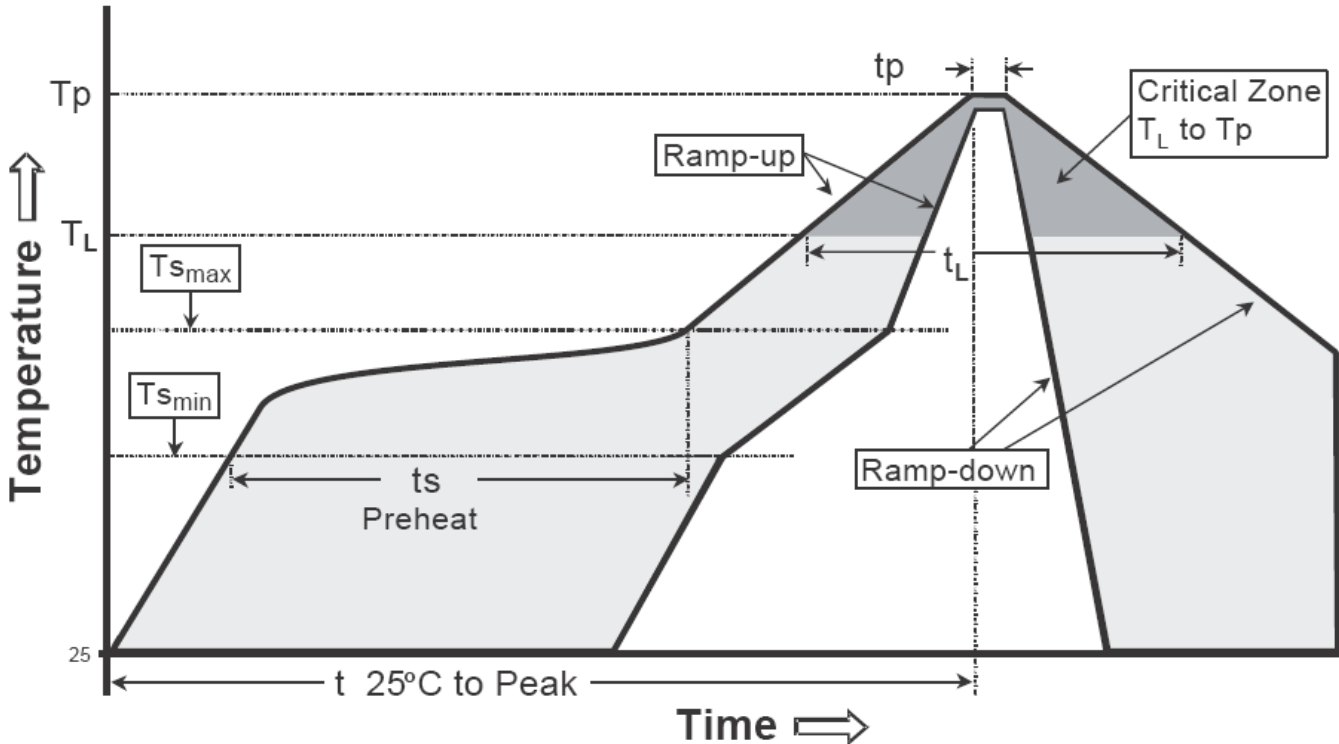
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

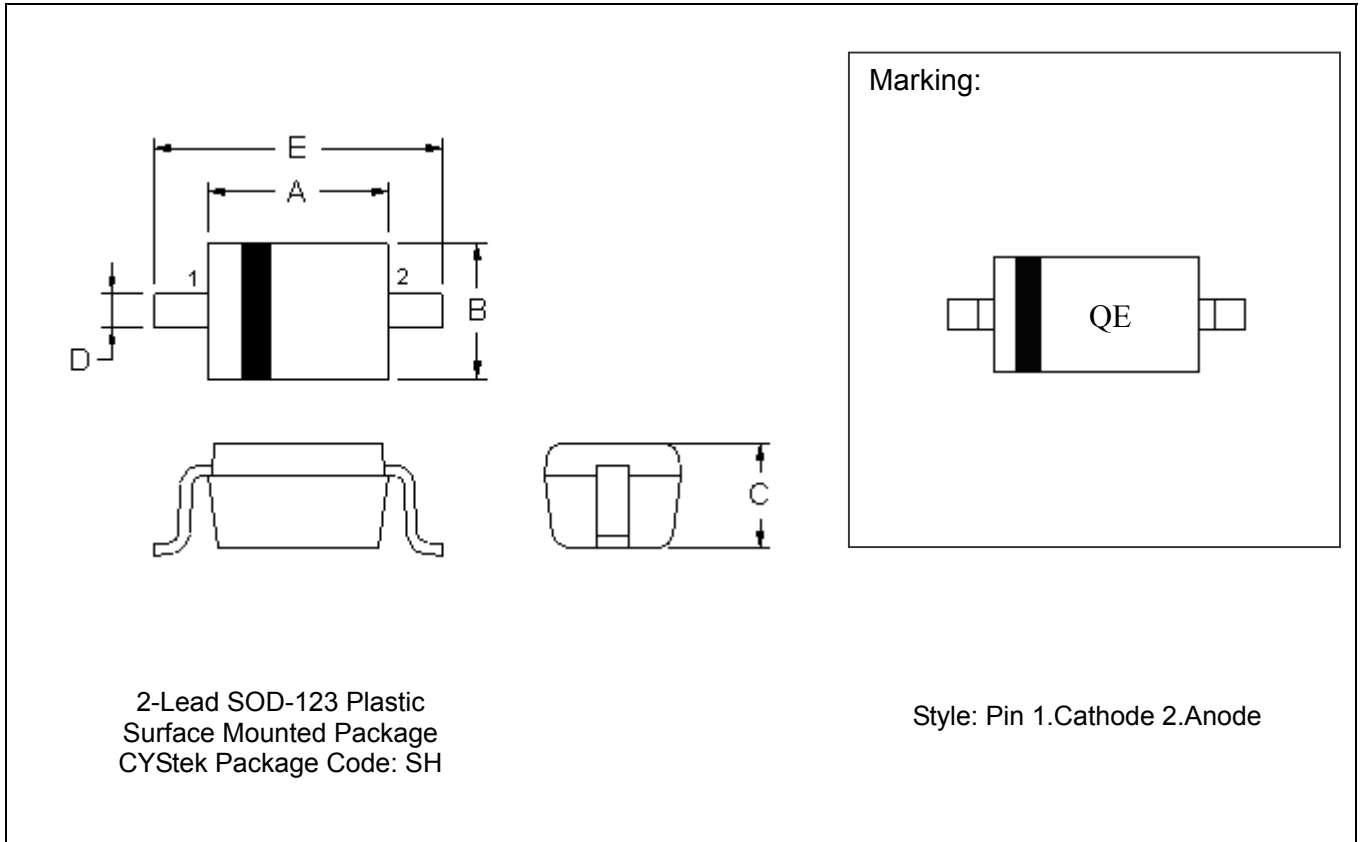
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Ts_max to T _P)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _s min)	100°C	150°C
-Temperature Max(T _s max)	150°C	200°C
-Time(ts_min to ts_max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note :1. All temperatures refer to topside of the package, measured on the package body surface.
 2. For devices mounted on FR-4 PCB of 1.6mm or equivalent grade PCB. If other grade PCB is used, care should be taken to match the coefficients of thermal expansion between components and PCB. If they are not matched well, the solder joints may crack or the bodies of the parts may crack or shatter as the assembly cools.

SOD-123 Dimension



2-Lead SOD-123 Plastic
 Surface Mounted Package
 CYStek Package Code: SH

Style: Pin 1.Cathode 2.Anode

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.102	0.110	2.600	2.800	D	0.018	0.026	0.450	0.650
B	0.059	0.067	1.500	1.700	E	0.140	0.152	3.550	3.850
C	0.041	0.049	1.050	1.250					

Notes: 1.Controlling dimension : millimeters.
 2.Lead thickness specified per L/F drawing with solder plating.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.