

P-Channel Enhancement Mode Power MOSFET

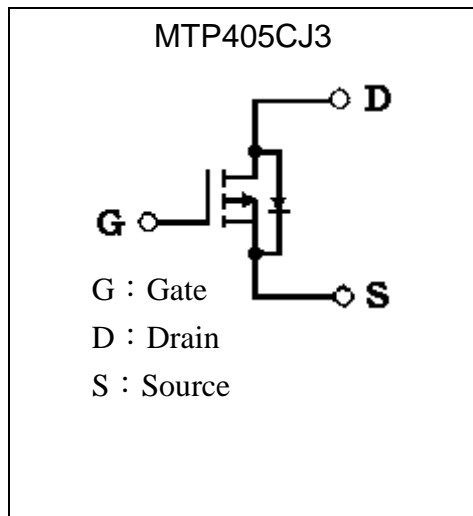
MTP405CJ3

BV_{DSS}	-30V
I_D @ V_{GS}=-10V, T_C=25°C	-34A
R_{DS(ON)}@ V_{GS}=-10V, I_D=-18A	21mΩ (typ)
R_{DS(ON)}@ V_{GS}=-4.5V, I_D=-10A	33mΩ (typ)

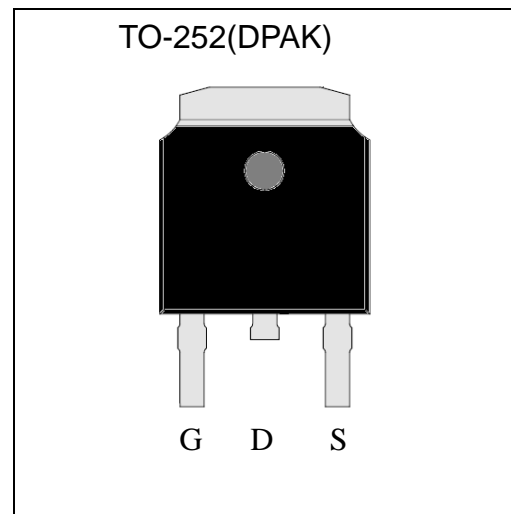
Features

- Single Drive Requirement
- Low On-resistance
- Fast switching Characteristic
- Pb-free lead plating and halogen-free package

Symbol

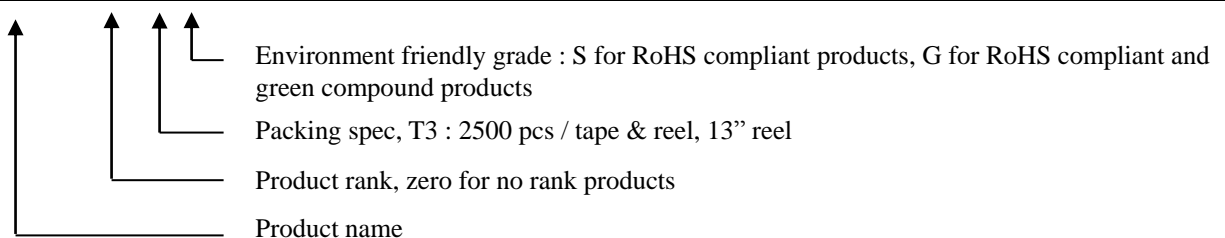


Outline



Ordering Information

Device	Package	Shipping
MTP405CJ3-0-T3-G	TO-252 (Pb-free lead plating package)	2500 pcs / Tape & Reel





Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit	
Drain-Source Voltage	V _{DS}	-30	V	
Gate-Source Voltage	V _{GS}	±20		
Continuous Drain Current @V _{GS} =-10V, T _C =25°C	I _D	-34	A	
Continuous Drain Current @V _{GS} =-10V, T _C =100°C		-21.5		
Continuous Drain Current @V _{GS} =-10V, T _A =25°C		-18		
Continuous Drain Current @V _{GS} =-10V, T _A =100°C		-11.4		
Pulsed Drain Current	I _{DM}	-80 *1	A	
Power Dissipation	P _D	T _C =25°C	50 *4	W
		T _C =100°C	20 *4	
		T _A =25°C	2.5	
		T _A =100°C	1.0	
Single Pulse Avalanche Energy	E _{AS}	45 *2	mJ	
Single Pulse Avalanche Current	I _{AS}	-18	A	
Operating Junction and Storage Temperature	T _j , T _{stg}	-55~+150	°C	

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	R _{th,j-c}	2.5	°C/W
Thermal Resistance, Junction-to-ambient, max	R _{th,j-a}	50 *3	°C/W

Note : *1. Pulse width limited by safe operating area.

*2 . T_j=25°C, V_{DD}=-15V, L=0.14mH, R_G=25Ω.

*3 . The value of R_{th,j-a} is measured with the device mounted on 1 in² FR-4 board with 2 oz. copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.

*4 . The power dissipation P_D is more useful in setting the upper dissipation limit for cases where additional heatsinking is used. It is used to determined the current rating, when this rating falls below the package limit.

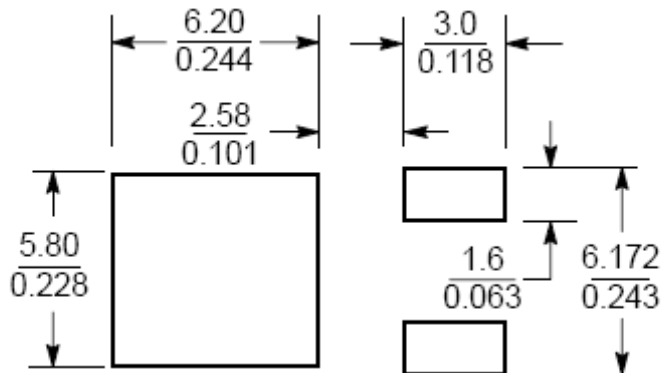
Characteristics (T_j=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	-30	-	-	V	V _{GS} =0V, I _D =-250μA
V _{GS(th)}	-1.0	-	-2.5		V _{DS} = V _{GS} , I _D =-250μA
G _{FS}	-	20	-	S	V _{DS} =-5V, I _D =-18A
I _{GSS}	-	-	±100	nA	V _{GS} =±20V, V _{DS} =0V
I _{DSS}	-	-	-1	μA	V _{DS} =-30V, V _{GS} =0V
I _{DSS}	-	-	-5		V _{DS} =-24V, V _{GS} =0V, T _j =55°C
*R _{DS(ON)}	-	21	30	mΩ	V _{GS} =-10V, I _D =-18A
*R _{DS(ON)}	-	33	45		V _{GS} =-4.5V, I _D =-10A
Dynamic					
*Q _g	-	20	-	nC	I _D =-18A, V _{DS} =-15V, V _{GS} =-10V
*Q _{gs}	-	3.3	-		
*Q _{gd}	-	4.6	-		

* $t_{d(ON)}$	-	7	-	ns	$V_{DS}=-15V, V_{GS}=-10V, R_G=3\Omega,$ $I_D=-18A$
* t_r	-	13.8	-		
* $t_{d(OFF)}$	-	61.6	-		
* t_f	-	41.2	-		
C_{iss}	-	984	-	pF	$V_{GS}=0V, V_{DS}=-15V, f=1MHz$
C_{oss}	-	116	-		
C_{rss}	-	102	-		
Source-Drain Diode					
* V_{SD}	-	-	-1	V	$I_S=-1A, V_{GS}=0V$
* I_S	-	-	-18	A	$V_D=V_G=0, V_S=-1V$
* t_{rr}	-	9.4	-	ns	$I_F=-18A, V_{GS}=0V, dI_F/dt=100A/\mu s$
* Q_{rr}	-	5.2	-	nC	

*Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

Recommended soldering footprint

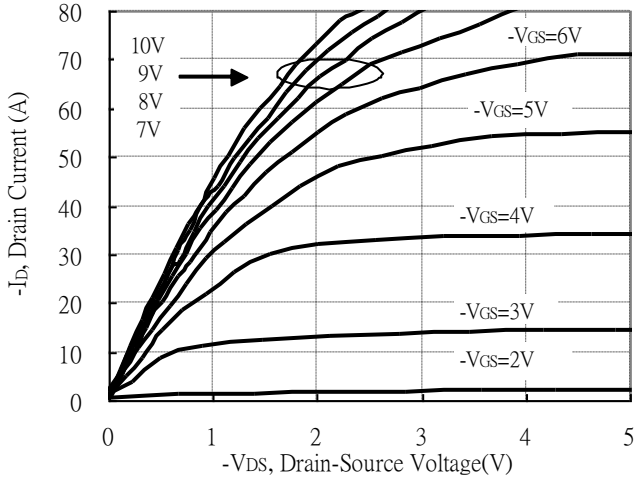


Unit ($\frac{mm}{inch}$)

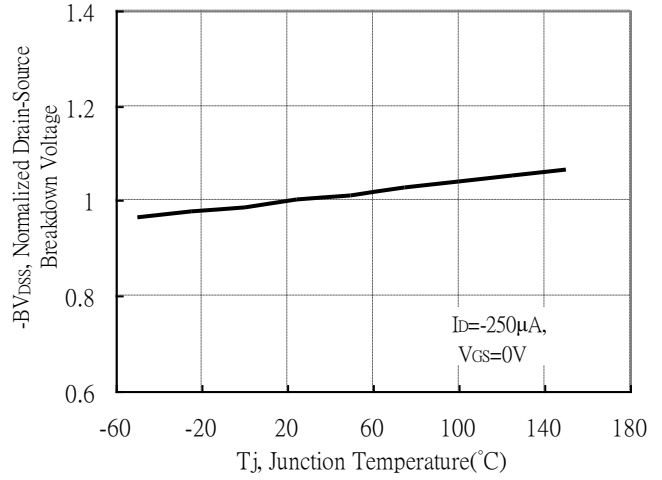


Typical Characteristics

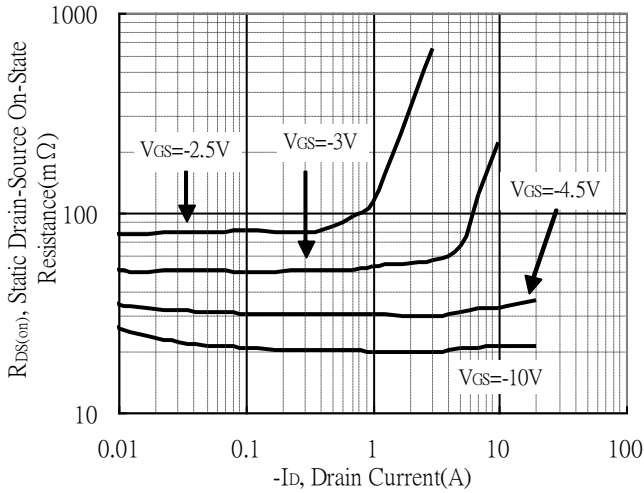
Typical Output Characteristics



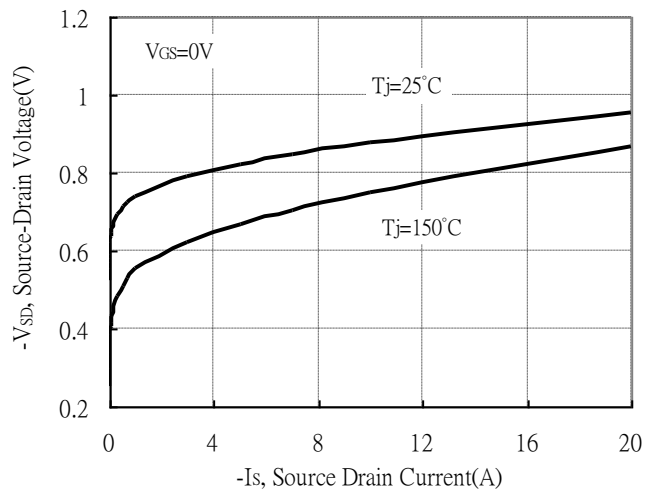
Normalized Brekdown Voltage vs Ambient Temperature



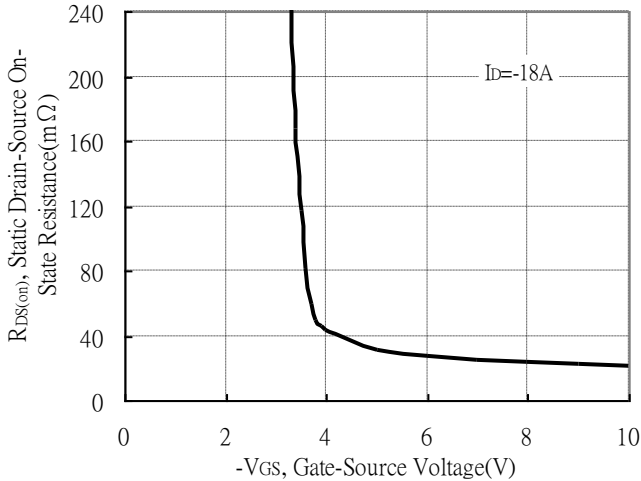
Static Drain-Source On-State resistance vs Drain Current



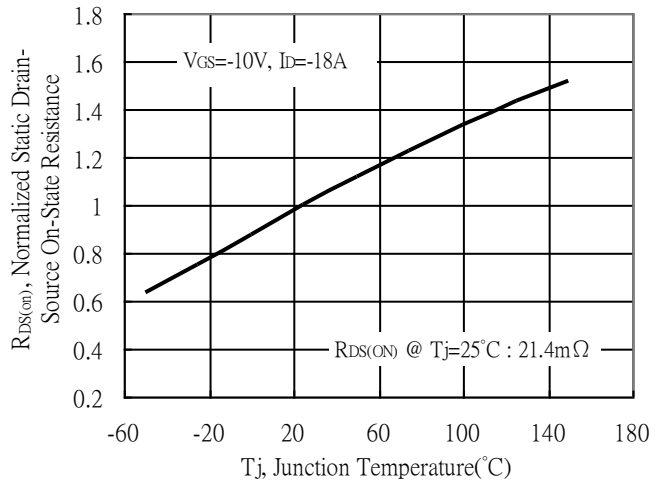
Source Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

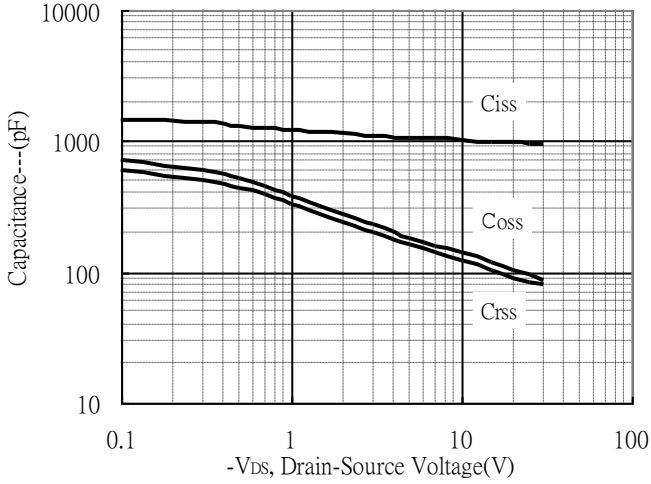


Normalized Drain-Source On-State Resistance vs Junction Temperature

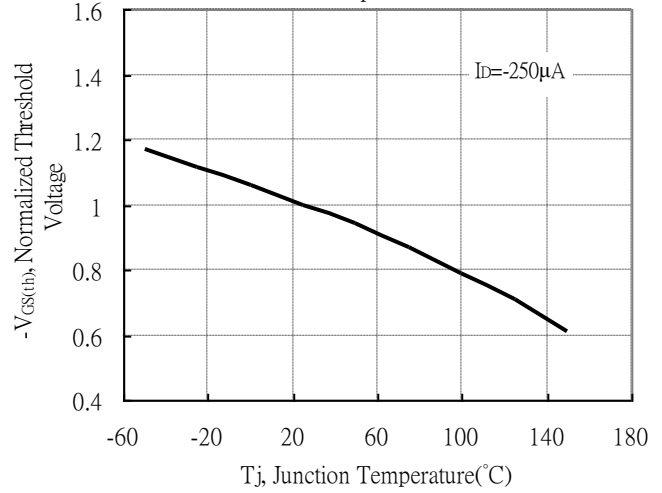


Typical Characteristics(Cont.)

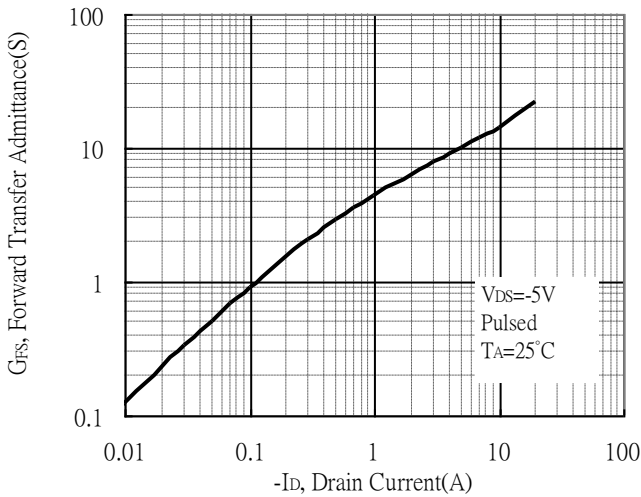
Capacitance vs Drain-to-Source Voltage



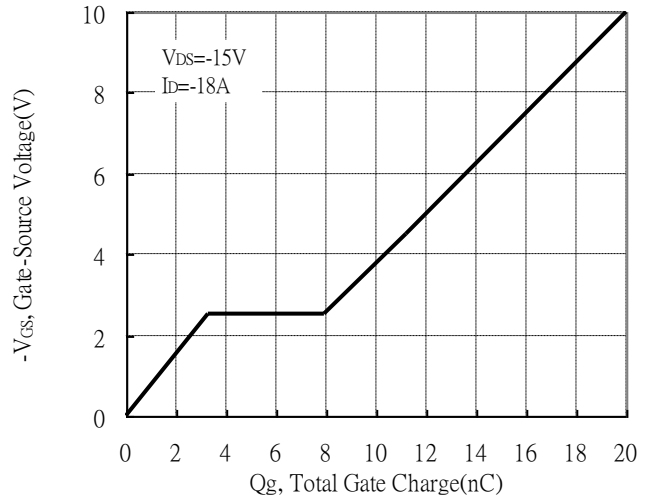
Normalized Threshold Voltage vs Junction Temperature



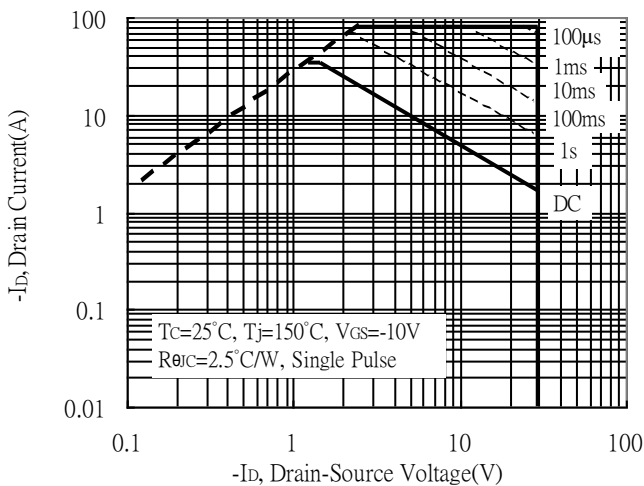
Forward Transfer Admittance vs Drain Current



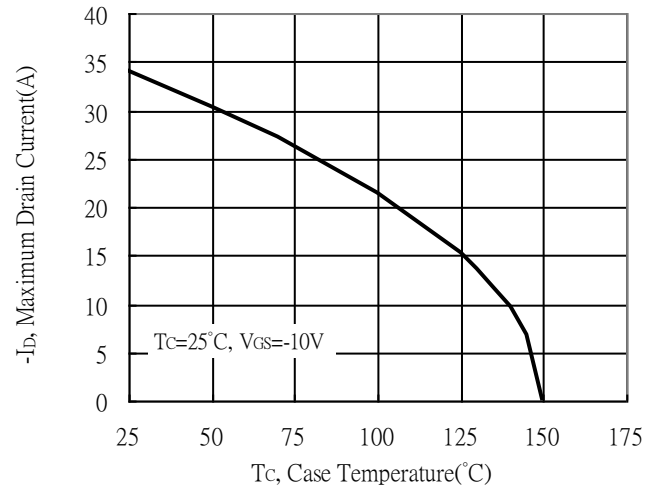
Gate Charge Characteristics



Maximum Safe Operating Area

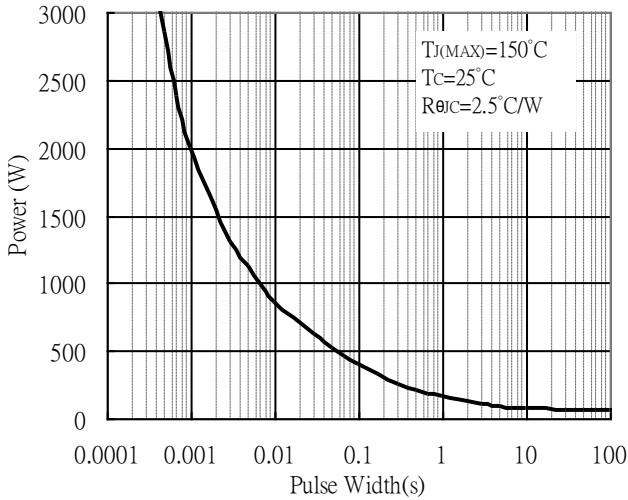


Maximum Drain Current vs Case Temperature

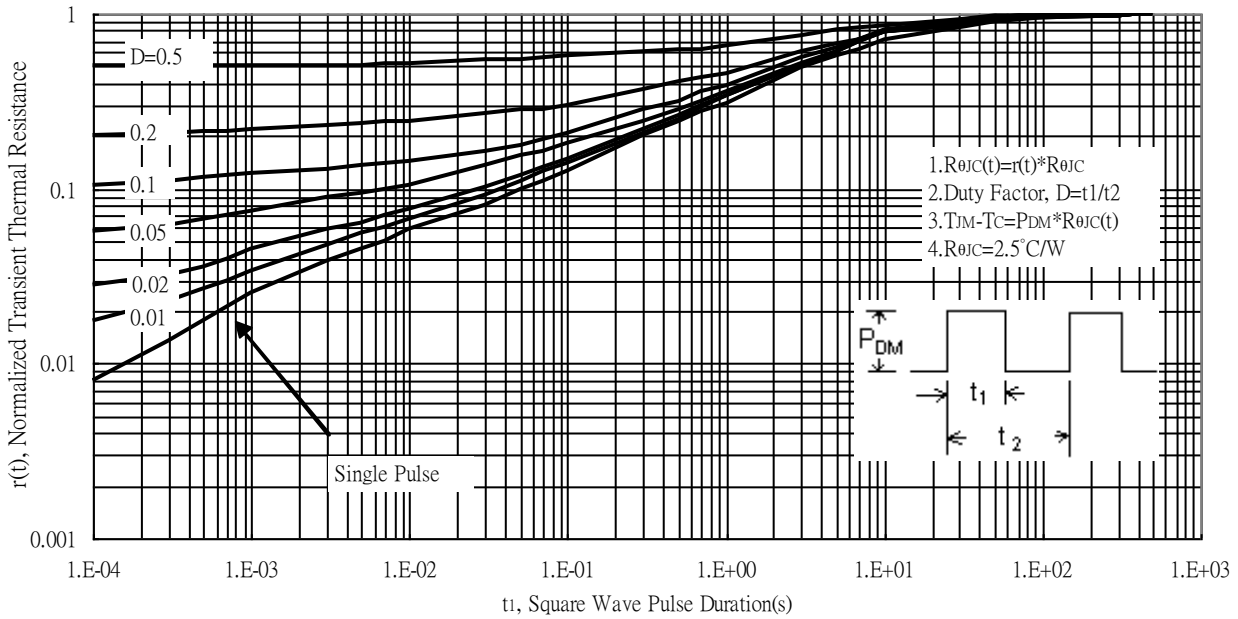


Typical Characteristics(Cont.)

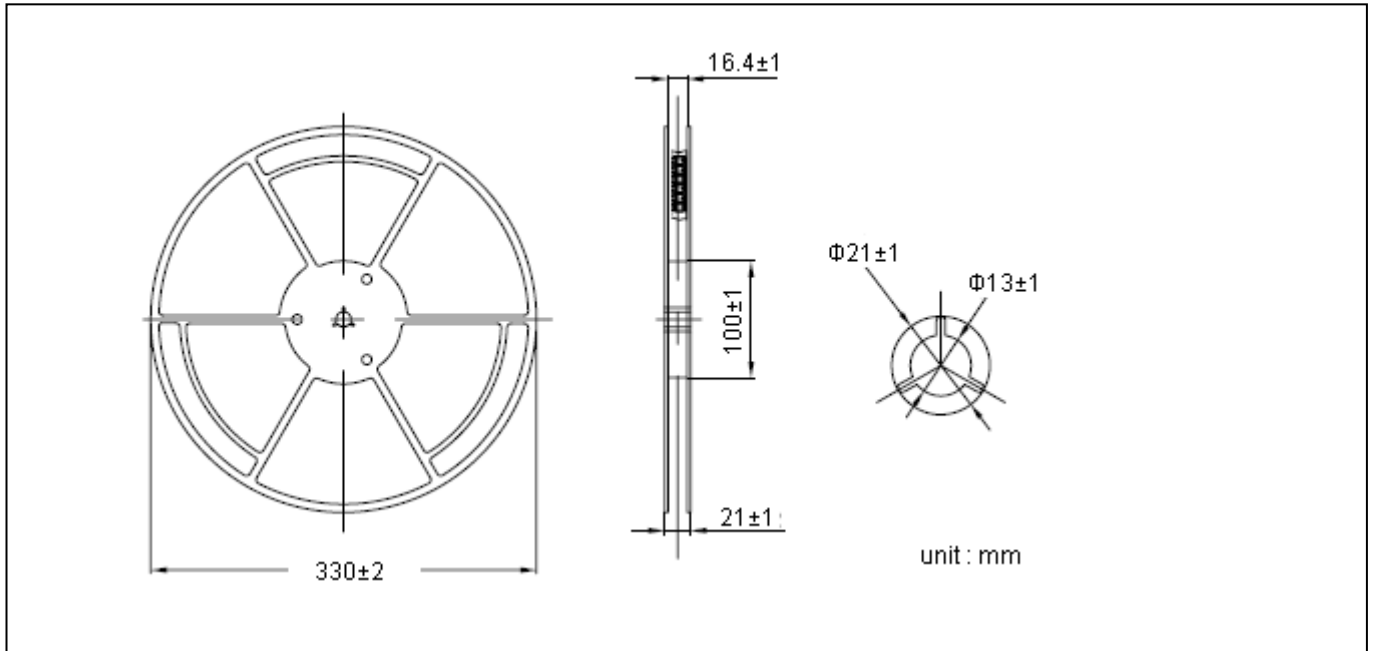
Single Pulse Power Rating, Junction to Case



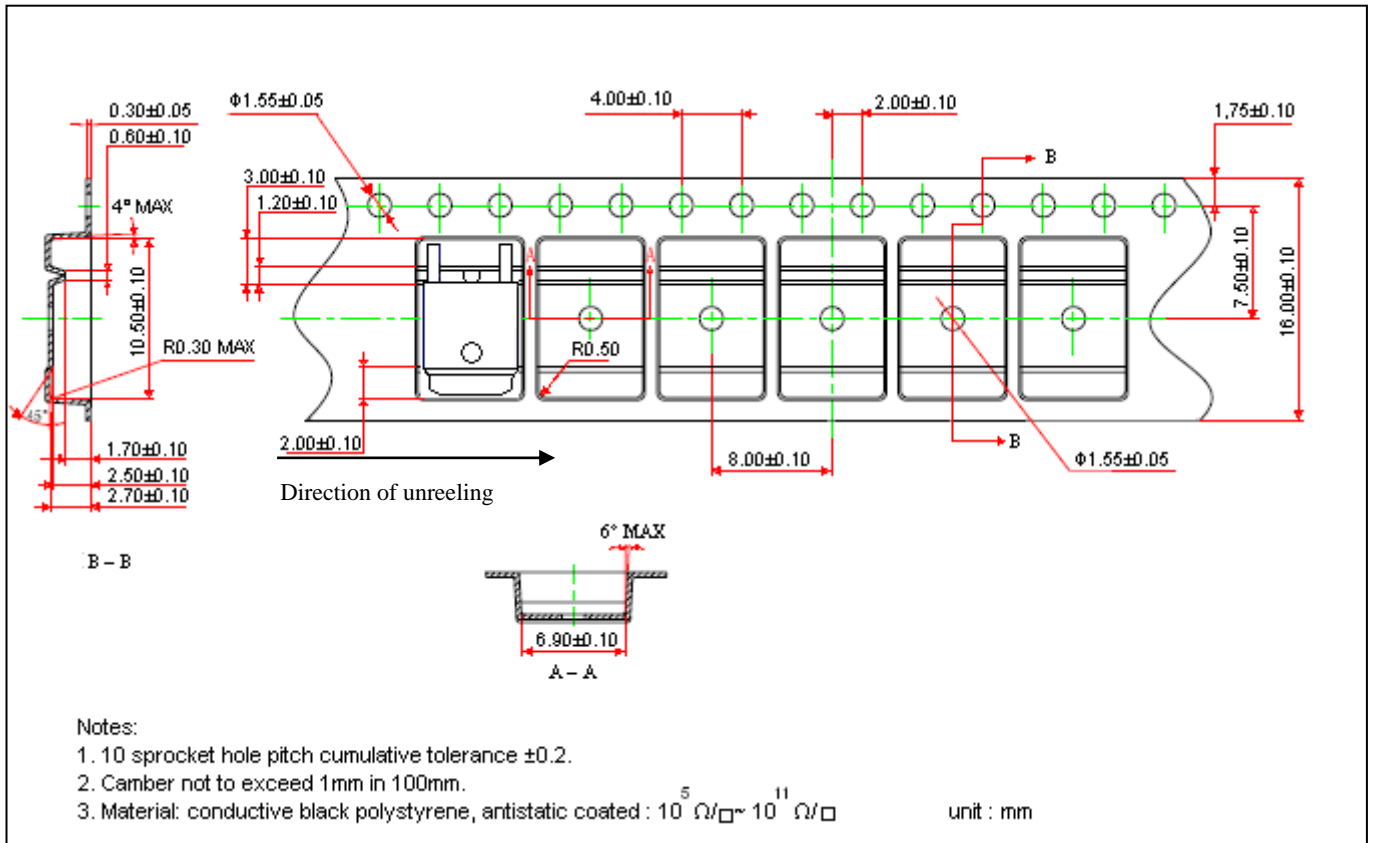
Transient Thermal Response Curves



Reel Dimension



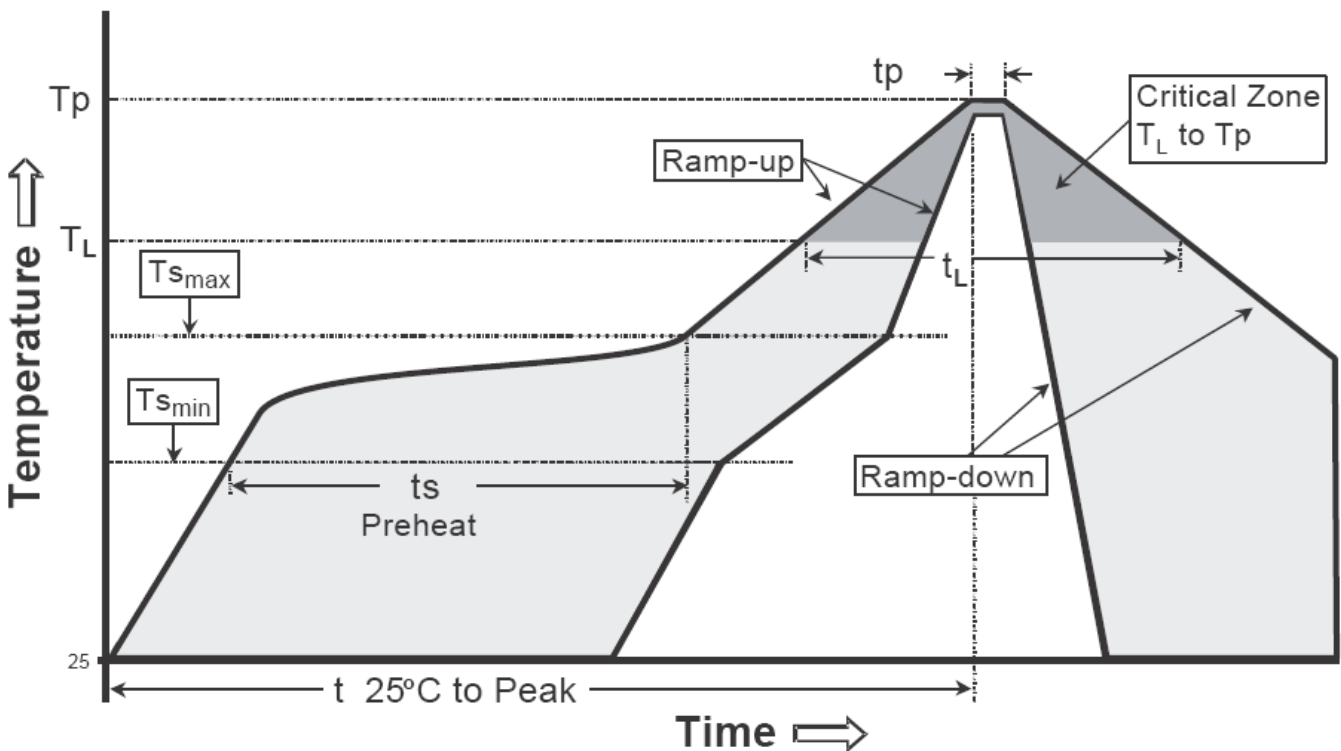
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

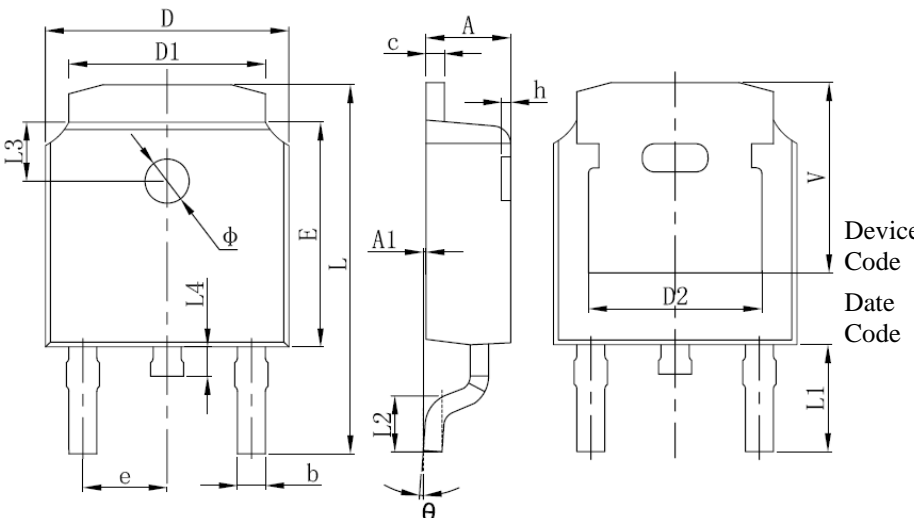
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-252 Dimension



3-Lead TO-252 Plastic Surface Mount Package
 CYStek Package Code: J3

Style: Pin 1.Gate 2.Drain 3.Source 4.Drain

Date Code :
 First Code : Last digit of Christian Year
 Second Code : Month Code : Jan→A, Feb→B, Mar→C, Apr→D, May→E, Jun→F, Jul→G,
 Aug→H, Sep→J, Oct→K, Nov→L, Dec→M
 Last Two Codes : Production Serial Code, 01~99

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.087	0.094	2.200	2.400	L	0.382	0.406	9.712	10.312
A1	0.000	0.005	0.000	0.127	L1	0.114	REF	2.900	REF
b	0.025	0.030	0.635	0.770	L2	0.055	0.067	1.400	1.700
c	0.018	0.023	0.460	0.580	L3	0.063	REF	1.600	REF
D	0.256	0.264	6.500	6.700	L4	0.024	0.039	0.600	1.000
D1	0.201	0.215	5.100	5.460	Φ	0.043	0.051	1.100	1.300
D2	0.190	REF	4.830	REF	θ	0°	8°	0°	8°
E	0.236	0.244	6.000	6.200	h	0.000	0.012	0.000	0.300
e	0.086	0.094	2.186	2.386	v	0.207	REF	5.250	REF

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead : Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.