

ESD protected N-CHANNEL MOSFET

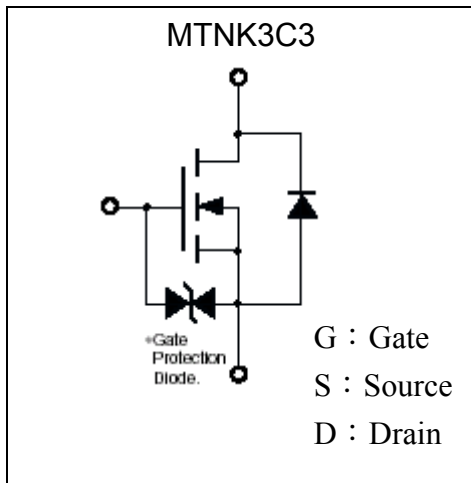
MTNK3C3

BV_{DSS}	20V
$I_D@V_{GS}=4.5V, T_A=25^\circ C$	100mA
$R_{DS(on)}@V_{GS}=4.5V, I_D=100mA$	3Ω (max)

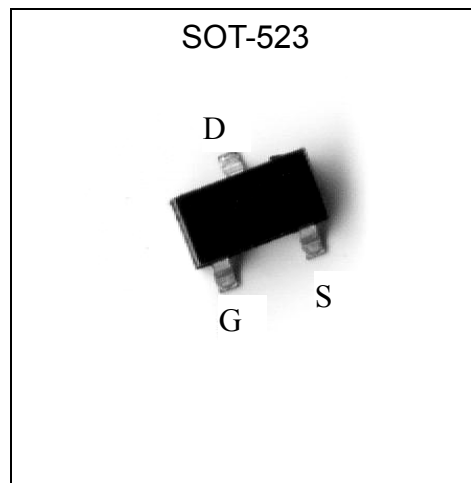
Description

- Low voltage drive, 1.8V.
- Easy to use in parallel.
- High speed switching.
- ESD protected device.
- Pb-free lead plating and halogen-free package.

Symbol

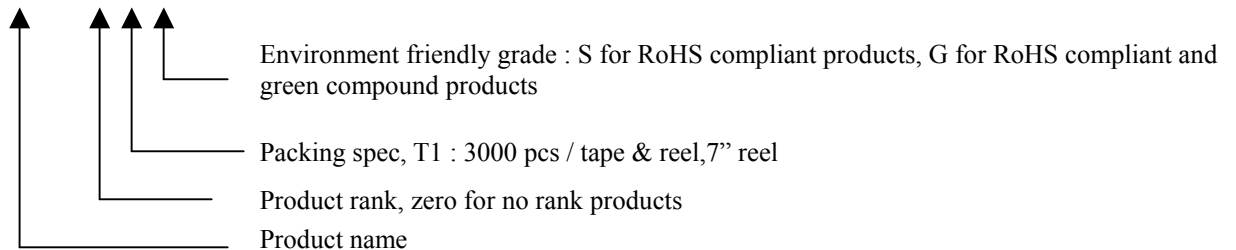


Outline



Ordering Information

Device	Package	Shipping
MTNK3C3-0-T1-G	SOT-523 (Pb-free lead plating and halogen-free package)	3000 pcs / tape & reel





Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	BV _{DSS}	20	V
Gate-Source Voltage	V _{GS}	±8	
Continuous Drain Current @V _{GS} =4.5V, T _A =25°C	I _D	100	mA
Pulsed Drain Current	I _{DM}	400 *1	
Total Power Dissipation	P _D	150 *2	mW
ESD susceptibility	V _{ESD}	350 *3	V
Operating Junction and Storage Temperature Range	T _j ; T _{stg}	-55~+150	°C
Thermal Resistance, Junction-to-Ambient	R _{th,ja}	833	°C/W

Note : *1. Pulse Width ≤ 300μs, Duty cycle ≤2%.
 *2. When device mounted on recommended land pattern.
 *3. Human body model, 1.5kΩ in series with 100pF.

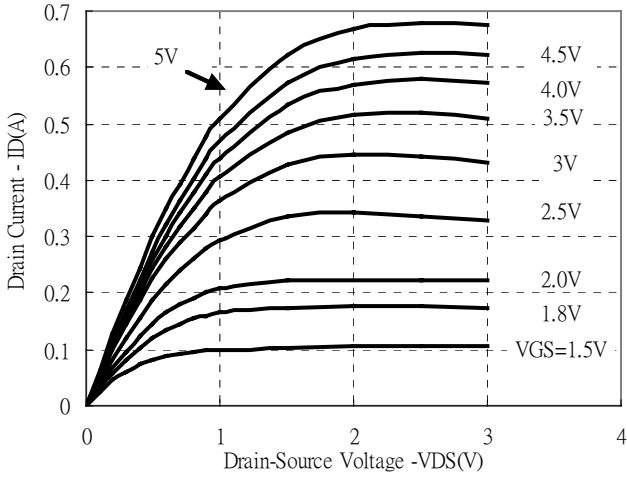
Electrical Characteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	20	-	-	V	V _{GS} =0V, I _D =100μA
V _{GS(th)}	0.5	-	1.0		V _{DS} =V _{GS} , I _D =250μA
I _{GSS}	-	-	±1	μA	V _{GS} =±8V, V _{DS} =0V
I _{DSS}	-	-	500	nA	V _{DS} =20V, V _{GS} =0V
R _{D(S)ON}	-	1.7	3	Ω	V _{GS} =4.5V, I _D =100mA
	-	3.5	6		V _{GS} =1.8V, I _D =20mA
G _{FS}	100	-	-	mS	V _{DS} =5V, I _D =100mA
Dynamic					
C _{iss}	-	23	50	pF	V _{DS} =10V, V _{GS} =0V, f=1MHz
C _{oss}	-	7.7	25		
C _{riss}	-	5.8	12		
Source-Drain Diode					
*V _{SD}	-	-	1	V	V _{GS} =0V, I _S =10mA

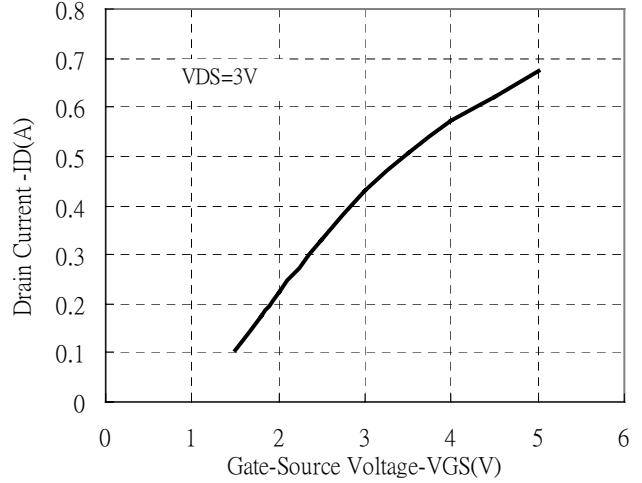
*Pulse Test : Pulse Width ≤300μs, Duty Cycle ≤2%

Typical Characteristics

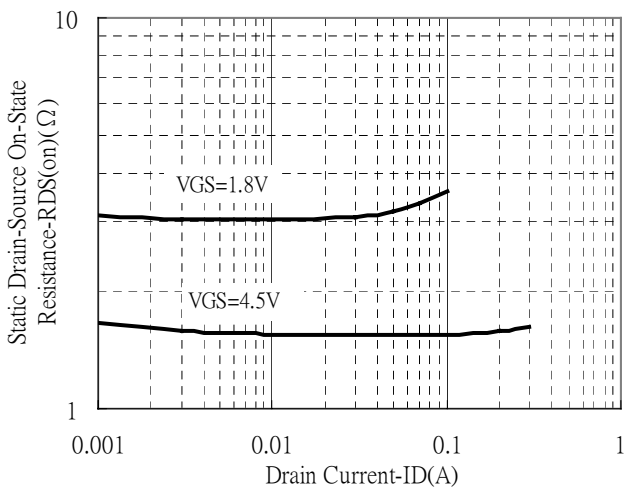
Typical Output Characteristics



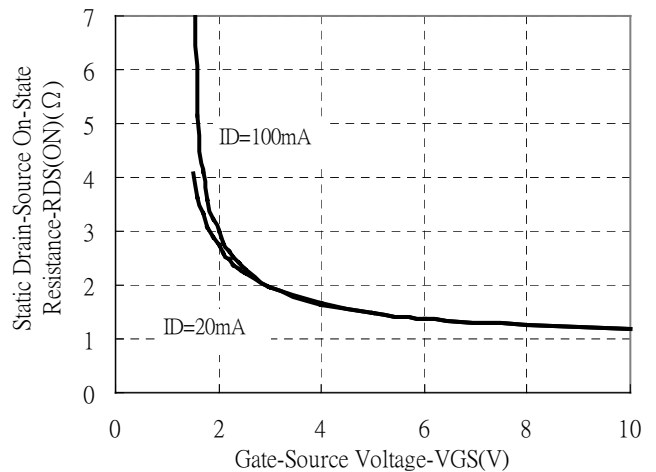
Typical Transfer Characteristics



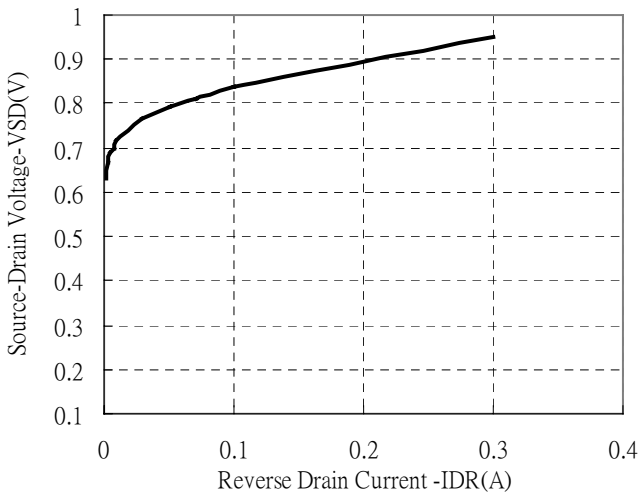
Static Drain-Source On-State resistance vs Drain Current



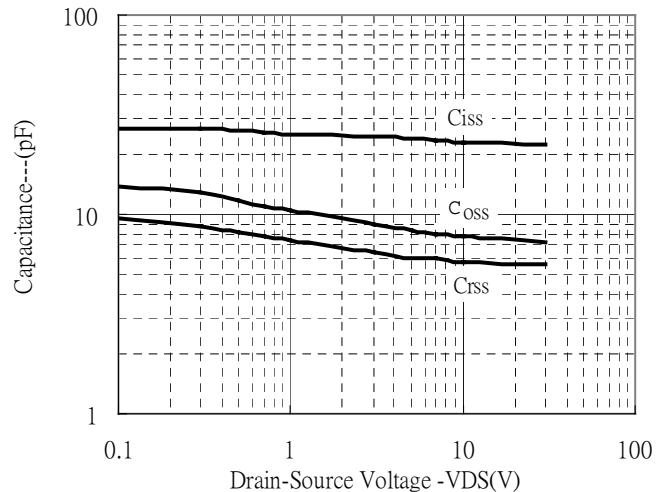
Static Drain-Source On-State Resistance vs Gate-Source Voltage



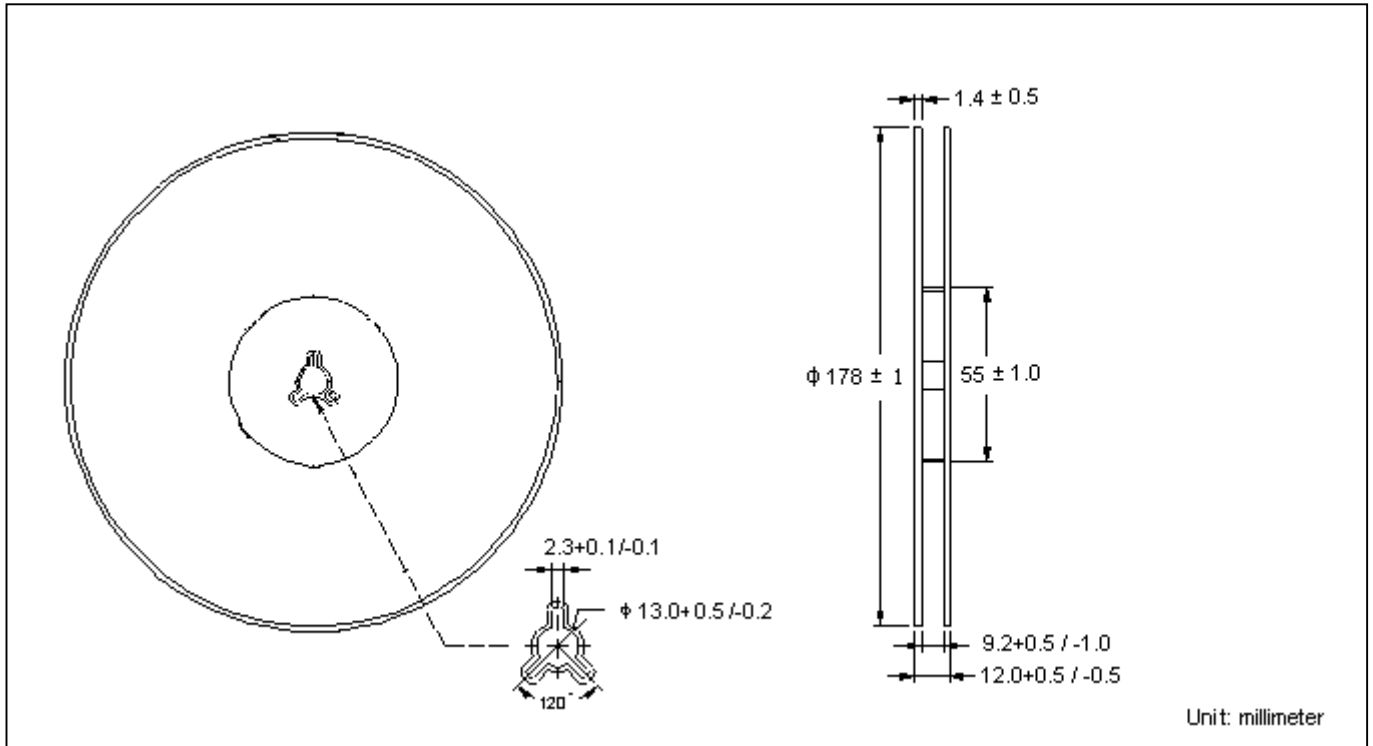
Reverse Drain Current vs Source-Drain Voltage



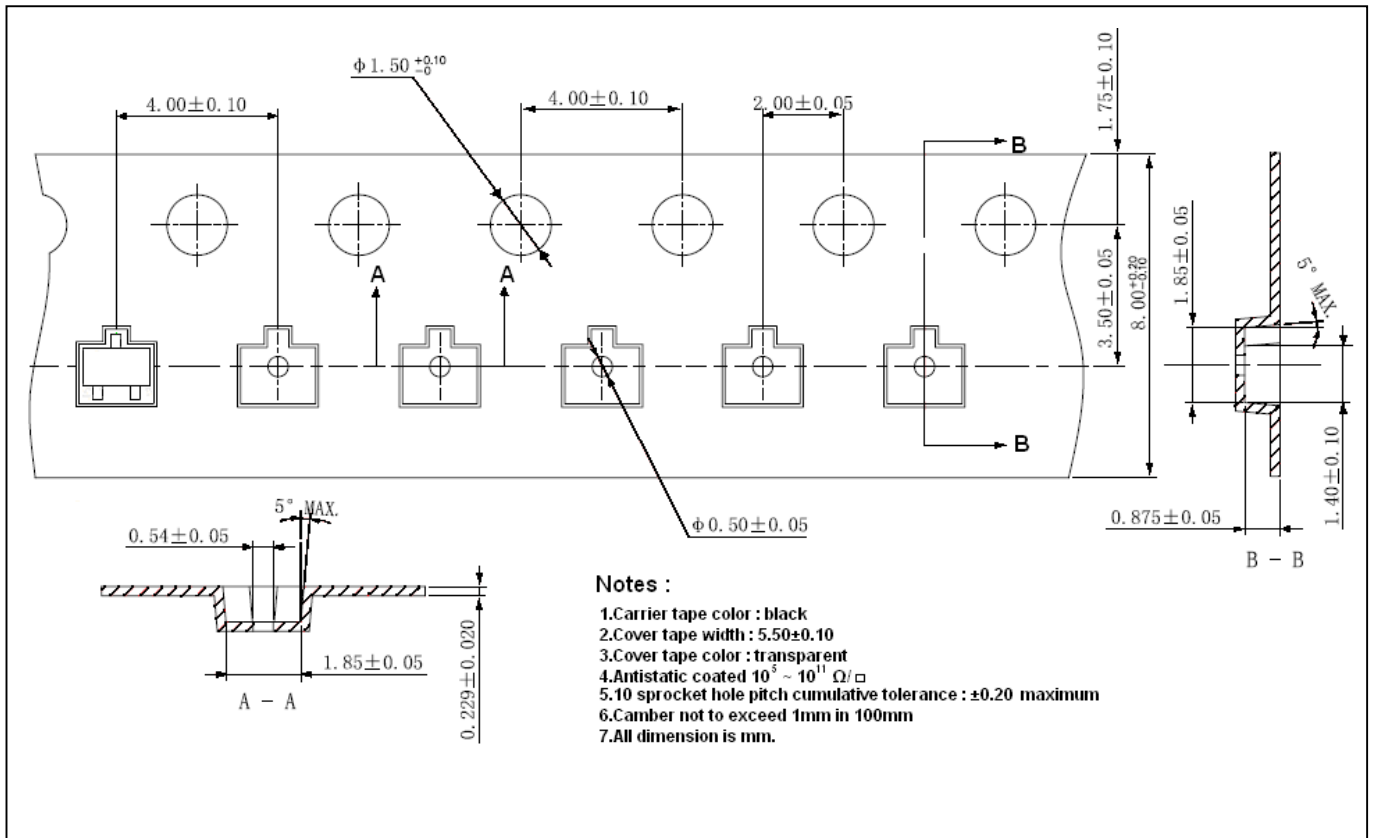
Capacitance vs Drain-to-Source Voltage



Reel Dimension



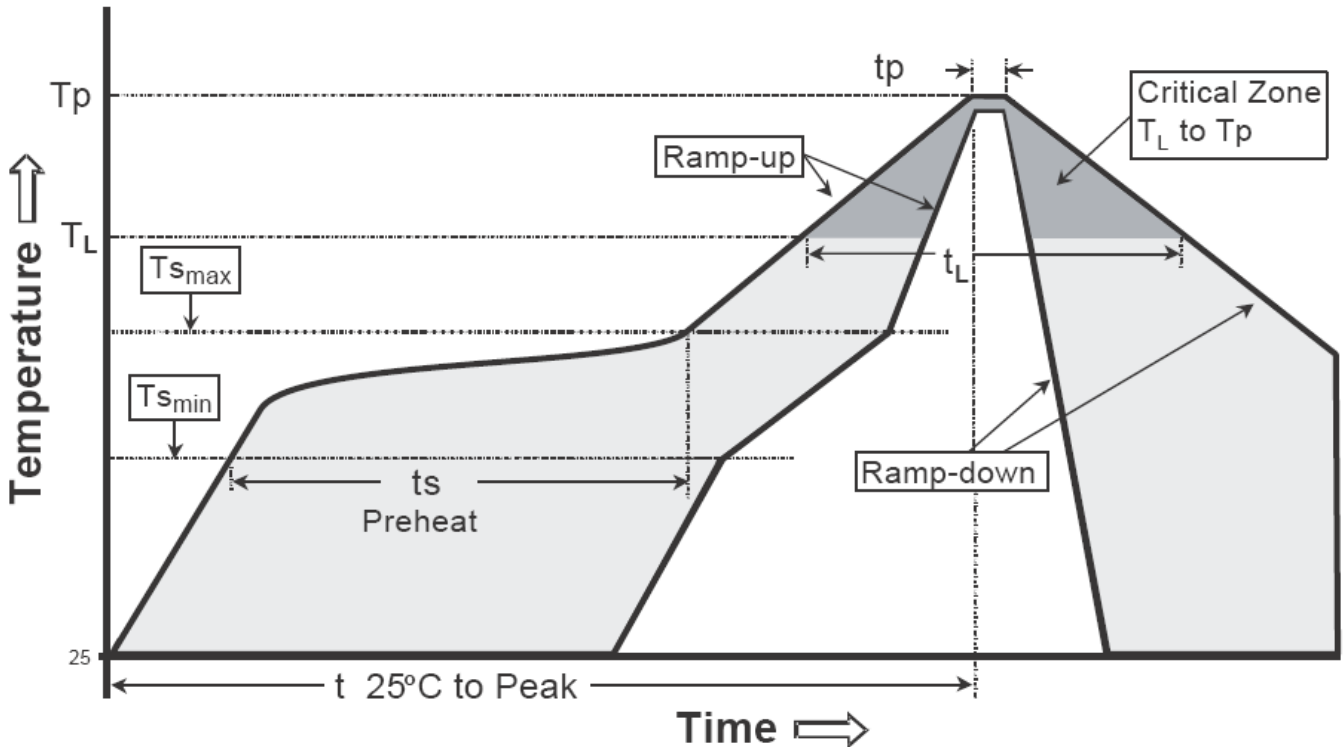
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

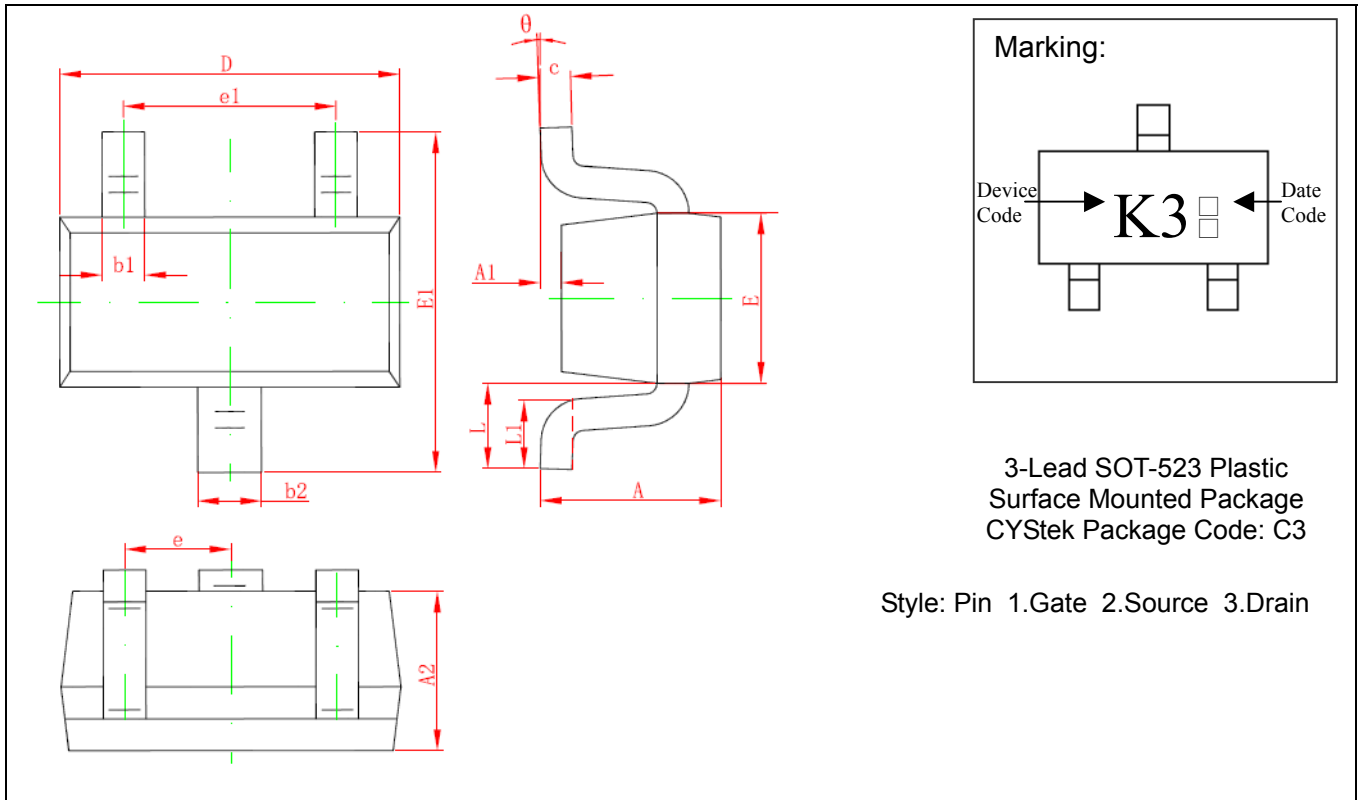
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (Tl)	183°C	217°C
- Time (tl)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-523 Dimension



DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.700	0.900	0.028	0.035	E	0.700	0.900	0.028	0.035
A1	0.000	0.100	0.000	0.004	E1	1.450	1.750	0.057	0.069
A2	0.700	0.800	0.028	0.031	e	0.500	TYP	0.020	TYP
b1	0.150	0.250	0.006	0.010	e1	0.900	1.100	0.035	0.043
b2	0.250	0.350	0.010	0.014	L	0.400	REF	0.016	REF
c	0.100	0.200	0.004	0.008	L1	0.260	0.460	0.010	0.018
D	1.500	1.700	0.059	0.067	θ	0°	8°	0°	8°

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

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