



N-Channel Enhancement Mode Power MOSFET

MTN9N50BFP

BV_{DSS}	500V
I_D @ V_{GS}=10V, T_C=25°C	8.5A
I_D @ V_{GS}=10V, T_C=100°C	5.4A
R_{DS(ON)}@ V_{GS}=10V, I_D=4.5A	0.63 Ω (typ)

Description

The MTN9N50BFP is a N-channel enhancement-mode MOSFET, providing the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness. The TO-220 package is universally preferred for all commercial-industrial applications

Features

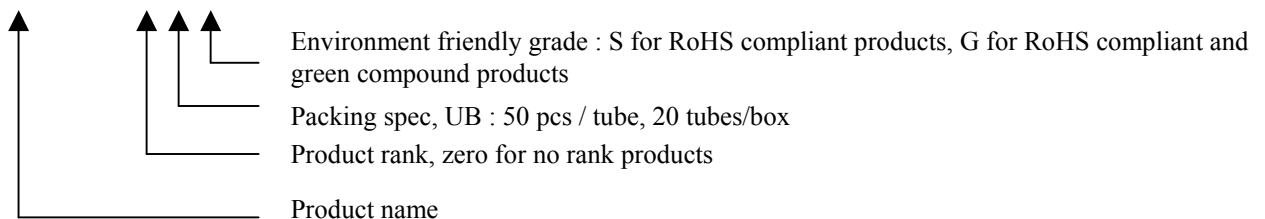
- Low On Resistance
- Simple Drive Requirement
- Low Gate Charge
- Fast Switching Characteristic
- Insulating package, front/back side insulating voltage=2500V(AC)
- RoHS compliant package

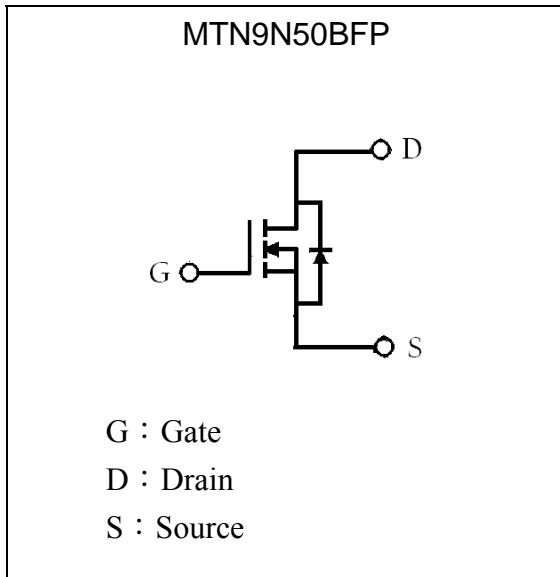
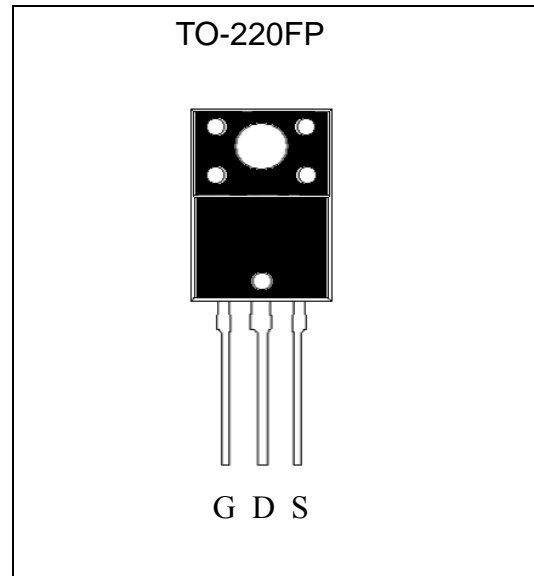
Applications

- Ballast
- Inverter

Ordering Information

Device	Package	Shipping
MTN9N50BFP-0-UB-S	TO-220FP (RoHS compliant package)	50 pcs/tube, 20 tubes/box, 4 boxes / carton



Symbol

Outline

Absolute Maximum Ratings (T_C=25°C)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage (Note 1)	V _{DS}	500	V
Gate-Source Voltage	V _{GS}	±30	
Continuous Drain Current @T _C =25°C, V _{GS} =10V	I _D	8.5*	A
Continuous Drain Current @T _C =100°C, V _{GS} =10V		5.4*	
Pulsed Drain Current @ V _{GS} =10V (Note 2)	I _{DM}	34*	
Single Pulse Avalanche Energy (Note 3)	E _{AS}	290	mJ
Avalanche Current (Note 2)	I _{AR}	8	A
Repetitive Avalanche Energy (Note 2)	E _{AR}	12.5	mJ
Maximum Temperature for Soldering @ Lead at 0.125 in(3.175mm) from case for 10 seconds	T _L	300	°C
Total Power Dissipation (T _C =25°C)	P _D	38.5	W
Linear Derating Factor above 25°C		0.3	W/°C
Operating Junction and Storage Temperature	T _J , T _{stg}	-55~+150	°C

*Drain current limited by maximum junction temperature

- Note : 1. T_J=+25°C to +150°C.
 2. Repetitive rating; pulse width limited by maximum junction temperature.
 3. I_{AS}=8A, V_{DD}=50V, L=5mH, R_G=25Ω, starting T_J=+25°C.



Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{th,j-c}$	3.25	°C/W
Thermal Resistance, Junction-to-ambient, max	$R_{th,j-a}$	62.5	°C/W

Characteristics (Tj=25°C, unless otherwise specified)

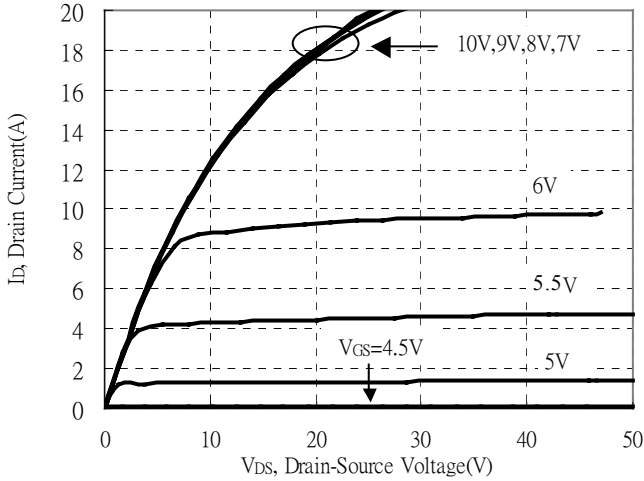
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV_{DSS}	500	-	-	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta BV_{DSS}/\Delta T_j$	-	0.6	-	V/°C	Reference to 25°C, $I_D=250\mu A$
$V_{GS(th)}$	2.0	-	4.0	V	$V_{DS} = V_{GS}, I_D=250\mu A$
* G_{FS}	-	8	-	S	$V_{DS} = 15V, I_D=4A$
I_{GSS}	-	-	±100	nA	$V_{GS}=\pm 30V$
I_{DSS}	-	-	1	μA	$V_{DS} = 500V, V_{GS} = 0V$
	-	-	25		$V_{DS} = 400V, V_{GS} = 0V, T_j=125^\circ C$
* $R_{DS(ON)}$	-	0.63	0.85	Ω	$V_{GS} = 10V, I_D=4.5A$
Dynamic					
* Q_g	-	26.8	-	nC	$I_D=8A, V_{DD}=250V, V_{GS}=10V$
* Q_{gs}	-	5.6	-		
* Q_{gd}	-	11	-		
* $t_{d(ON)}$	-	14.4	-	ns	$V_{DD}=250V, I_D=8A, V_{GS}=10V, R_G=10\Omega$
* t_r	-	11.8	-		
* $t_{d(OFF)}$	-	52.2	-		
* t_f	-	14.2	-		
C_{iss}	-	890	-	pF	$V_{GS}=0V, V_{DS}=25V, f=1MHz$
C_{oss}	-	103	-		
C_{rss}	-	45	-		
Source-Drain Diode					
* I_S	-	-	8	A	$V_D=V_G=0, V_S=1.3V$
* I_{SM}	-	-	32		
* V_{SD}	-	0.8	1.2	V	$I_S=4.5A, V_{GS}=0V$
* t_{rr}	-	350	-	ns	$V_{GS}=0, I_F=8A, dI_F/dt=100A/\mu s$
* Q_{rr}	-	2.1	-	μC	

*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

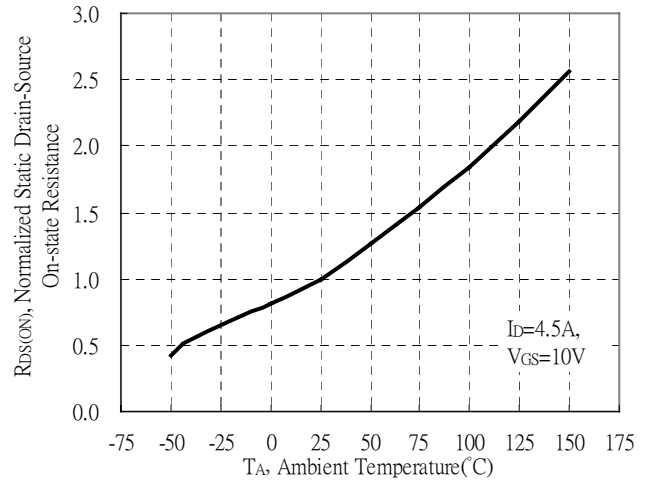


Typical Characteristics

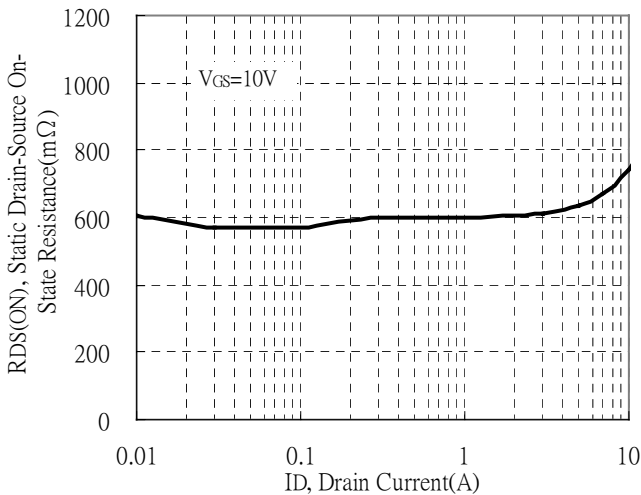
Typical Output Characteristics



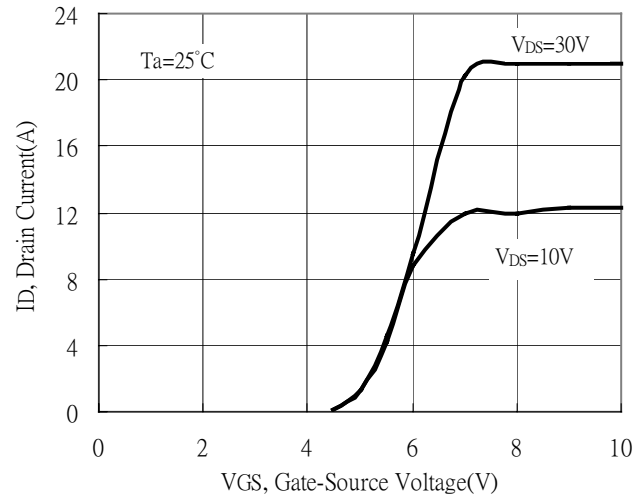
Static Drain-Source On-resistance vs Ambient Temperature



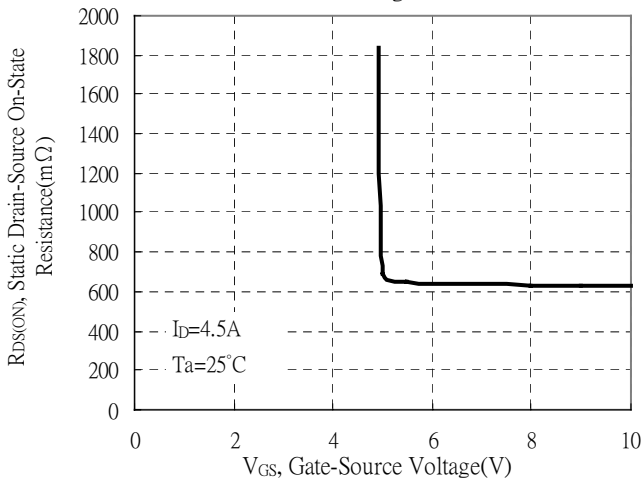
Static Drain-Source On-State resistance vs Drain Current



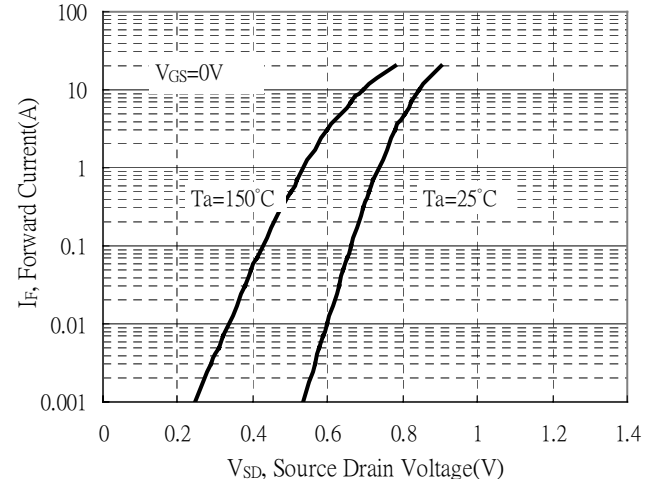
Drain Current vs Gate-Source Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage



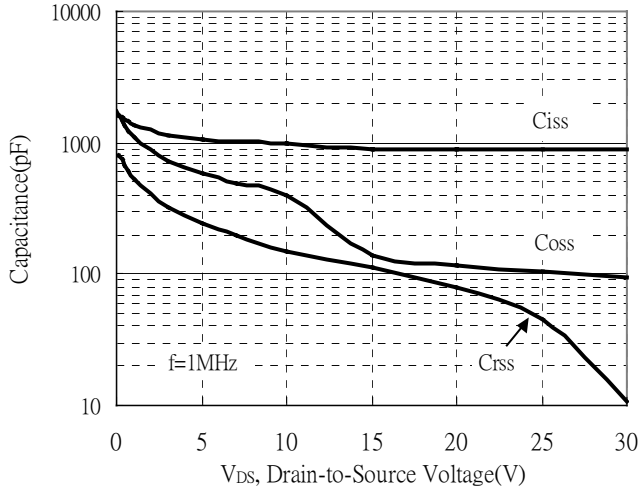
Forward Drain Current vs Source-Drain Voltage



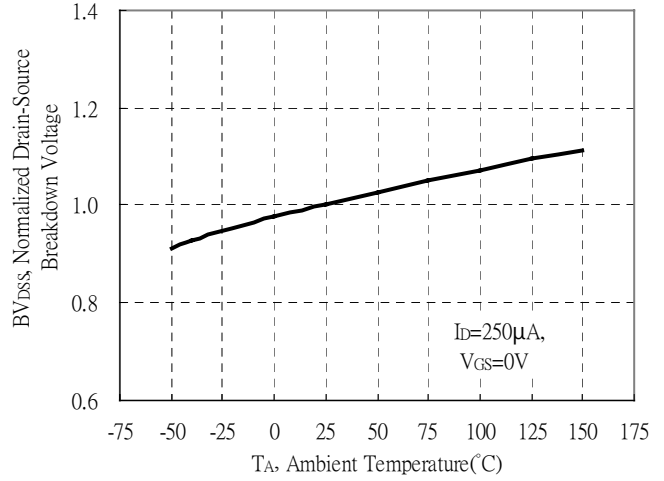


Typical Characteristics(cont.)

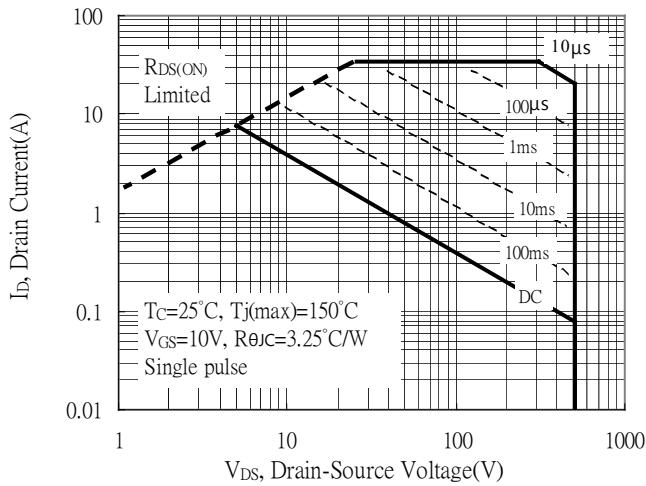
Capacitance vs Reverse Voltage



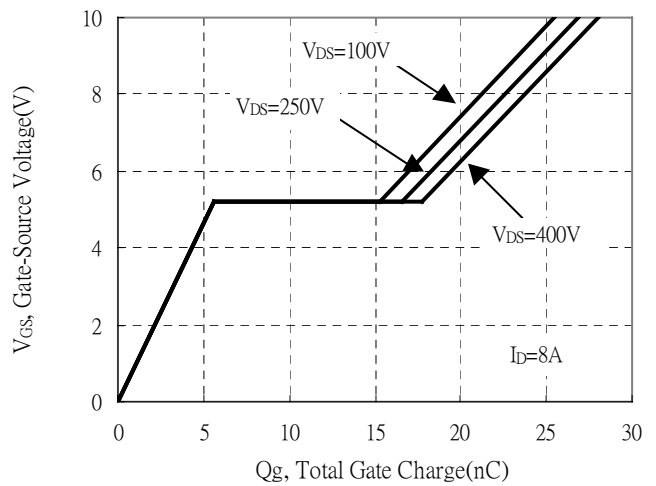
Brekdown Voltage vs Ambient Temperature



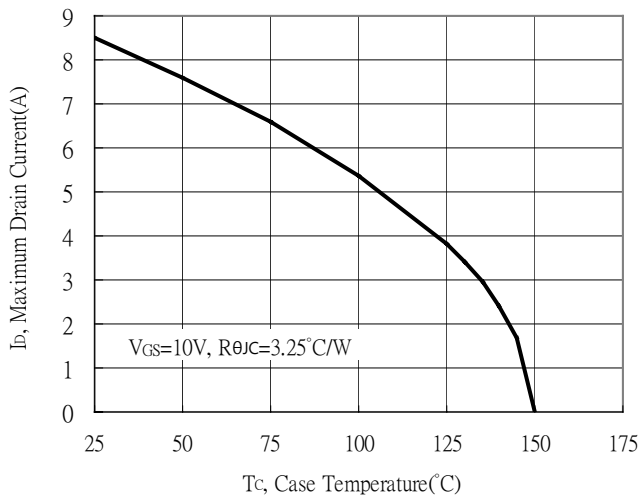
Maximum Safe Operating Area



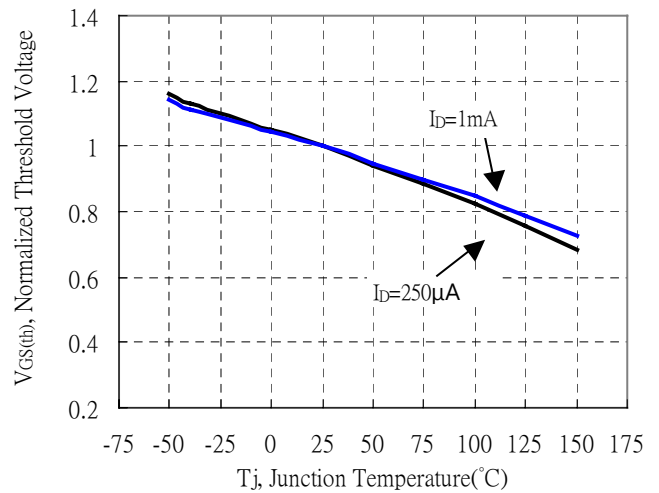
Gate Charge Characteristics



Maximum Drain Current vs Case Temperature



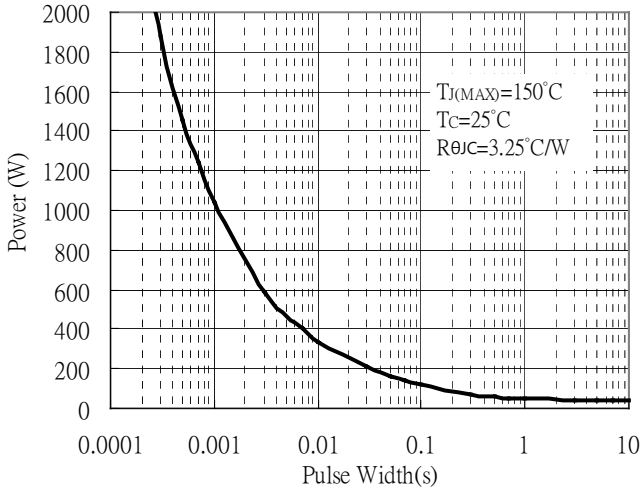
Threshold Voltage vs Junction Temperature



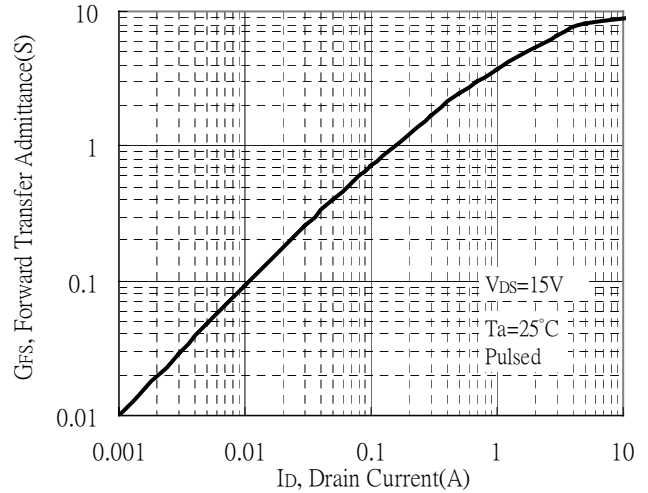


Typical Characteristics(Cont.)

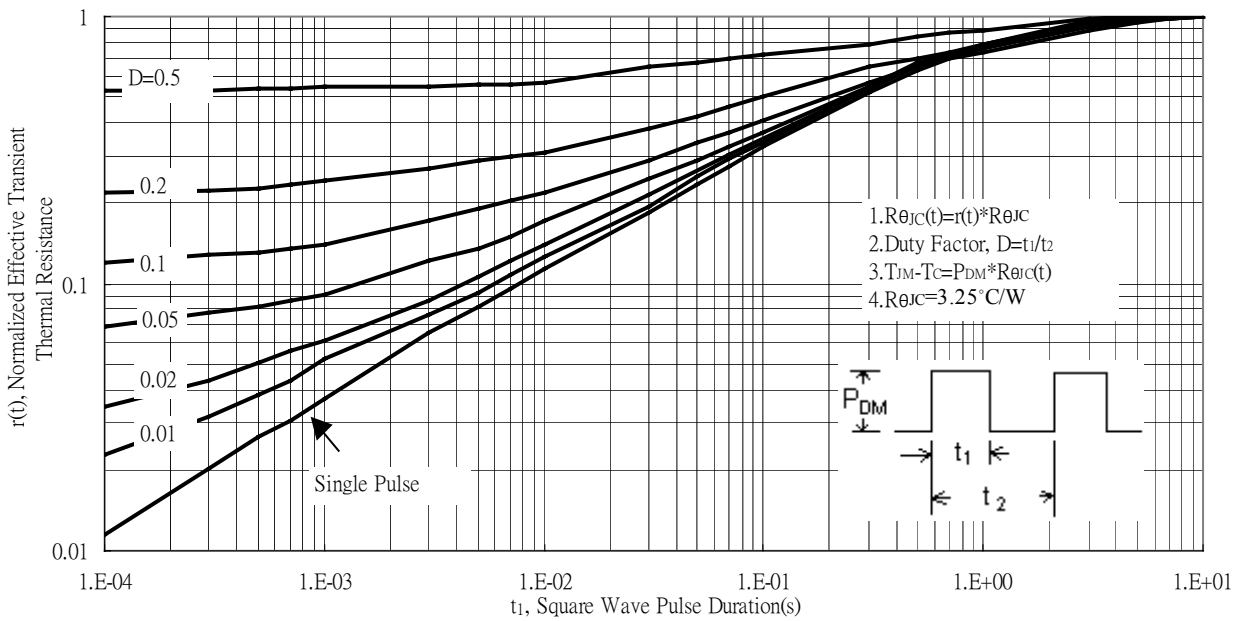
Single Pulse Power Rating, Junction to Case



Forward Transfer Admittance vs Drain Current



Transient Thermal Response Curves



Test Circuit and Waveforms

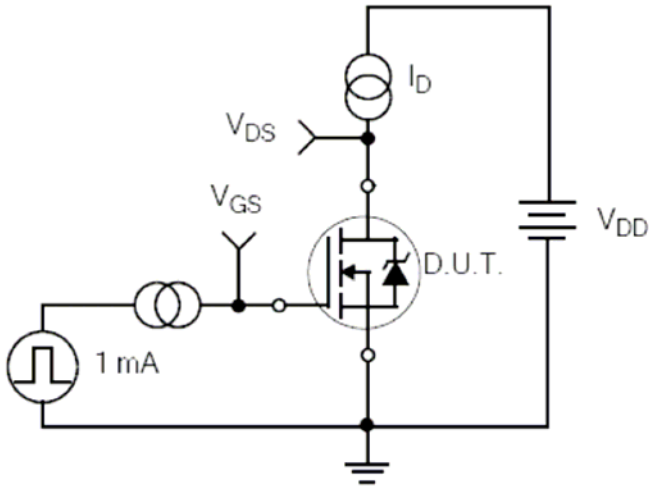


Figure 12. Gate Charge Test Circuit

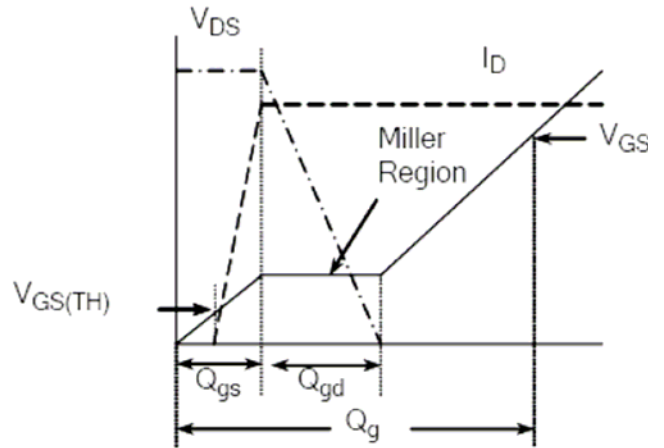


Figure 13. Gate Charge Waveform

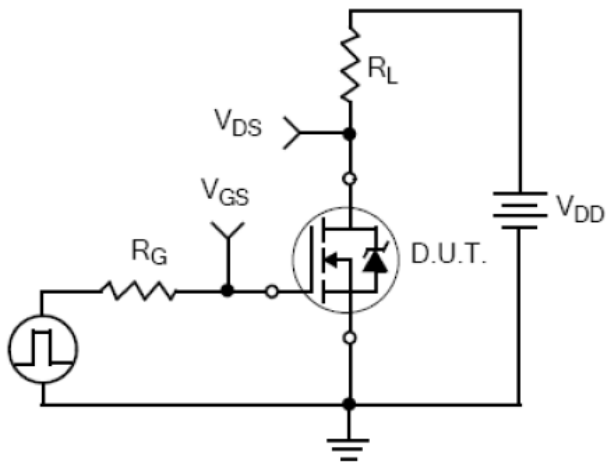


Figure 14. Resistive Switching Test Circuit

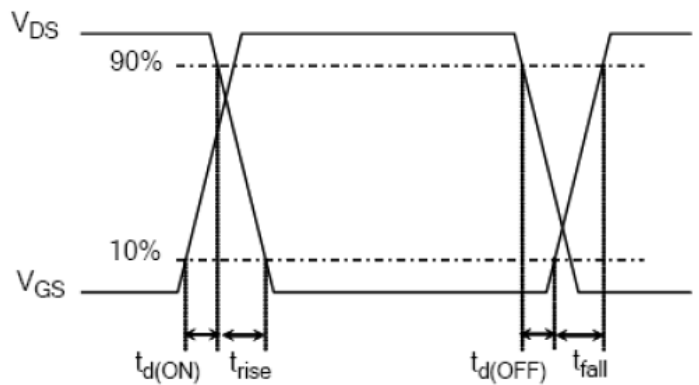


Figure 15. Resistive Switching Waveforms

Test Circuit and Waveforms(Cont.)

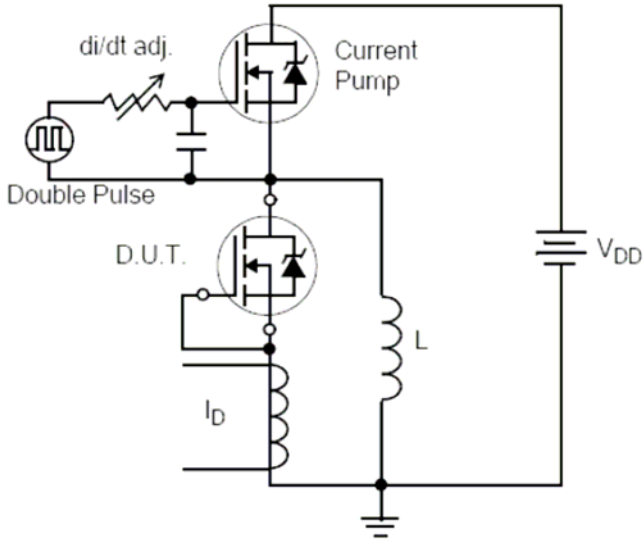


Figure 16. Diode Reverse Recovery Test Circuit

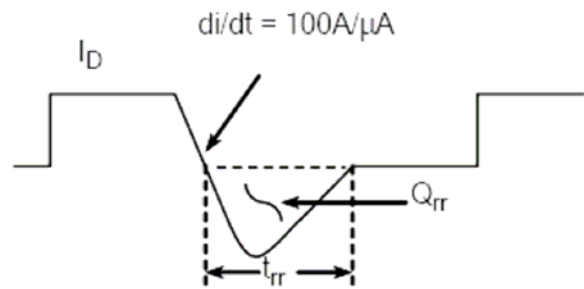


Figure 17. Diode Reverse Recovery Waveform

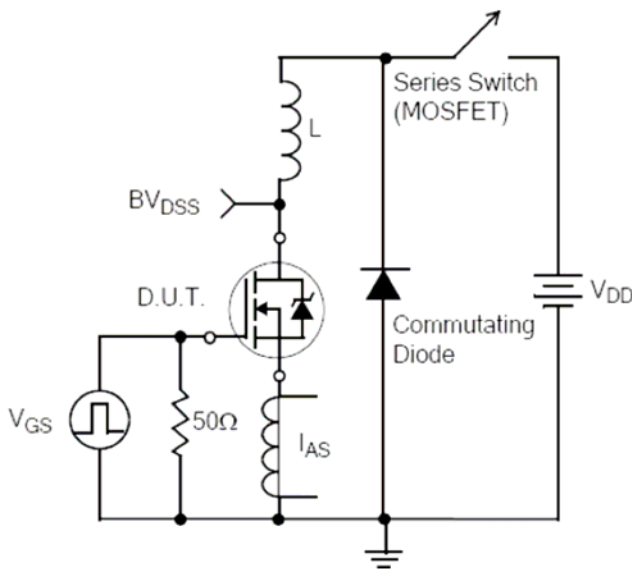


Figure 18. Unclamped Inductive Switching Test Circuit

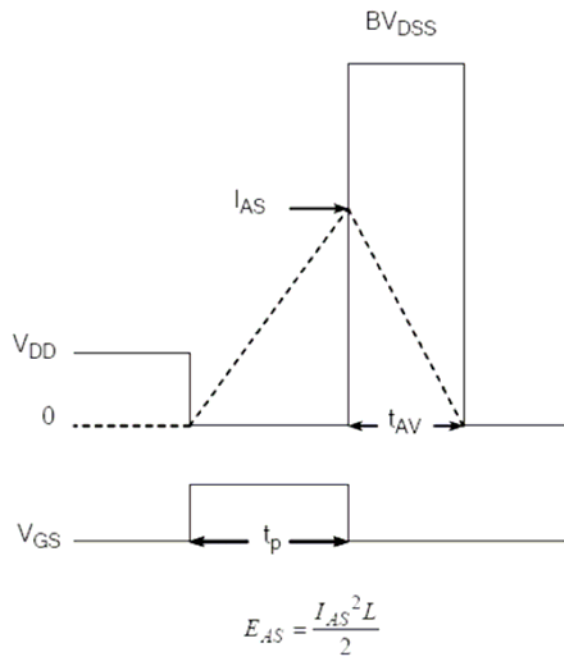
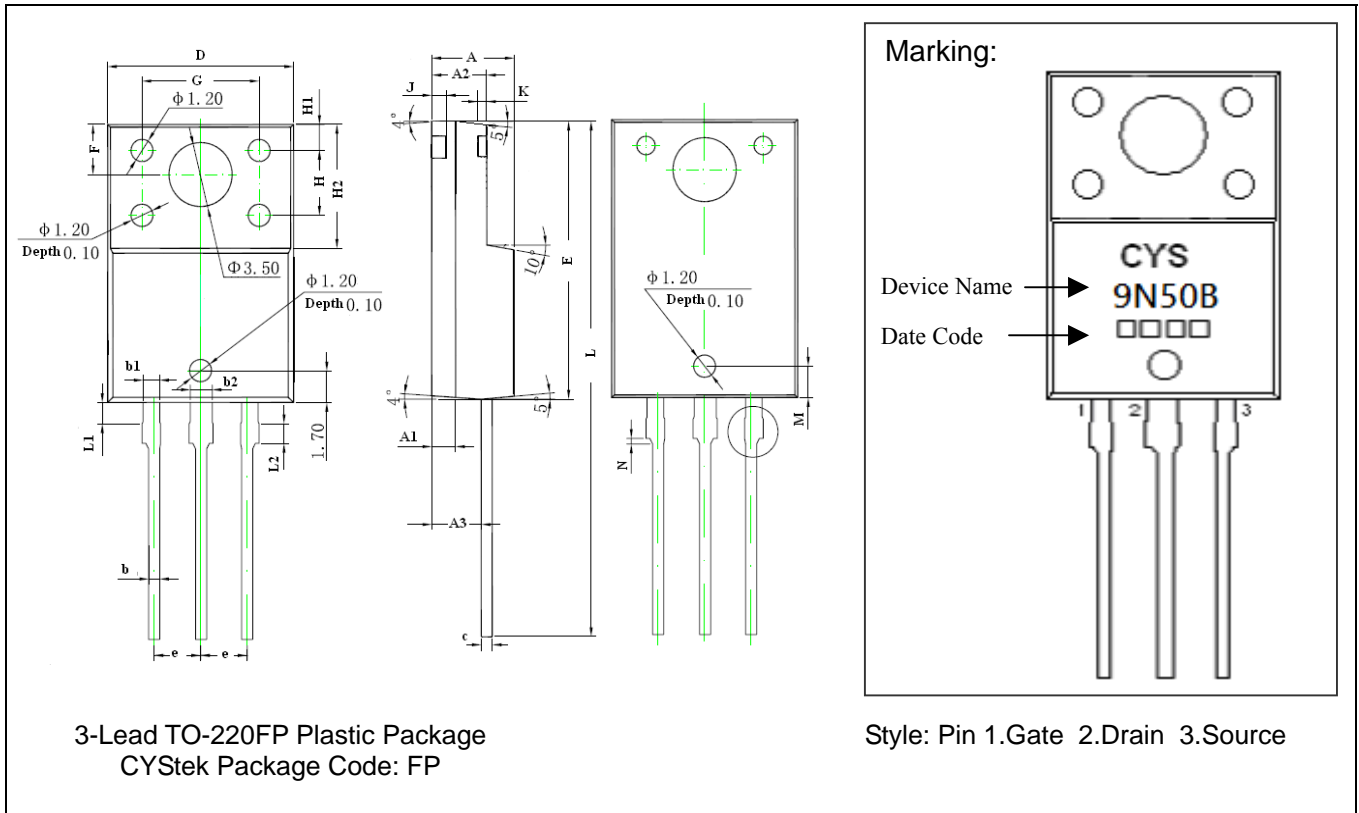


Figure 19. Unclamped Inductive Switching Waveforms

TO-220FP Dimension



3-Lead TO-220FP Plastic Package
 CYStek Package Code: FP

Marking:
 Device Name → CYS 9N50B
 Date Code → □□□□

Style: Pin 1.Gate 2.Drain 3.Source

*Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.171	0.183	4.35	4.65	G	0.246	0.258	6.25	6.55
A1	0.051 REF		1.300 REF		H	0.138 REF		3.50 REF	
A2	0.112	0.124	2.85	3.15	H1	0.055 REF		1.40 REF	
A3	0.102	0.110	2.60	2.80	H2	0.256	0.272	6.50	6.90
b	0.020	0.030	0.50	0.75	J	0.031 REF		0.80 REF	
b1	0.031	0.041	0.80	1.05	K	0.020		0.50 REF	
b2	0.047 REF		1.20 REF		L	1.102	1.118	28.00	28.40
c	0.020	0.030	0.500	0.750	L1	0.043	0.051	1.10	1.30
D	0.396	0.404	10.06	10.26	L2	0.036	0.043	0.92	1.08
E	0.583	0.598	14.80	15.20	M	0.067 REF		1.70 REF	
e	0.100 *		2.54*		N	0.012 REF		0.30 REF	
F	0.106 REF		2.70 REF						

- Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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