

N -Channel Logic Level Enhancement Mode Power MOSFET

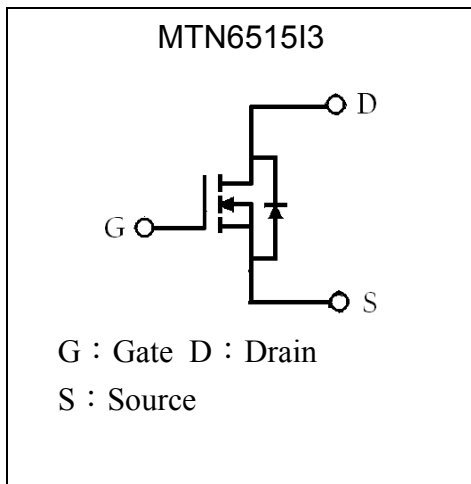
MTN6515I3

BV_{DSS}	150V
I_D@V_{GS}=10V, T_C=25°C	20A
R_{DS(ON)}@V_{GS}=10V, I_D=15A	60mΩ (typ)
R_{DS(ON)}@V_{GS}=5V, I_D=10A	59mΩ (typ)
R_{DS(ON)}@V_{GS}=3V, I_D=3A	60mΩ (typ)

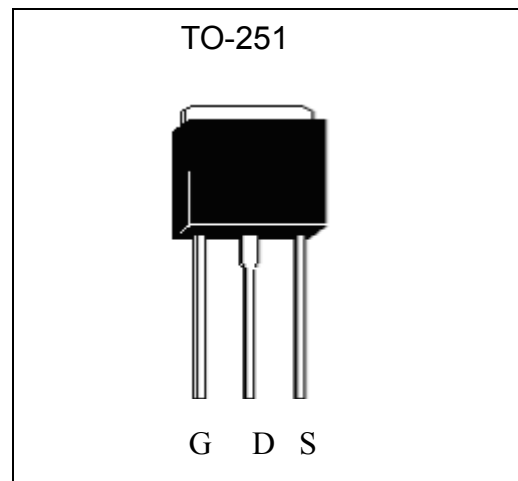
Features

- Low Gate Charge
- Simple Drive Requirement
- Pb-free lead plating package

Equivalent Circuit

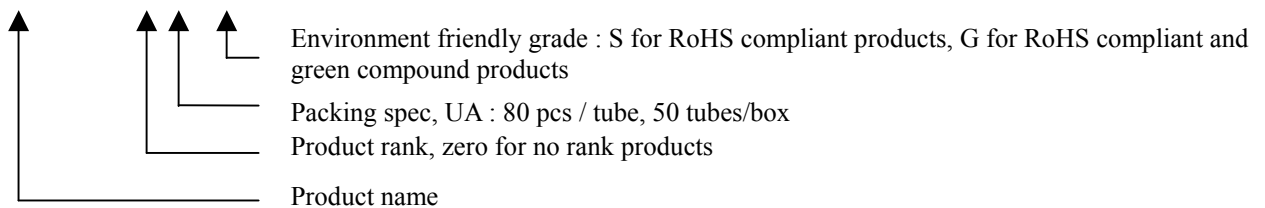


Outline



Ordering Information

Device	Package	Shipping
MTN6515I3-0-UA-G	TO-251 (RoHS compliant and halogen-free package)	80 pcs/tube, 50 tubes/box





Absolute Maximum Ratings (T_C=25°C, unless otherwise noted)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V _{DS}	150	V
Gate-Source Voltage	V _{GS}	±16	
Continuous Drain Current @ V _{GS} =10V, T _C =25°C	I _D	20	A
Continuous Drain Current @ V _{GS} =10V, T _C =100°C		14	
Pulsed Drain Current *1	I _{DM}	60	
Avalanche Current	I _{AS}	20	
Avalanche Energy @ L=0.47mH, I _D =20A, R _G =25Ω *3	E _{AS}	94	mJ
Repetitive Avalanche Energy @ L=0.05mH *2	E _{AR}	2.5	
Total Power Dissipation @T _C =25°C	P _D	60	W
Total Power Dissipation @T _C =100°C		30	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55~+175	°C

Note : *1. Pulse width limited by maximum junction temperature.
 *2. Duty cycle ≤ 1%.
 *3. 100% tested by conditions of L=0.47mH, I_{AS}=12A, V_{GS}=10V, V_{DD}=50V

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	R _{θJC}	2.5	°C/W
Thermal Resistance, Junction-to-ambient, max	R _{θJA}	100	

Characteristics (T_C=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	150	-	-	V	V _{GS} =0V, I _D =250μA
V _{GS(th)}	0.45	-	1.20		V _{DS} =V _{GS} , I _D =250μA
I _{GSS}	-	-	±100	nA	V _{GS} =±12V, V _{DS} =0V
I _{DSS}	-	-	1	μA	V _{DS} =120V, V _{GS} =0V
	-	-	25		V _{DS} =100V, V _{GS} =0V, T _J =125°C
R _{DS(ON)} *1	-	60	75	mΩ	V _{GS} =10V, I _D =15A
	-	59	75		V _{GS} =5V, I _D =10A
	-	60	75		V _{GS} =3V, I _D =3A
G _{FS} *1	-	48	-	S	V _{DS} =5V, I _D =10A
Dynamic					
Q _g *1, 2	-	30	-	nC	I _D =10A, V _{DS} =80V, V _{GS} =5V
Q _{gs} *1, 2	-	4.8	-		
Q _{gd} *1, 2	-	16	-		
t _{d(ON)} *1, 2	-	23	-	ns	V _{DS} =75V, I _D =1A, V _{GS} =4.5V, R _G =6Ω
t _r *1, 2	-	22	-		
t _{d(OFF)} *1, 2	-	91	-		
t _f *1, 2	-	63	-		



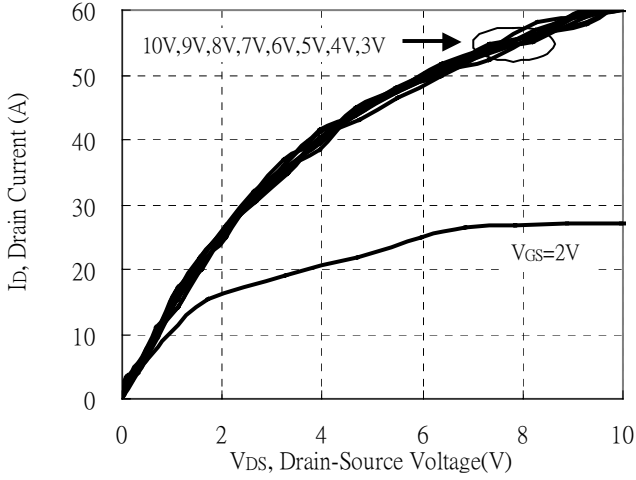
Ciss	-	2282	-	pF	V _{GS} =0V, V _{DS} =25V, f=1MHz
Coss	-	120	-		
Crss	-	66	-		
Source-Drain Diode					
I _S *1	-	-	20	A	
I _{SM} *3	-	-	60		
V _{SD} *1	-	0.85	1.3	V	I _F =I _S , V _{GS} =0V
trr	-	50	-	ns	I _F =20A, dI _F /dt=100A/μs
Qrr	-	120	-	nC	

Note : *1.Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%
*2.Independent of operating temperature
*3.Pulse width limited by maximum junction temperature.

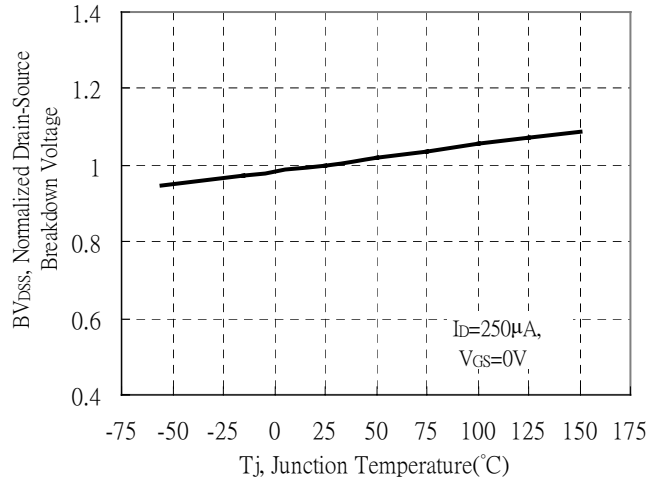


Typical Characteristics

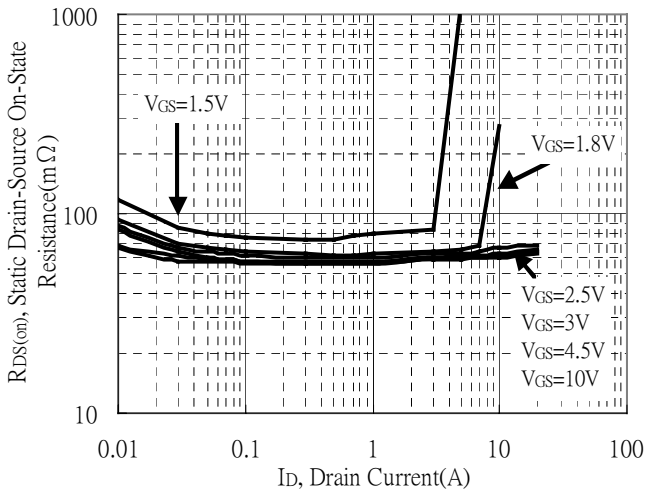
Typical Output Characteristics



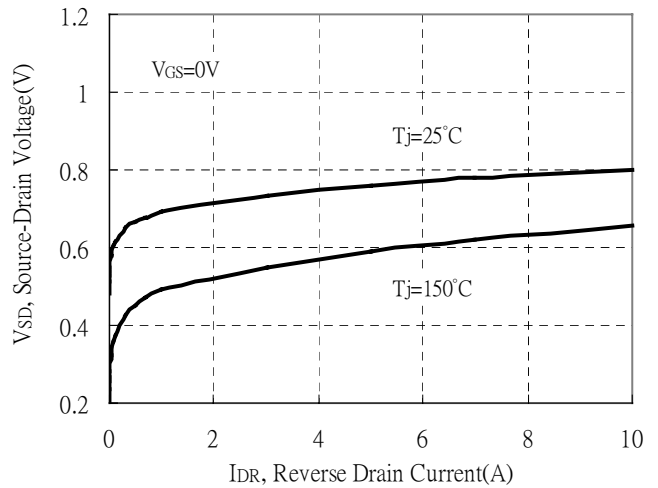
Brekdown Voltage vs Ambient Temperature



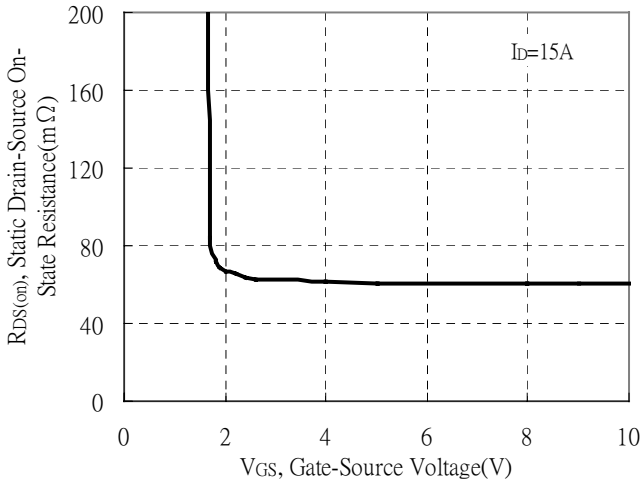
Static Drain-Source On-State resistance vs Drain Current



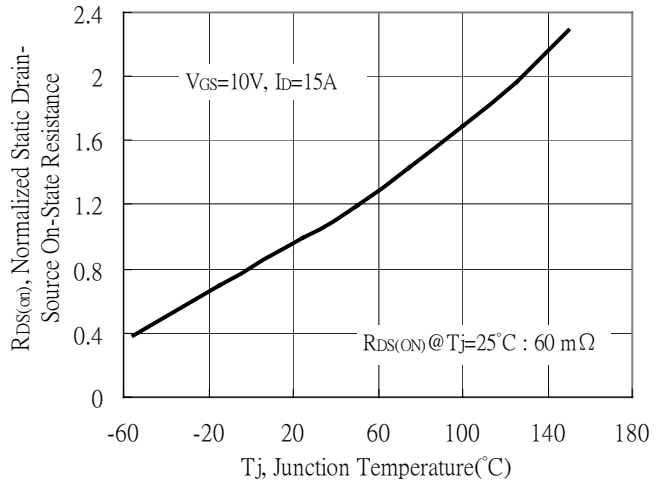
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage



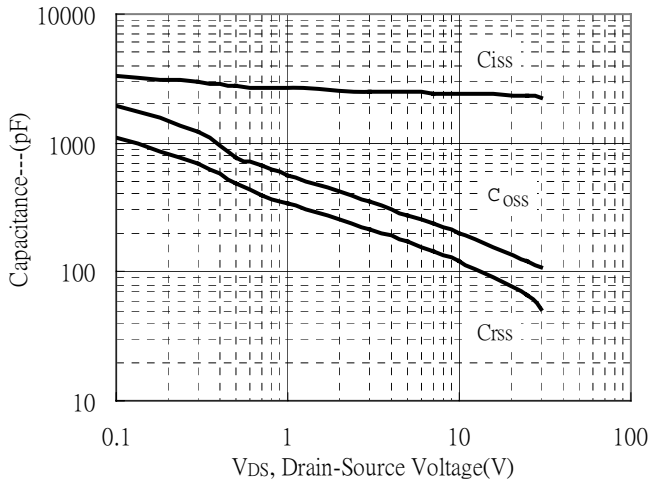
Drain-Source On-State Resistance vs Junction Temperature



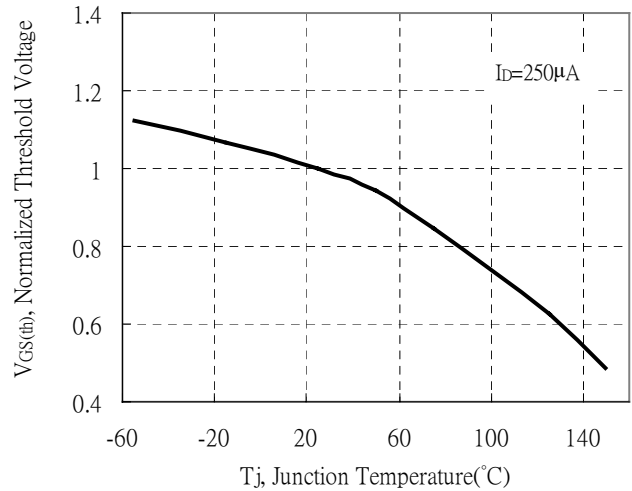


Typical Characteristics (Cont.)

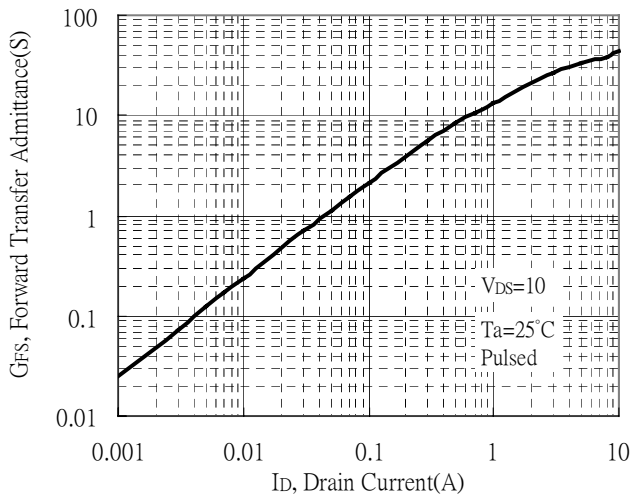
Capacitance vs Drain-to-Source Voltage



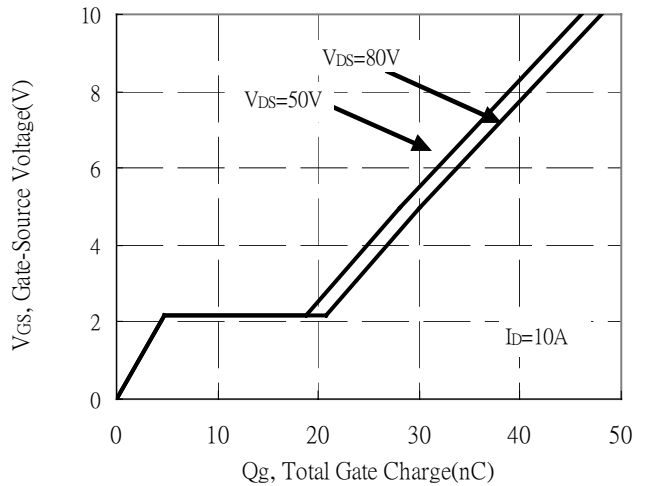
Threshold Voltage vs Junction Temperature



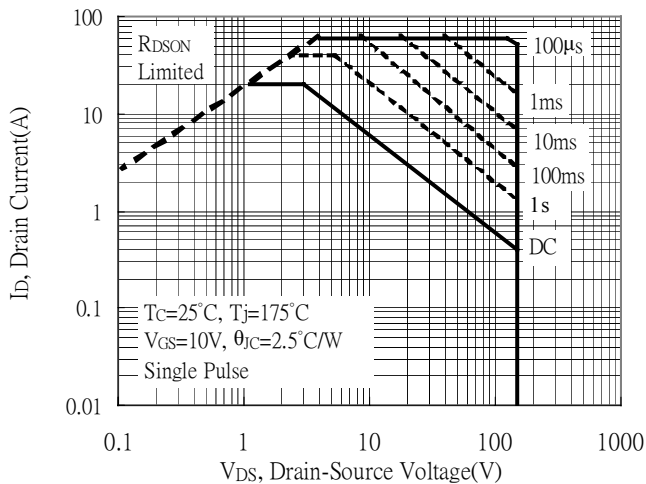
Forward Transfer Admittance vs Drain Current



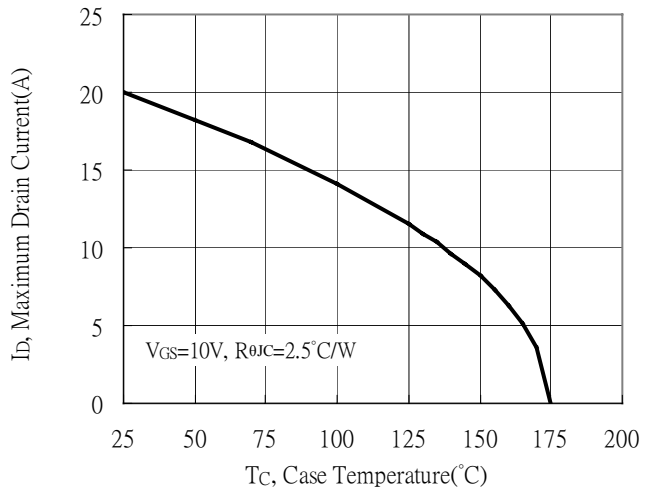
Gate Charge Characteristics



Maximum Safe Operating Area



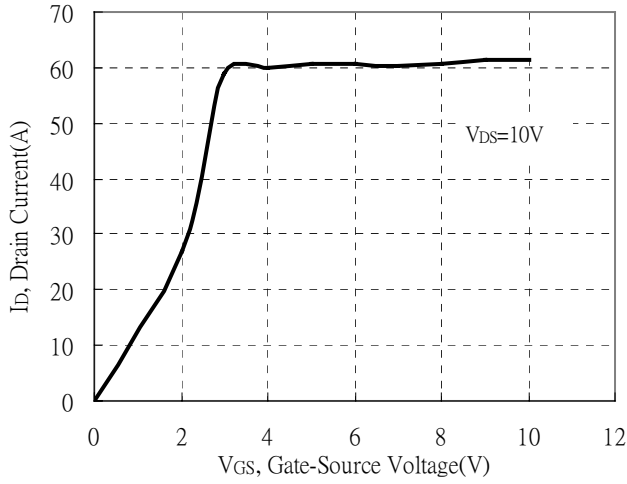
Maximum Drain Current vs Case Temperature



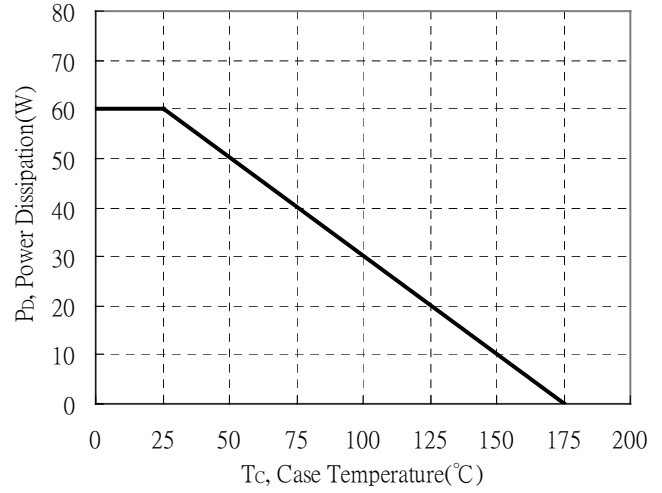


Typical Characteristics (Cont.)

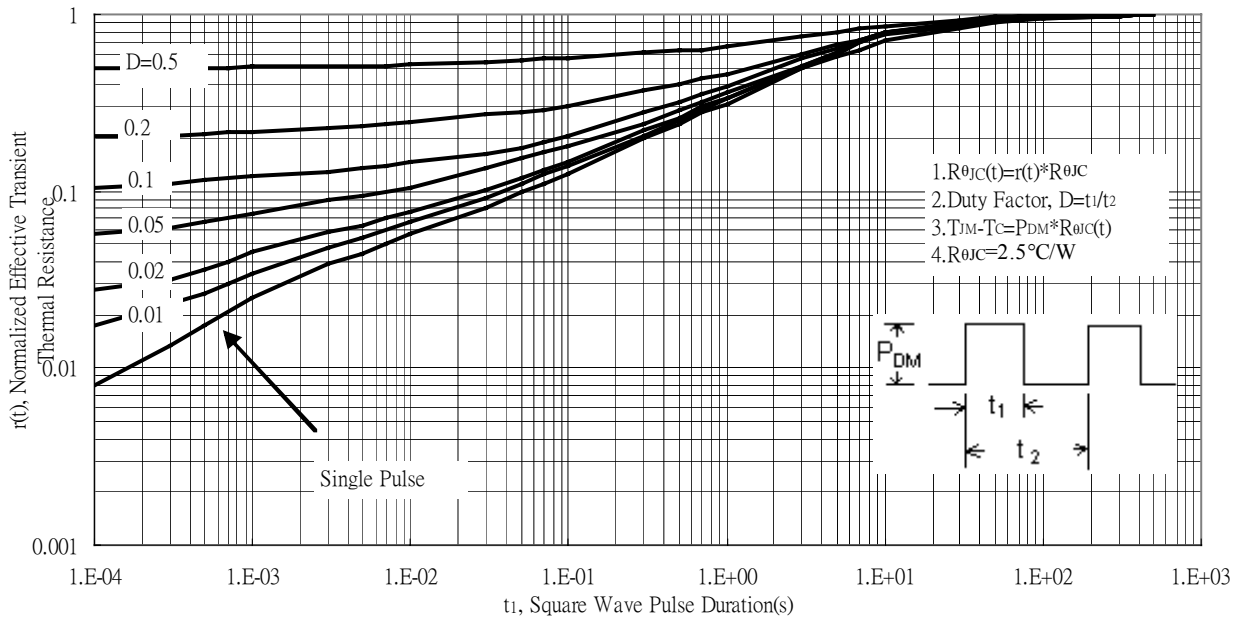
Typical Transfer Characteristics



Power Derating Curve



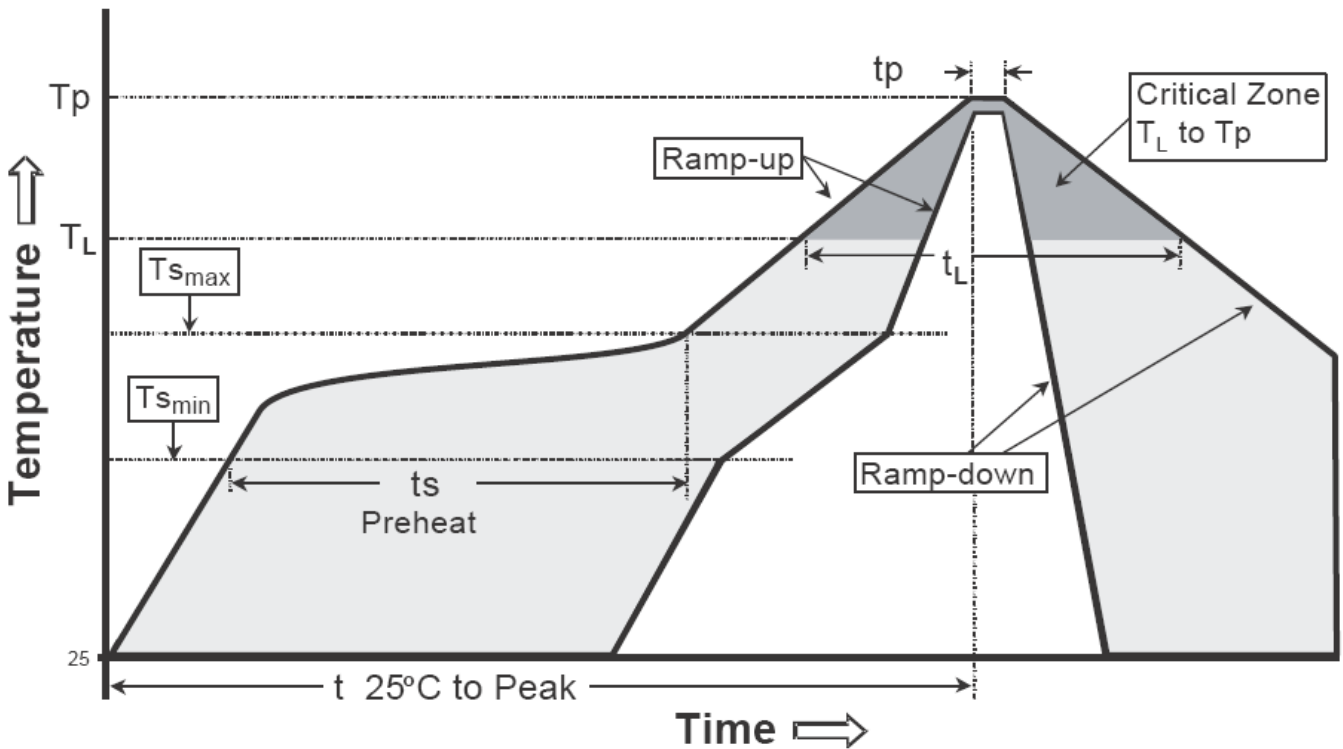
Transient Thermal Response Curves



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

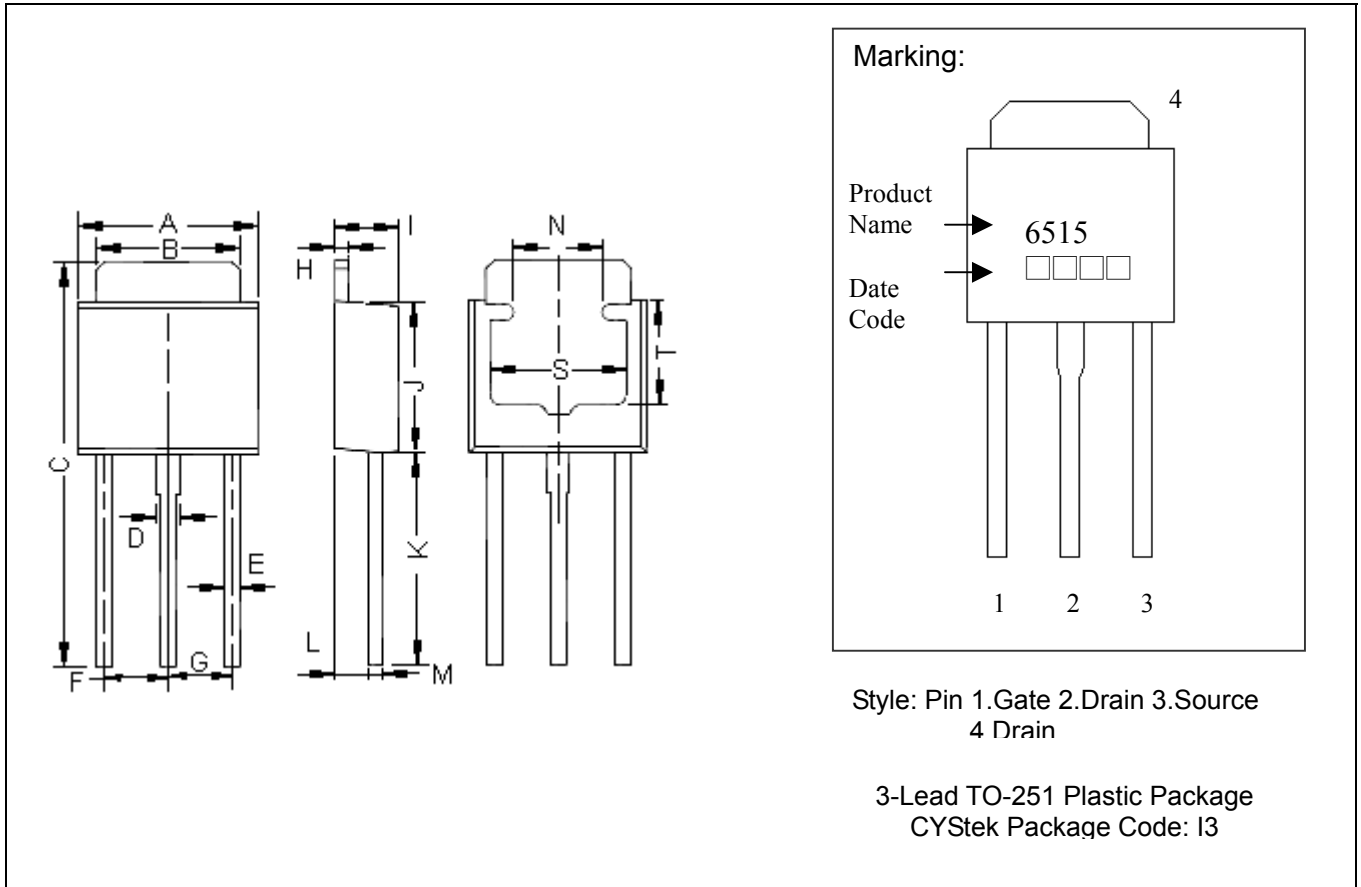
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-251 Dimension



Marking:

Product Name → 6515
 Date Code → □□□□

Style: Pin 1.Gate 2.Drain 3.Source
 4 Drain

3-Lead TO-251 Plastic Package
 CYStek Package Code: I3

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.2500	0.2618	6.35	6.65	I	0.0866	0.0945	2.20	2.40
B	0.2047	0.2126	5.20	5.40	J	0.2126	0.2244	5.40	5.70
C	0.5709	0.5866	14.50	14.90	K	0.2992	0.3071	7.60	7.80
D	0.0276	0.0354	0.70	0.90	L	0.0453	0.0492	1.15	1.25
E	0.0199	0.0276	0.50	0.70	M	0.0169	0.0228	0.43	0.58
F	0.0886	0.0925	2.25	2.35	N	0.1181	REF	3.00	REF
G	0.0886	0.0925	2.25	2.35	S	0.1969	REF	5.00	REF
H	0.0169	0.0228	0.43	0.58	T	0.1496	REF	3.80	REF

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

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