

N-Channel Enhancement Mode Power MOSFET

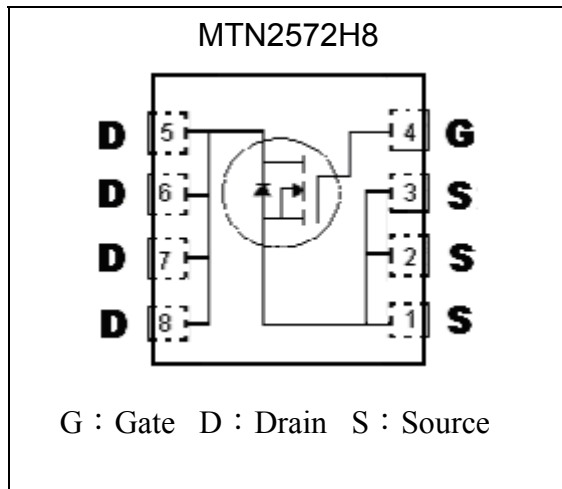
MTN2572H8

BV _{DSS}		150V
I _D @V _{GS} =10V, T _C =25°C		32A
R _{DS(on)} (TYP)	V _{GS} =10V, I _D =20A	36mΩ
	V _{GS} =10V, I _D =12A	36mΩ

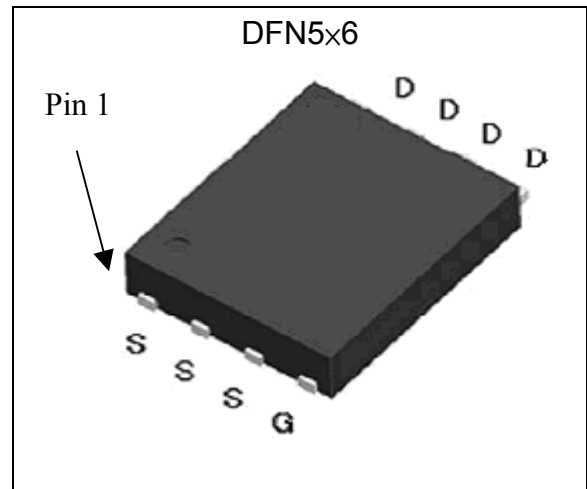
Features

- Single Drive Requirement
- Low On-resistance
- Fast Switching Characteristic
- Pb-free lead plating and Halogen-free package

Symbol

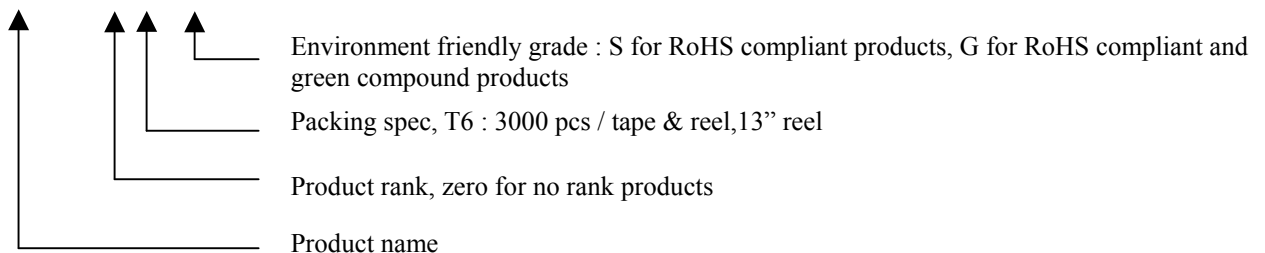


Outline



Ordering Information

Device	Package	Shipping
MTN2572H8-0-T6-G	DFN 5 ×6 (Pb-free lead plating and halogen-free package)	3000 pcs / tape & reel





Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit	
Drain-Source Voltage	V _{DS}	150	V	
Gate-Source Voltage	V _{GS}	±20		
Continuous Drain Current @ T _C =25°C, V _{GS} =10V (Note 1)	I _D	32	A	
Continuous Drain Current @ T _C =100°C, V _{GS} =10V (Note 1)		23		
Continuous Drain Current @ T _A =25°C, V _{GS} =10V (Note 2)	I _{DSM}	5.2 *3		
Continuous Drain Current @ T _A =70°C, V _{GS} =10V (Note 2)		4.2 *3		
Pulsed Drain Current (Note 3)	I _{DM}	60 *1		
Avalanche Current (Note 3)	I _{AS}	30		
Avalanche Energy @ L=0.1mH, I _D =18A, V _{DD} =25V (Note 5)	E _{AS}	16	mJ	
Repetitive Avalanche Energy @ L=0.05mH (Note 3)	E _{AR}	22.5 *2		
Total Power Dissipation	P _D	T _C =25°C (Note 1)	94	W
		T _C =100°C (Note 1)	47	
	P _{DSM}	T _A =25°C (Note 2)	2.5	
		T _A =70°C (Note 2)	1.6	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55~+175	°C	

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	R _{θJC}	1.6	°C/W
Thermal Resistance, Junction-to-ambient, max (Note 2)	R _{θJA}	50	
Thermal Resistance, Junction-to-ambient, max (Note 4)		125	

- Note : 1. The power dissipation P_D is based on T_{J(MAX)}=175 °C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
2. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2 oz. copper, in a still air environment with T_A=25 °C. The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
3. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175 °C. Ratings are based on low frequency and low duty cycles to keep initial T_J=25°C.
4. When mounted on the minimum pad size recommended (PCB mount), t≤10s.
5. 100% tested by conditions of L=0.1mH, I_{AS}=10A, V_{GS}=10V, V_{DD}=25V

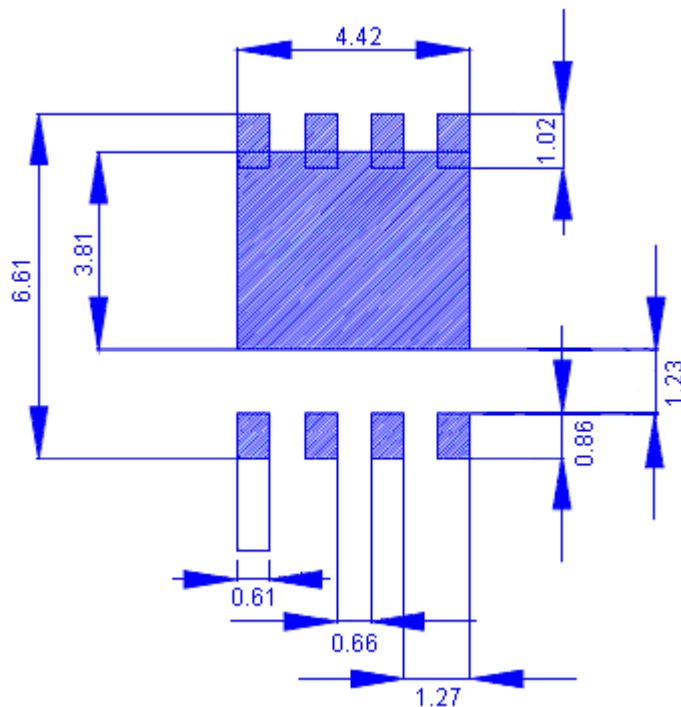
Characteristics (Tc=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	150	-	-	V	V _{GS} =0V, I _D =250µA
ΔBV _{DSS} /ΔT _J	-	0.1	-	V/°C	Reference to 25°C, I _D =250µA
V _{GS(th)}	1.5	-	4	V	V _{DS} = V _{GS} , I _D =250µA
G _{FS} *1	-	40.6	-	S	V _{DS} =5V, I _D =20A
I _{GSS}	-	-	±100	nA	V _{GS} =±20V, V _{DS} =0V
I _{DSS}	-	-	1	µA	V _{DS} =120V, V _{GS} =0V
	-	-	25		V _{DS} =120V, V _{GS} =0V, T _J =125°C
R _{DS(ON)} *1	-	36	45	mΩ	V _{GS} =10V, I _D =20A
	-	36	45		V _{GS} =10V, I _D =12A

Dynamic					
Ciss	-	2102	2740	pF	V _{GS} =0V, V _{DS} =25V, f=1MHz
Coss	-	233	310		
Crss	-	71	110		
Qg *1,2	-	42.8	64.2	nC	I _D =20A, V _{DS} =80V, V _{GS} =10V
Qgs *1,2	-	8.2	12.3		
Qgd *1,2	-	13	19.5		
t _{d(ON)} *1,2	-	18.4	-	ns	V _{DS} =75V, I _D =1A, V _{GS} =10V, R _G =6Ω
t _r *1,2	-	30.4	-		
t _{d(OFF)} *1,2	-	60	-		
t _f *1,2	-	16.4	-		
R _g	-	3.4	-	Ω	f=1MHz
Source-Drain Diode					
I _S *1	-	-	32	A	
I _{SM} *3	-	-	60		
V _{SD} *1	-	0.79	1.3	V	I _S =12A, V _{GS} =0V
t _{rr}	-	55	-	ns	I _F =25A, dI _F /dt=100A/μs
Q _{rr}	-	154	-	nC	

Note : *1.Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%
 *2.Independent of operating temperature
 *3.Pulse width limited by maximum junction temperature.

Recommended Soldering Footprint

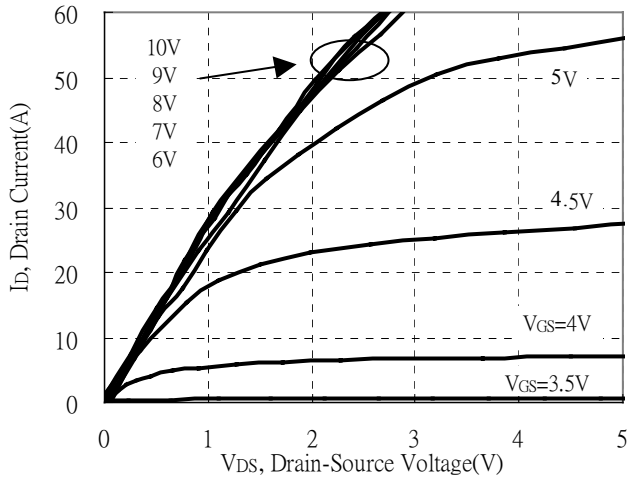


unit : mm

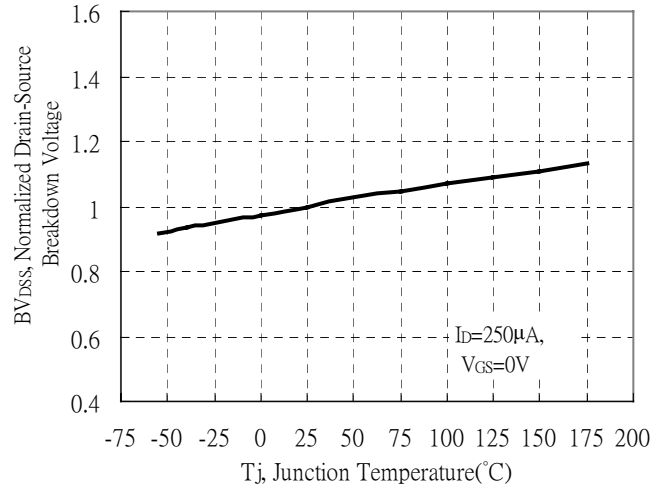


Typical Characteristics

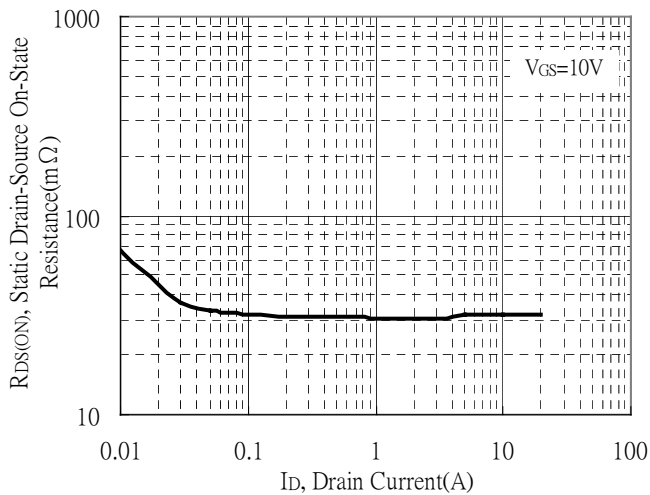
Typical Output Characteristics



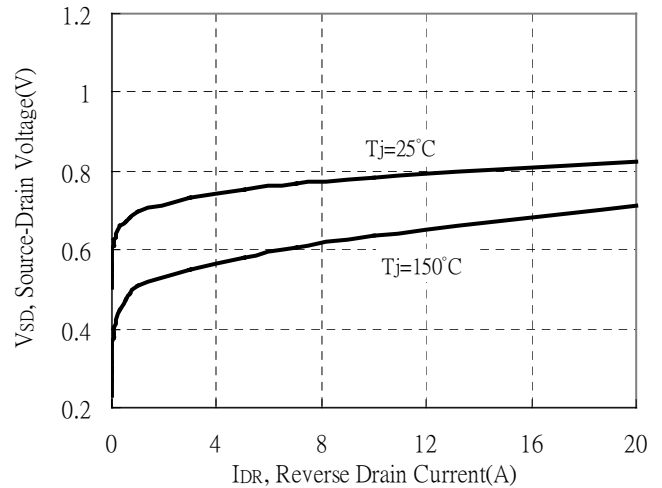
Brekdown Voltage vs Ambient Temperature



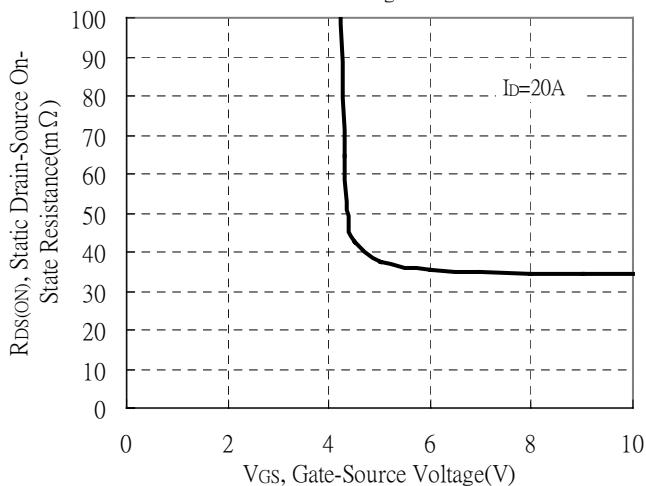
Static Drain-Source On-State resistance vs Drain Current



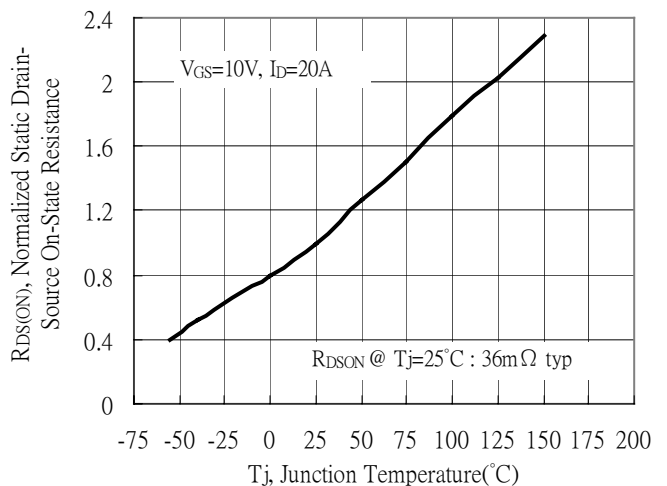
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

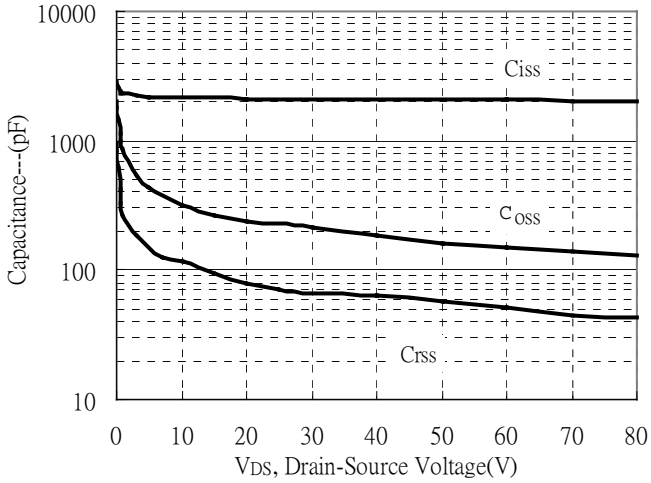


Drain-Source On-State Resistance vs Junction Temperature

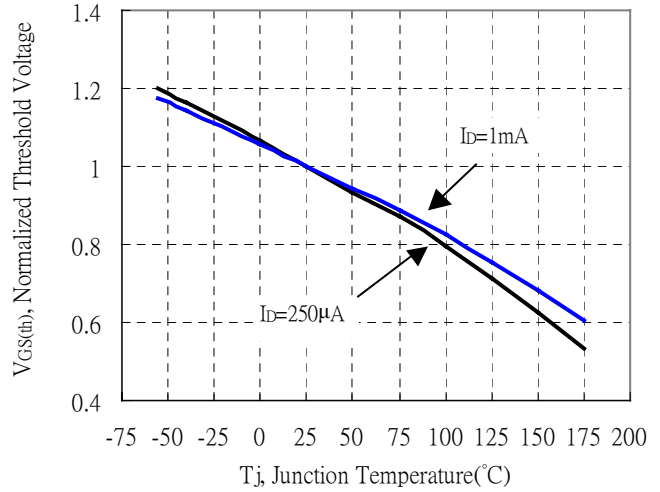


Typical Characteristics(Cont.)

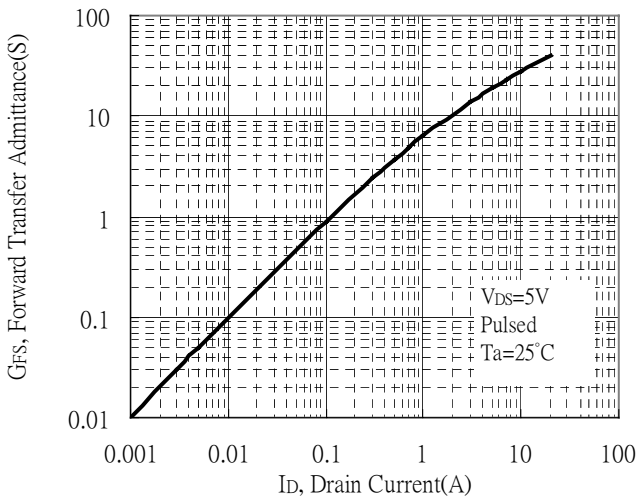
Capacitance vs Drain-to-Source Voltage



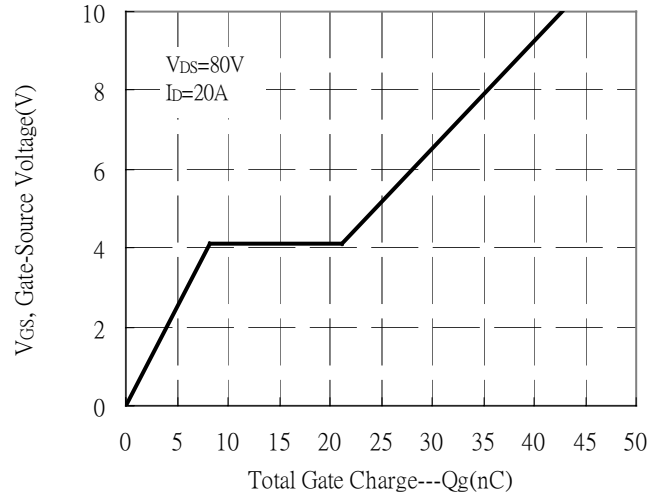
Normalized Threshold Voltage vs Junction Temperature



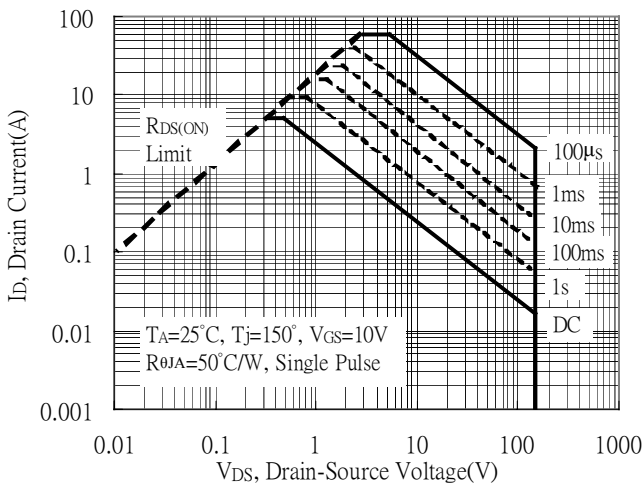
Forward Transfer Admittance vs Drain Current



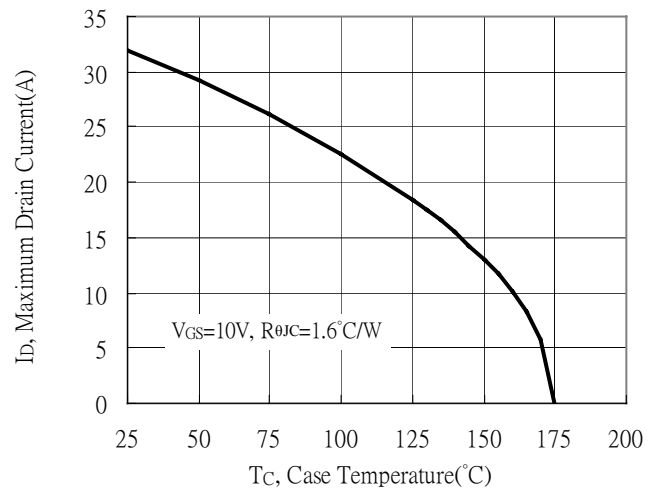
Gate Charge Characteristics



Maximum Safe Operating Area

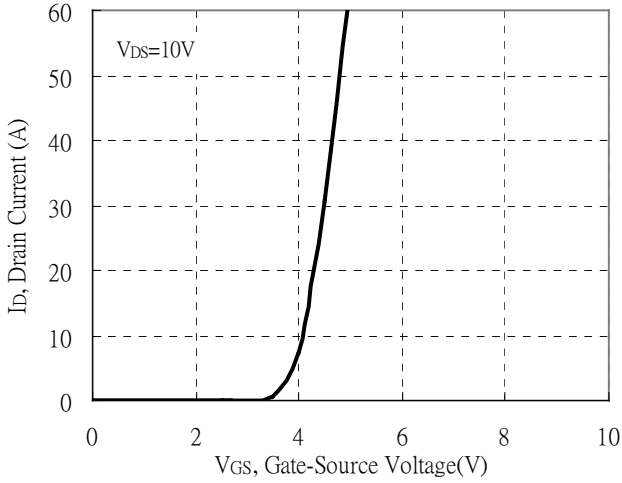


Maximum Drain Current vs Case Temperature

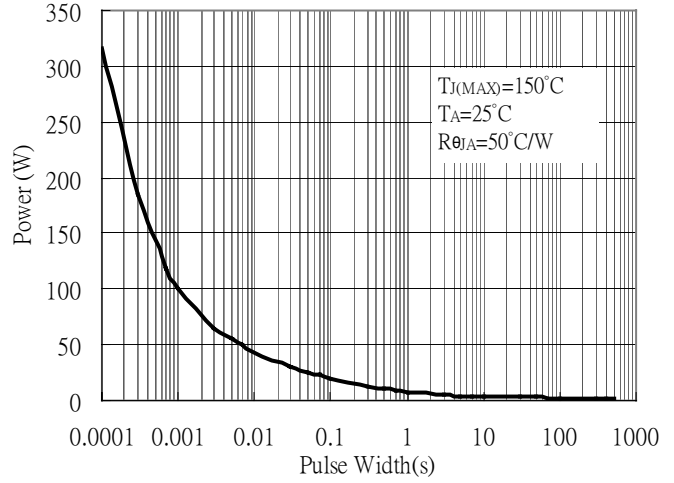


Typical Characteristics(Cont.)

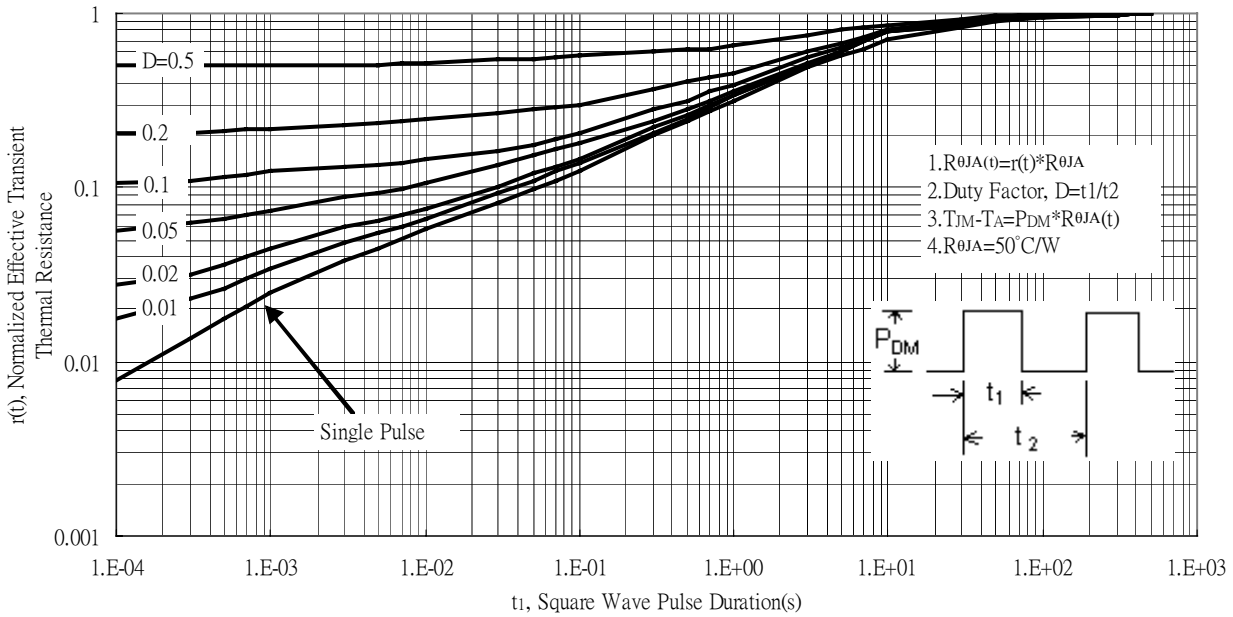
Typical Transfer Characteristics



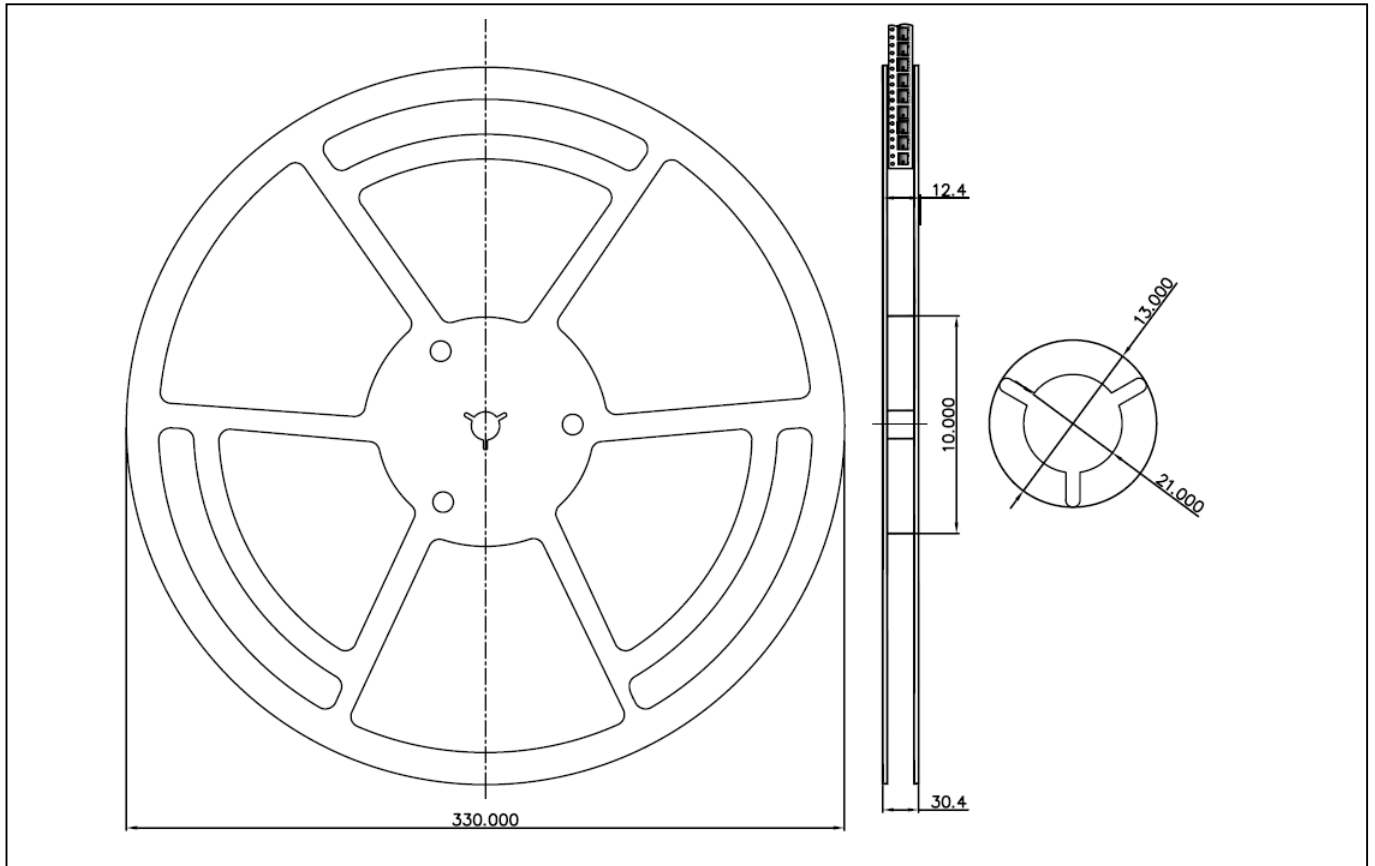
Single Pulse Maximum Power Dissipation



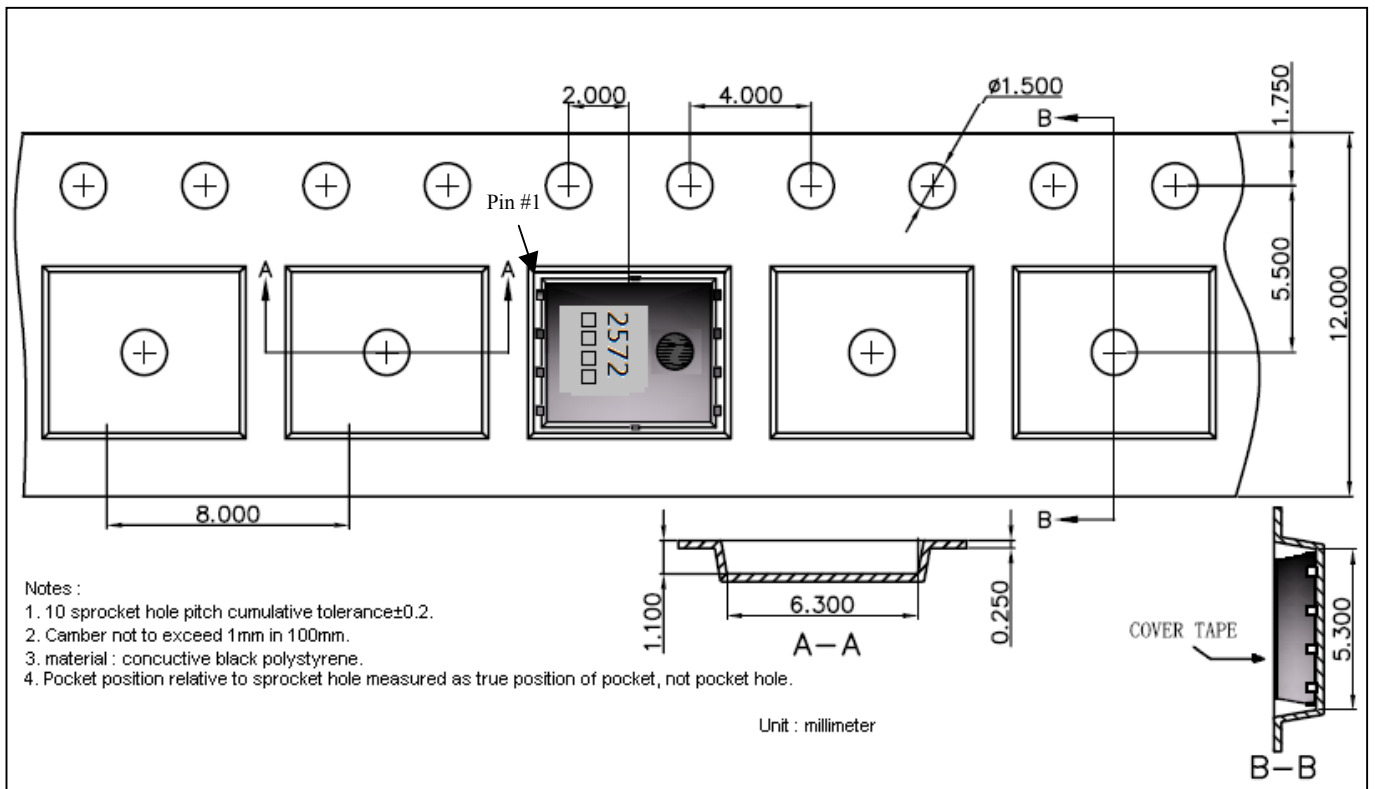
Transient Thermal Response Curves



Reel Dimension



Carrier Tape Dimension



Notes :

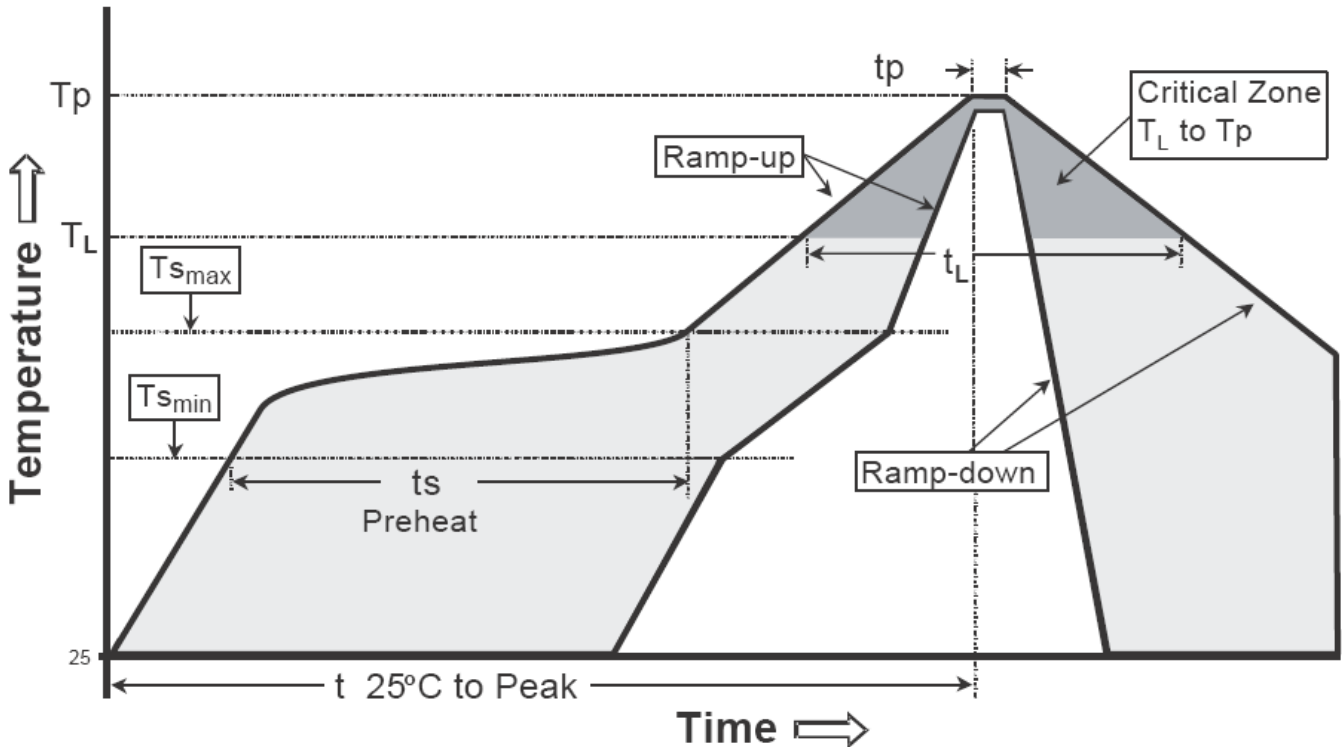
1. 10 sprocket hole pitch cumulative tolerance ± 0.2 .
2. Camber not to exceed 1mm in 100mm.
3. material : conductive black polystyrene.
4. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Unit : millimeter

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

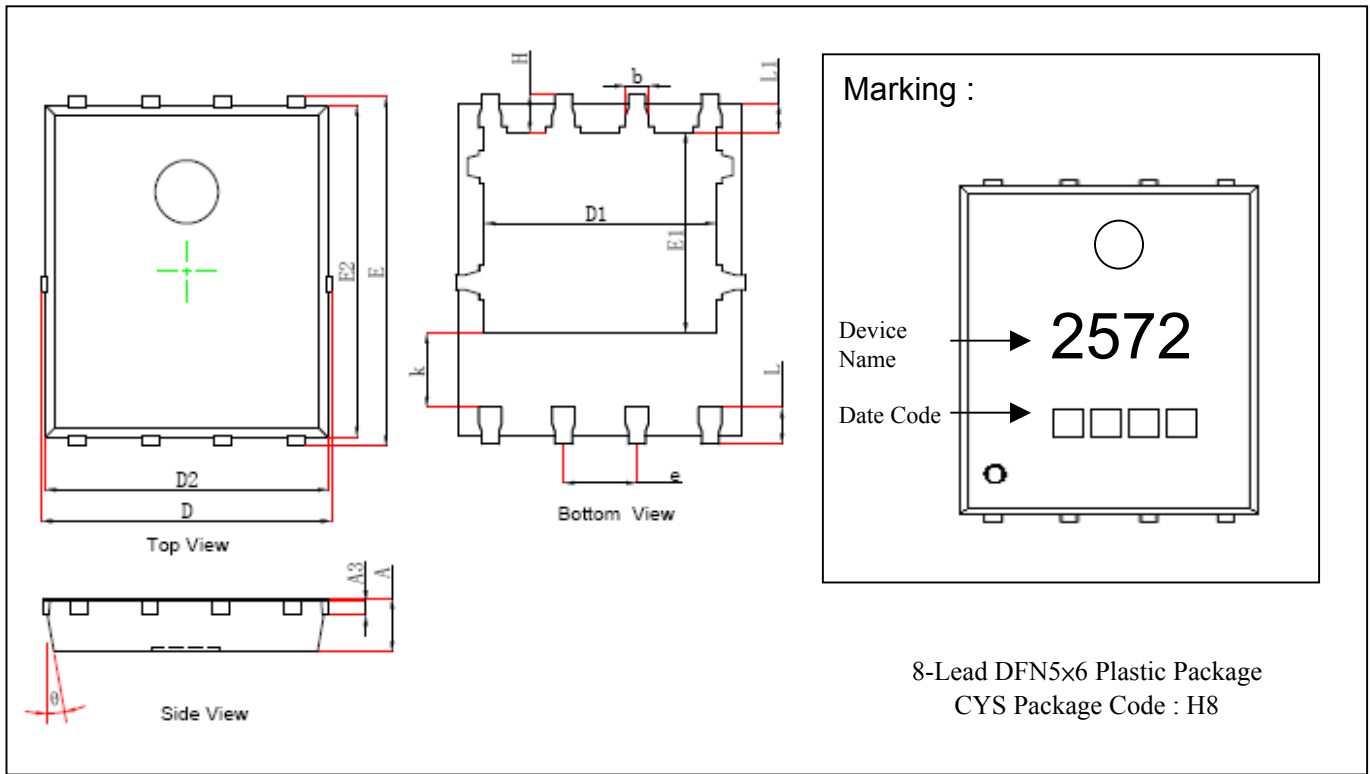
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (Tl)	183°C	217°C
- Time (tl)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

DFN5x6 Dimension (C Forming)



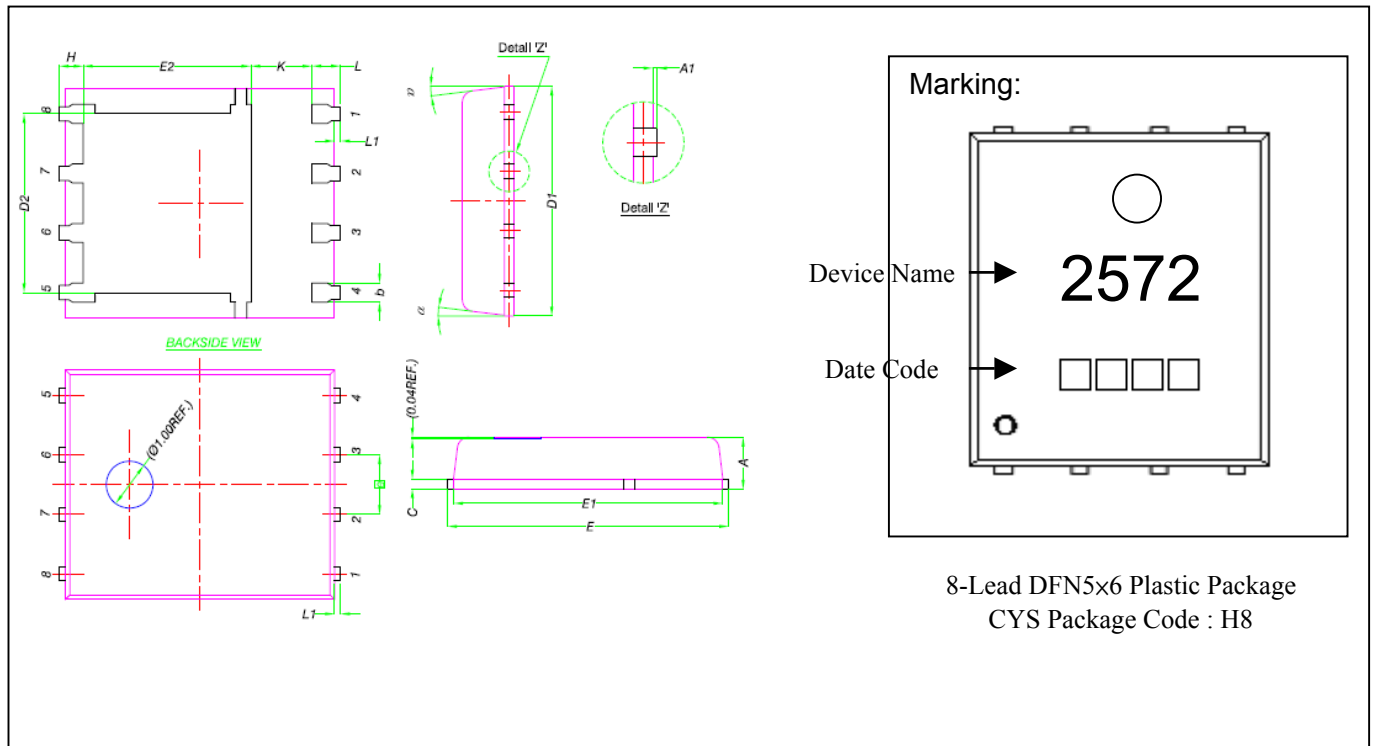
DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039	k	1.190	1.390	0.047	0.055
A3	0.254	REF	0.010	REF	b	0.350	0.450	0.014	0.018
D	4.944	5.096	0.195	0.201	e	1.270	TYP.	0.050	TYP.
E	5.974	6.126	0.235	0.241	L	0.559	0.711	0.022	0.028
D1	3.910	4.110	0.154	0.162	L1	0.424	0.576	0.017	0.023
E1	3.375	3.575	0.133	0.141	H	0.574	0.726	0.023	0.029
D2	4.824	4.976	0.190	0.196	θ	10°	12°	10°	12°
E2	5.674	5.826	0.223	0.229					

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

DFN5x6 Dimension (G Forming)



DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.90	1.10	0.035	0.043	E2	3.38	3.78	0.133	0.149
A1	0.00	0.05	0.000	0.002	e	1.27	BSC	0.050	BSC
b	0.33	0.51	0.013	0.020	H	0.41	0.61	0.016	0.024
C	0.20	0.30	0.008	0.012	K	1.10	-	0.043	-
D1	4.80	5.00	0.189	0.197	L	0.51	0.71	0.020	0.028
D2	3.61	3.96	0.142	0.156	L1	0.06	0.20	0.002	0.008
E	5.90	6.10	0.232	0.240	θ	8°	12°	8°	12°
E1	5.70	5.80	0.224	0.228					

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.