N-Channel Enhancement Mode Power MOSFET

MTN12N30FP

BV_{DSS}	300V
I_D@V_{GS}=10V, T_C=25˚C	12A
$R_{DSON(TYP)}$@ V_{GS}=10V, I_D=6A	248mΩ

Description

The MTN12N30FP is a N-channel enhancement-mode MOSFET, providing the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness.
The TO-220FP package is universally preferred for all commercial-industrial applications

Features

- Low On Resistance
- Simple Drive Requirement
- Low Gate Charge
- Fast Switching Characteristic
- Insulating package, front/back side insulating voltage=2500V(AC)
- RoHS compliant package

Applications

- Power Factor Correction
- LCD TV Power
- Full and Half Bridge Power

Ordering Information

Device	Package	Shipping
MTN12N30FP-0-UB-S	TO-220FP (RoHS compliant package)	50 pcs/tube, 20 tubes/box, 4 boxes / carton

Environment friendly grade : S for RoHS compliant products, G for RoHS compliant and green compound products

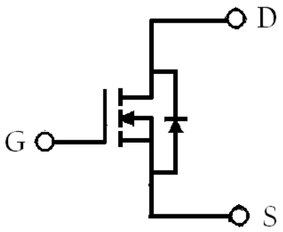
Packing spec, UB : 50 pcs / tube, 20 tubes/box

Product rank, zero for no rank products

Product name

Symbol

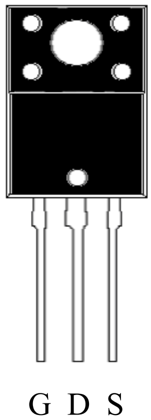
MTN12N30FP



G : Gate
D : Drain
S : Source

Outline

TO-220FP



Absolute Maximum Ratings (Tc=25°C)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage (Note 1)	V_{DS}	300	V
Gate-Source Voltage	V_{GS}	±30	
Continuous Drain Current	I_D	12*	A
Continuous Drain Current @Tc=100°C		7.6*	
Pulsed Drain Current @ V_{GS}=10V (Note 2)	I_{DM}	30*	
Avalanche Current	I_{AS}	3.8	
Single Pulse Avalanche Energy @ L=60mH, I_D=3.8Amps, V_{DD}=150V (Note3)	E_{AS}	430	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	5	V/ns
Maximum Temperature for Soldering @ Lead at 0.063 in(1.6mm) from case for 10 seconds	T_L	300	°C
Maximum Temperature for Soldering @ Package Body for 10 seconds	T_{PKG}	260	°C
Total Power Dissipation (Tc=25℃)	P_D	36	W
Linear Derating Factor above 25℃		0.3	W/°C
Operating Junction and Storage Temperature	Tj, Tstg	-55~+150	°C

*Drain current limited by maximum junction temperature

Note : 1. T_J=+25℃ to +150℃.
2. Pulse width limited by maximum junction temperature.
3. 100% tested by conditions of L=10mH, I_{AS}=2A, V_{DD}=150V.
4. I_{SD}=10A, dI/dt<100A/μs, V_{DD}<BV_{DSS}, T_J=+150℃.

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{th,j-c}$	3.5	°C/W
Thermal Resistance, Junction-to-ambient, max	$R_{th,j-a}$	65	°C/W

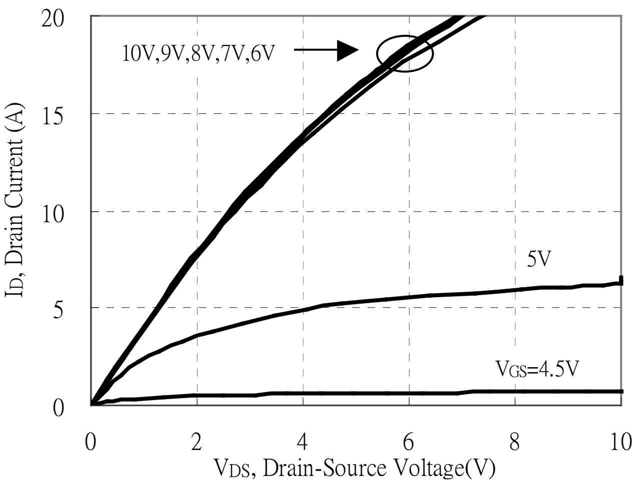
Characteristics (Tj=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV_{DSS}	300	-	-	V	V_{GS}=0V, I_D=250μA
$\Delta BV_{DSS}/\Delta Tj$	-	0.29	-	V/°C	Reference to 25°C, I_D=250μA
$V_{GS(th)}$	3.0	-	4.5	V	V_{DS} = V_{GS}, I_D=250μA
*G_{FS}	5	10.2	30	S	V_{DS} =15V, I_D=6A
I_{GSS}	-	-	±100	nA	V_{GS}=±30V, V_{DS}=0V
I_{DSS}	-	-	1	μA	V_{DS} =300V, V_{GS} =0V
	-	-	25		V_{DS} =240V, V_{GS} =0V, Tj=125°C
*$R_{DS(ON)}$	120	248	340	mΩ	V_{GS} =10V, I_D=6A
Dynamic					
*Qg	18	24.7	31	nC	I_D=12A, V_{DD}=240V, V_{GS}=10V
*Qgs	4	5.8	8		
*Qgd	7	10.3	13		
*$t_{d(ON)}$	7	14.6	22	ns	V_{DD}=150V, I_D=12A, V_{GS}=10V, R_G=25Ω
*tr	23	46.2	69		
*$t_{d(OFF)}$	19	39.2	59		
*t_f	30	59.6	89		
Ciss	765	1022	1280	pF	V_{GS}=0V, V_{DS}=25V, f=1MHz
Coss	65	88	110		
Crss	36	48	60		
Rg	0.5	1.1	2.0	Ω	f=1MHz
Source-Drain Diode					
*I_S	-	-	12	A	
*I_{SM}	-	-	30		
*V_{SD}	0.5	0.71	1	V	I_S=1A, V_{GS}=0V
*trr	95	121	145	ns	V_{GS}=0V, I_F=12A, dI_F/dt=100A/μs
*Qrr	390	490	640	μC	

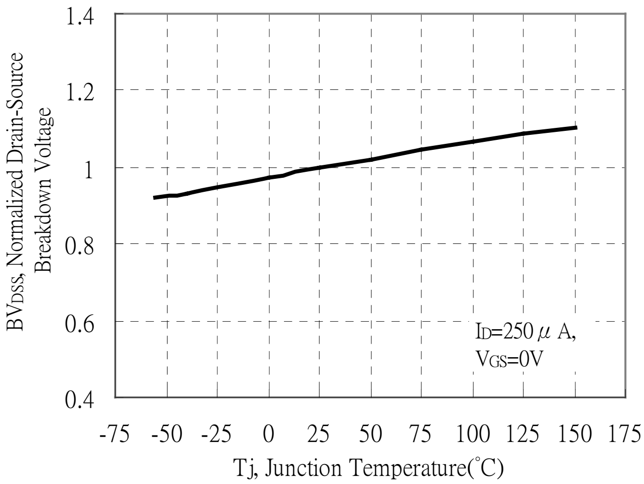
*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Typical Characteristics

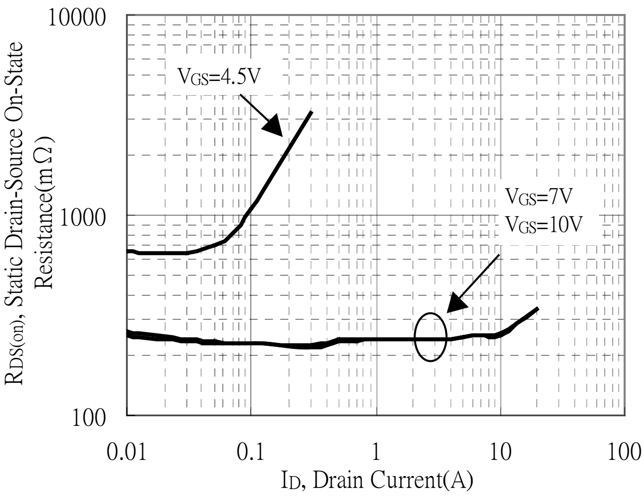
Typical Output Characteristics



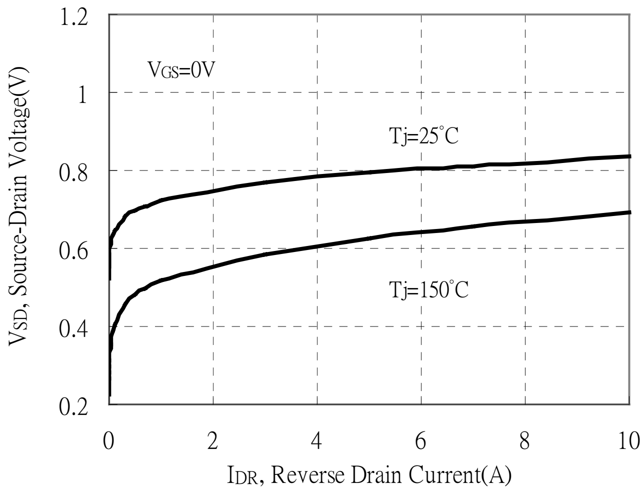
Brekdown Voltage vs Ambient Temperature



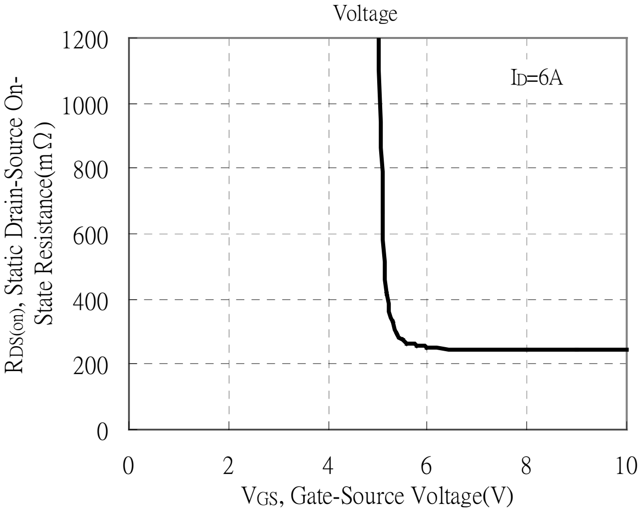
Static Drain-Source On-State resistance vs Drain Current



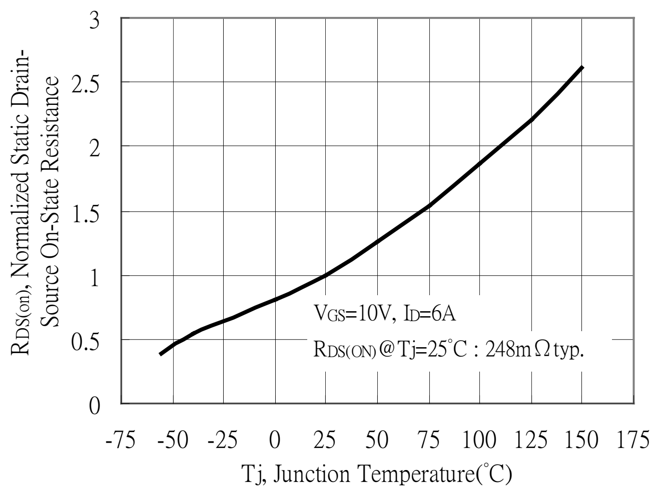
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

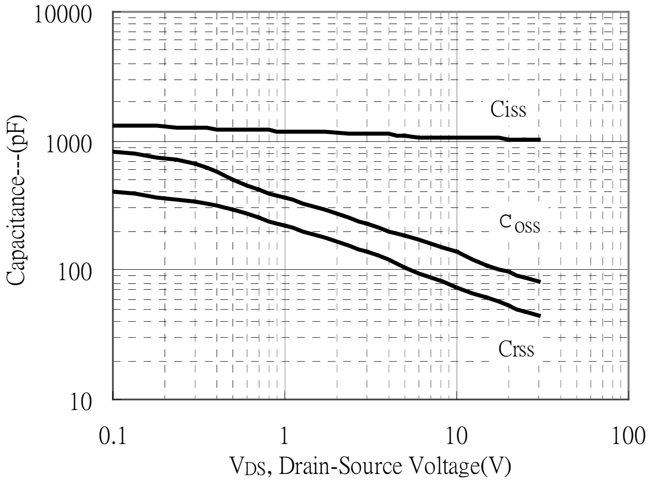


Drain-Source On-State Resistance vs Junction Tempearture

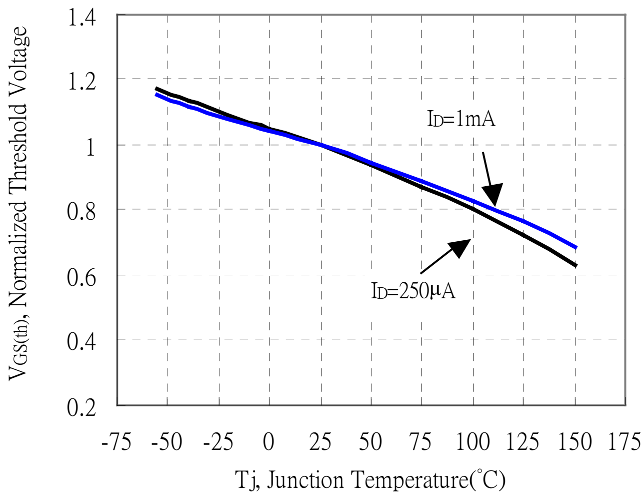


Typical Characteristics(Cont.)

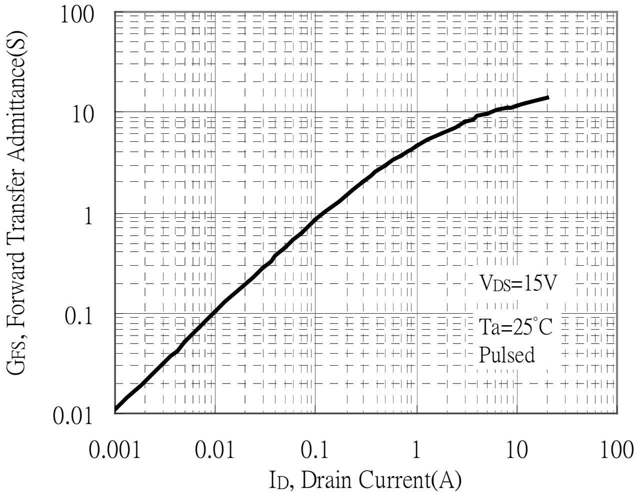
Capacitance vs Drain-to-Source Voltage



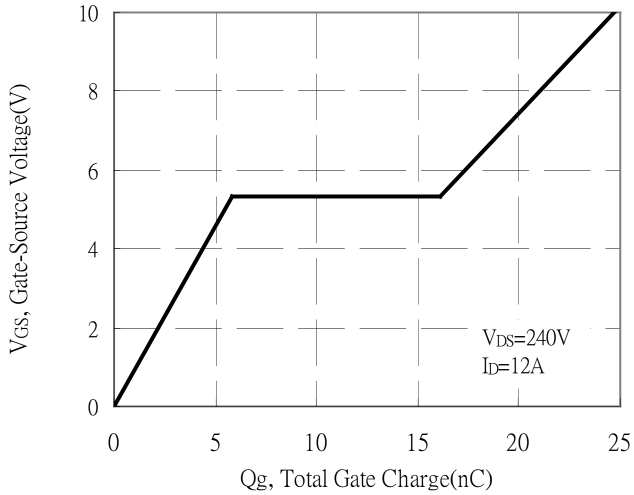
Threshold Voltage vs Junction Tempearture



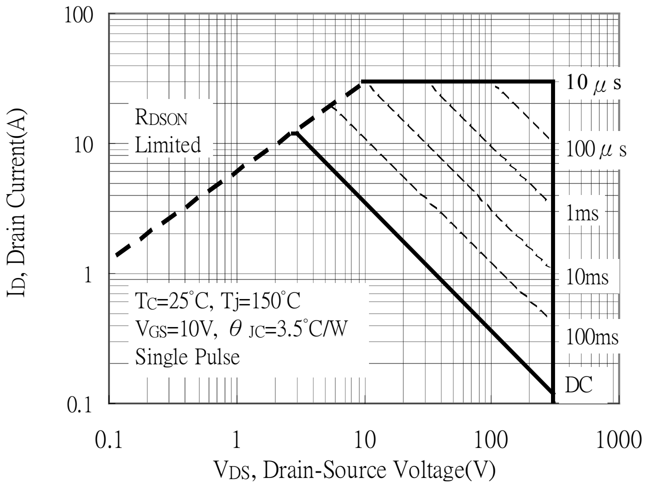
Forward Transfer Admittance vs Drain Current



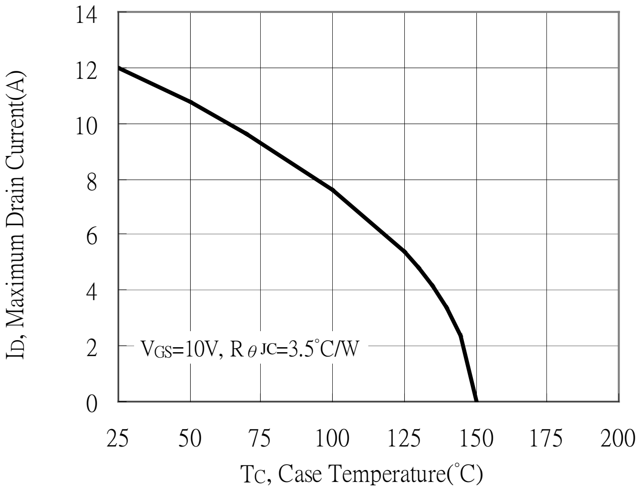
Gate Charge Characteristics



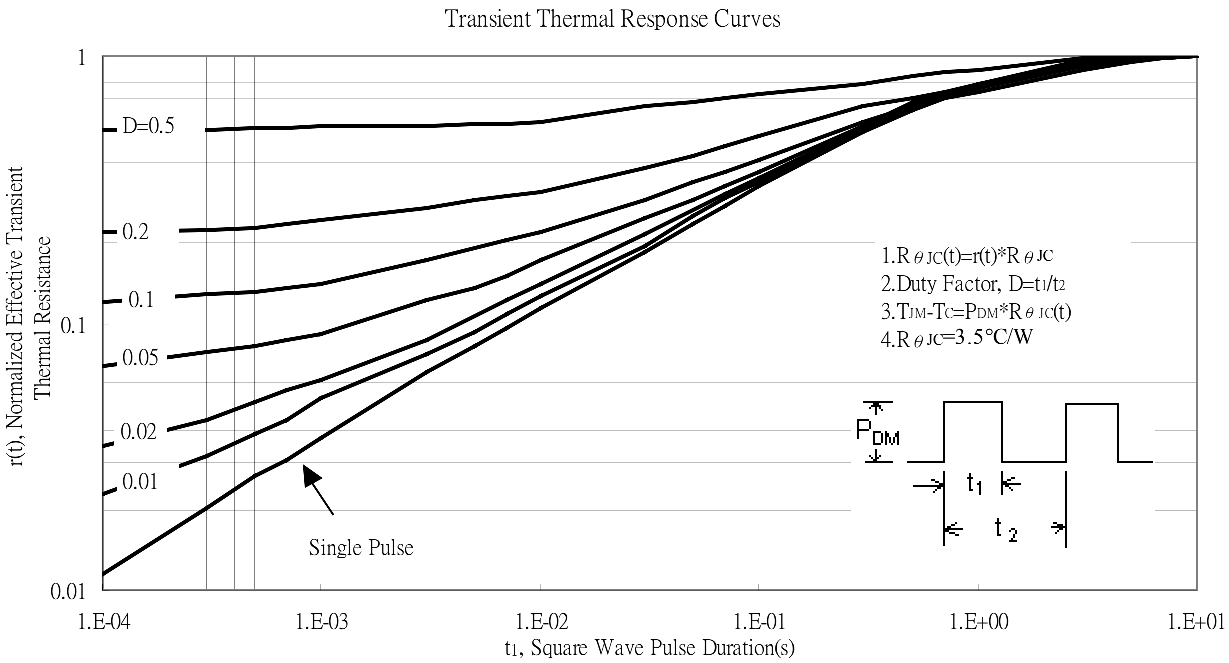
Maximum Safe Operating Area



Maximum Drain Current vs Case Temperature



Typical Characteristics(Cont.)



Test Circuit and Waveforms

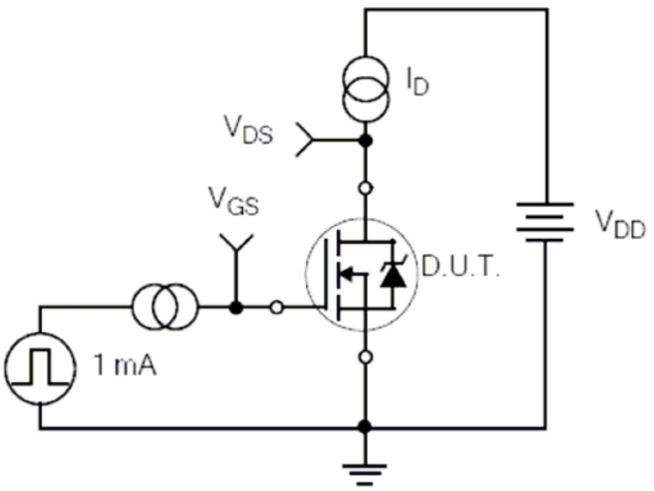


Figure 12. Gate Charge Test Circuit

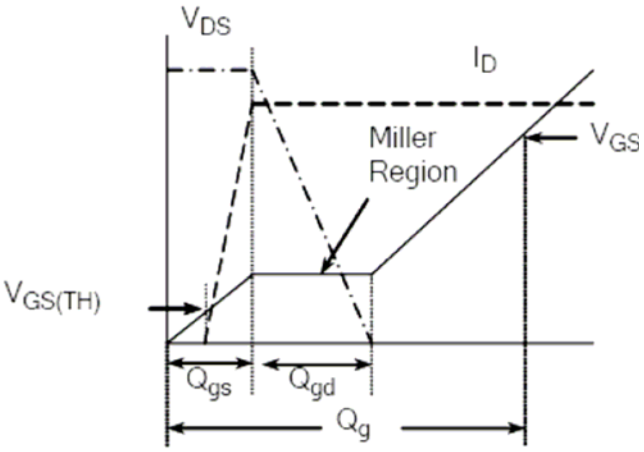


Figure 13. Gate Charge Waveform

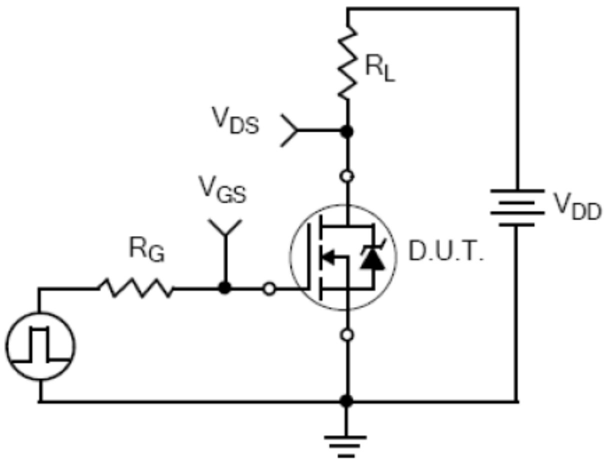


Figure 14. Resistive Switching Test Circuit

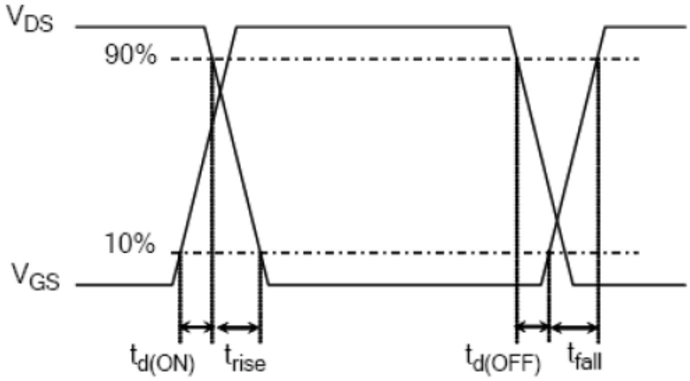


Figure 15. Resistive Switching Waveforms

Test Circuit and Waveforms(Cont.)

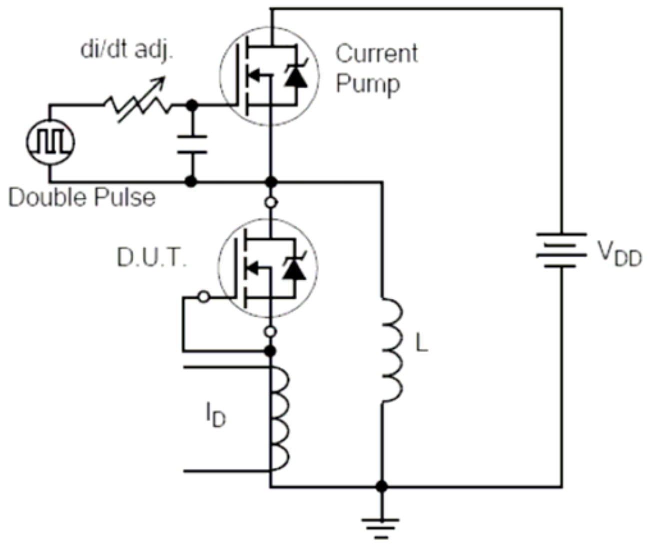


Figure 16. Diode Reverse Recovery Test Circuit

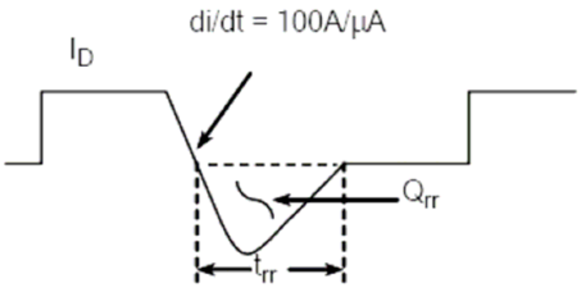


Figure 17. Diode Reverse Recovery Waveform

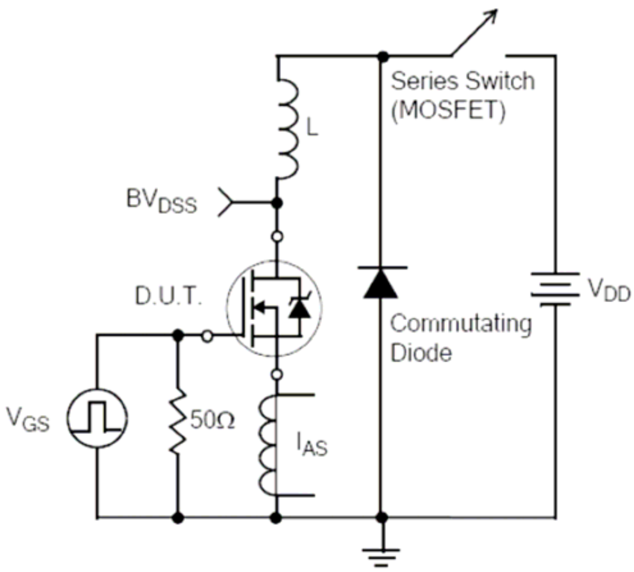
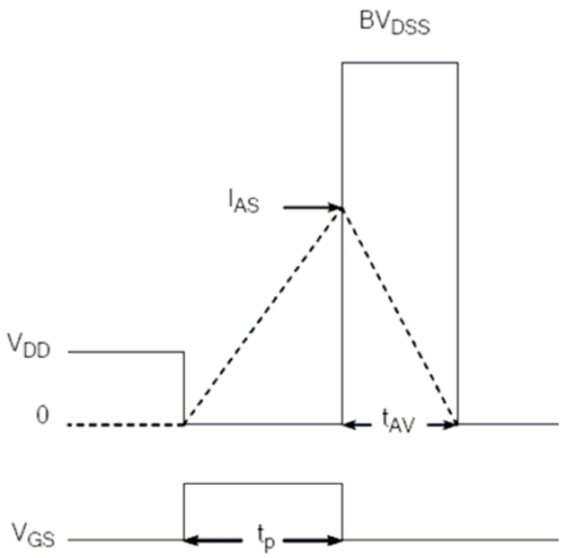


Figure 18. Unclamped Inductive Switching Test Circuit



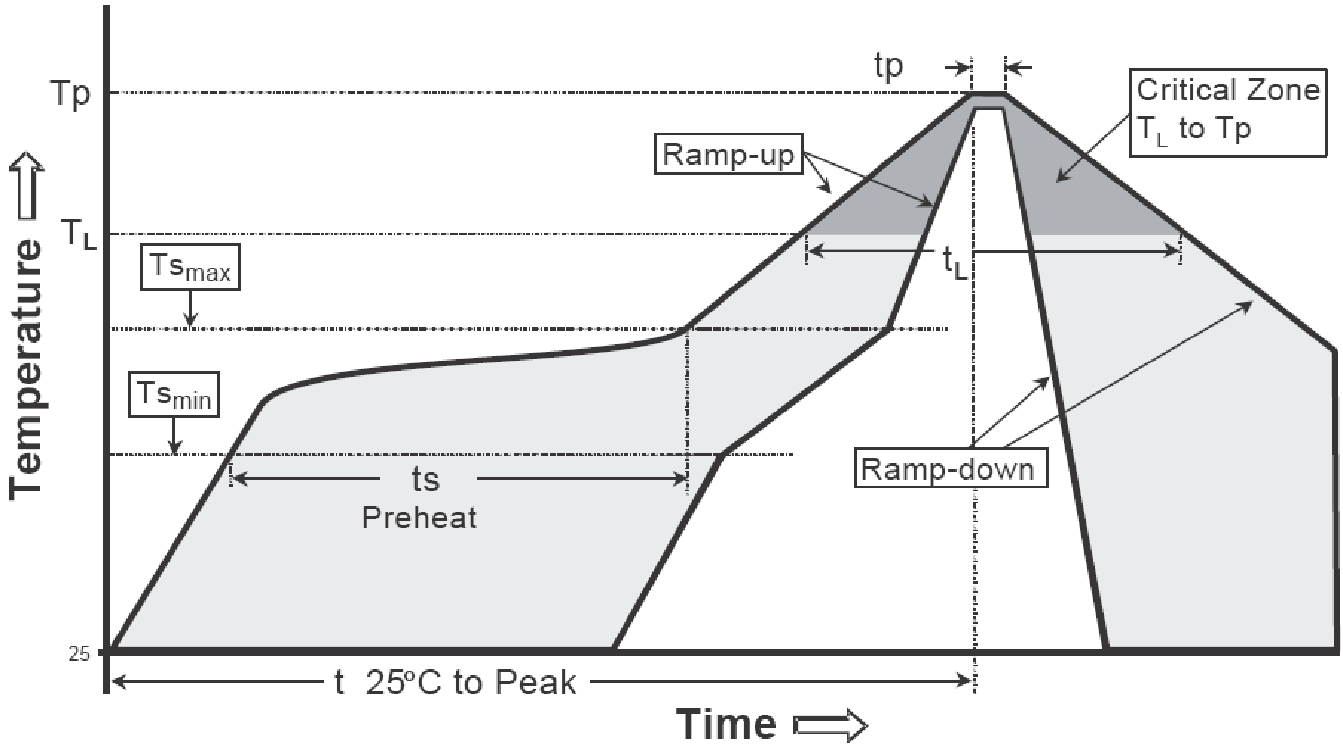
$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

Figure 19. Unclamped Inductive Switching Waveforms

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

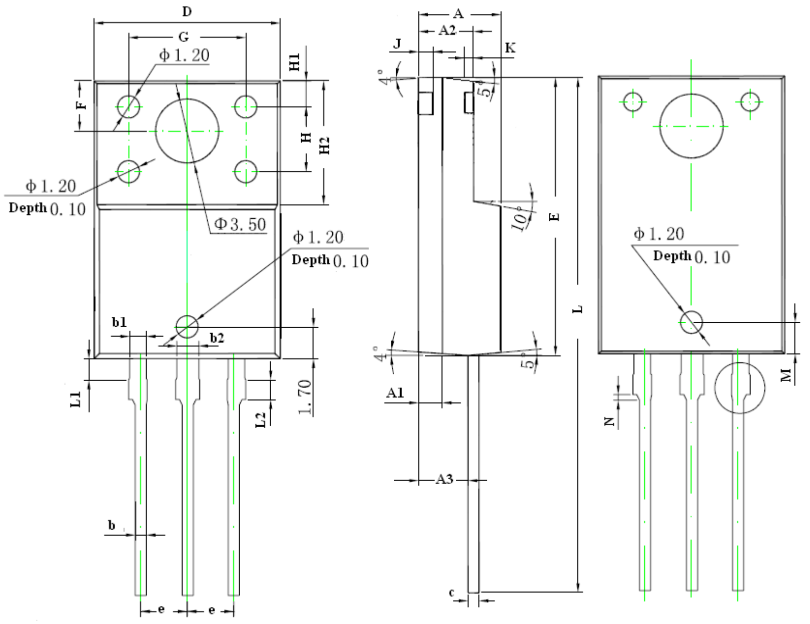
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(Ts min) −Temperature Max(Ts max) −Time(ts min to ts max)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: −Temperature (TL) − Time (tL)	183°C 60-150 seconds	217°C 60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

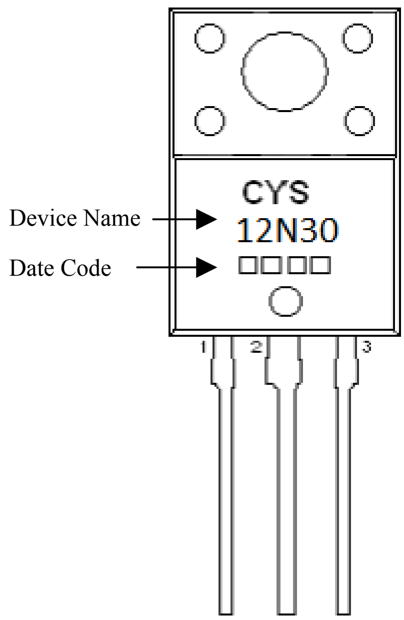
Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-220FP Dimension



3-Lead TO-220FP Plastic Package
CYStek Package Code: FP

Marking:



Style: Pin 1.Gate 2.Drain 3.Source

*Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.171	0.183	4.35	4.65	G	0.246	0.258	6.25	6.55
A1	0.051 REF		1.300 REF		H	0.138 REF		3.50 REF	
A2	0.112	0.124	2.85	3.15	H1	0.055 REF		1.40 REF	
A3	0.102	0.110	2.60	2.80	H2	0.256	0.272	6.50	6.90
b	0.020	0.030	0.50	0.75	J	0.031 REF		0.80 REF	
b1	0.031	0.041	0.80	1.05	K	0.020		0.50 REF	
b2	0.047 REF		1.20 REF		L	1.102	1.118	28.00	28.40
c	0.020	0.030	0.500	0.750	L1	0.043	0.051	1.10	1.30
D	0.396	0.404	10.06	10.26	L2	0.036	0.043	0.92	1.08
E	0.583	0.598	14.80	15.20	M	0.067 REF		1.70 REF	
e	0.100 *		2.54*		N	0.012 REF		0.30 REF	
F	0.106 REF		2.70 REF						

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice: