

N-Channel Enhancement Mode Power MOSFET

MTEE2N20FP

BV_{DSS}	200V
I_D	4A
R_{DS(ON)}@ V_{GS}=10V, I_D=2.9A	650 mΩ (typ)
R_{DS(ON)}@ V_{GS}=7V, I_D=1A	590 mΩ (typ)

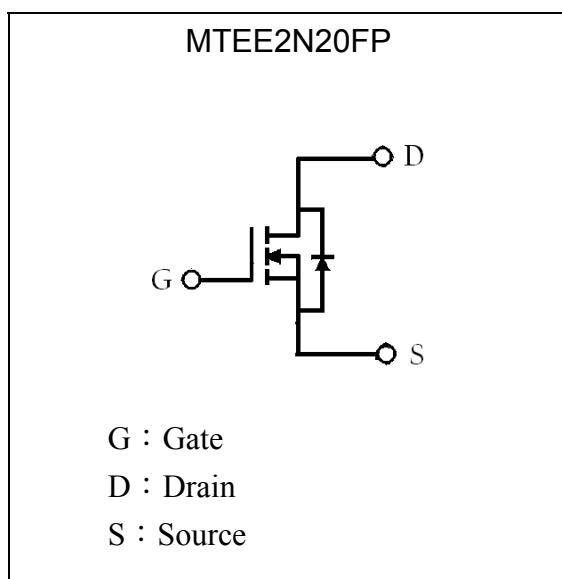
Description

The MTEE2N20FP is a N-channel enhancement-mode MOSFET, providing the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness. The TO-220FP package is universally preferred for all commercial-industrial applications

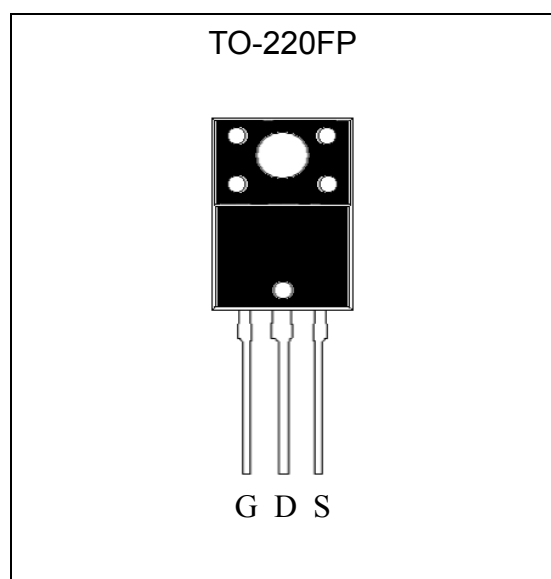
Features

- Low On Resistance
- Simple Drive Requirement
- Low Gate Charge
- Fast Switching Characteristic
- Insulating package, front/back side insulating voltage=2500V(AC)
- RoHS compliant package

Symbol



Outline



**Absolute Maximum Ratings** ($T_C=25^{\circ}\text{C}$)

Parameter	Symbol	Limits	Unit	
Drain-Source Voltage (Note 1)	V_{DS}	200	V	
Gate-Source Voltage	V_{GS}	± 30		
Continuous Drain Current @ $T_C=25^{\circ}\text{C}$, $V_{GS}=10\text{V}$ (Note 1)	I_D	4*	A	
Continuous Drain Current @ $T_C=100^{\circ}\text{C}$, $V_{GS}=10\text{V}$ (Note 1)		2.8*		
Continuous Drain Current @ $T_A=25^{\circ}\text{C}$, $V_{GS}=10\text{V}$ (Note 2)	I_{DSM}	1.2		
Continuous Drain Current @ $T_A=70^{\circ}\text{C}$, $V_{GS}=10\text{V}$ (Note 2)		0.9		
Pulsed Drain Current @ $V_{GS}=10\text{V}$ (Note 3)	I_{DM}	9*		
Avalanche Current (Note 3)	I_{AR}	2		
Single Pulse Avalanche Energy @ $L=10\text{mH}$, $I_D=2\text{Amps}$, $V_{DD}=50\text{V}$ (Note 2)	E_{AS}	20	mJ	
Repetitive Avalanche Energy (Note 3)	E_{AR}	2.5		
Power Dissipation	$T_C=25^{\circ}\text{C}$ (Note 1)	P_D	25	W
	$T_C=100^{\circ}\text{C}$ (Note 1)		12	
	$T_A=25^{\circ}\text{C}$ (Note 2)	P_{DSM}	2	
	$T_A=70^{\circ}\text{C}$ (Note 2)		1.3	
Maximum Temperature for Soldering @ Lead at 0.063 in(1.6mm) from case for 10 seconds	T_L	300	$^{\circ}\text{C}$	
Maximum Temperature for Soldering @ Package Body for 10 seconds	T_{PKG}	260		
Operating Junction and Storage Temperature	T_j, T_{stg}	-55~+175		

*Drain current limited by maximum junction temperature

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{\theta JC}$	6	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-ambient, max (Note 2)	$R_{\theta JA}$	62.5	$^{\circ}\text{C}/\text{W}$

- Note : 1. The power dissipation P_D is based on $T_{J(MAX)}=175^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
2. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2 oz. copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.
3. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=175^{\circ}\text{C}$. Ratings are based on low frequency and low duty cycles to keep initial $T_J=25^{\circ}\text{C}$.



Characteristics (Tj=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	200	-	-	V	V _{GS} =0V, I _D =250μA
ΔBV _{DSS} /ΔT _j	-	0.2	-	V/°C	Reference to 25°C, I _D =250μA
V _{GS(th)}	2.5	3.5	4.5	V	V _{DS} = V _{GS} , I _D =250μA
*G _{FS}	-	1	-	S	V _{DS} =40V, I _D =1A
I _{GSS}	-	-	±100	nA	V _{GS} =±30V
I _{DSS}	-	-	10	μA	V _{DS} =200V, V _{GS} =0V
I _{DSS}	-	-	100		V _{DS} =160V, V _{GS} =0V, T _j =125°C
*R _{DS(ON)}	-	650	800	mΩ	V _{GS} =10V, I _D =2.9A
	-	590	730		V _{GS} =7V, I _D =1A
Dynamic					
*Q _g	-	6.5	-	nC	V _{DD} =160V, I _D =4A, V _{GS} =10V
*Q _{gs}	-	1.3	-		
*Q _{gd}	-	3.3	-		
*t _{d(ON)}	-	9	-	ns	V _{DD} =100V, I _D =4A, V _{GS} =10V, R _G =25 Ω
*t _r	-	16	-		
*t _{d(OFF)}	-	15	-		
*t _f	-	13	-		
C _{iss}	-	232	-	pF	V _{GS} =0V, V _{DS} =25V, f=1MHz
C _{oss}	-	25	-		
C _{rss}	-	9.1	-		
Source-Drain Diode					
*I _S	-	-	2	A	
*I _{SM}	-	-	8		
*V _{SD}	-	0.77	1.2	V	I _S =1A, V _{GS} =0V
*t _{rr}	-	120	-	ns	V _{GS} =0, I _F =2A, dI/dt=100A/μs
*Q _{rr}	-	500	-	nC	

*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

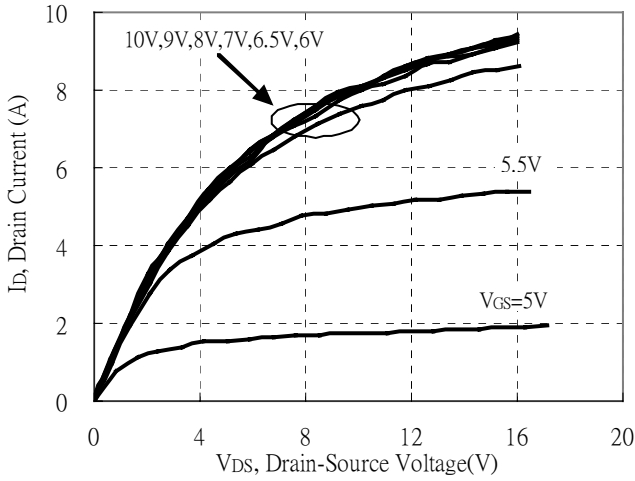
Ordering Information

Device	Package	Shipping
MTEE2N20FP-0-UB-S	TO-220FP (RoHS compliant)	50 pcs/tube, 20 tubes/box, 4 boxes / carton

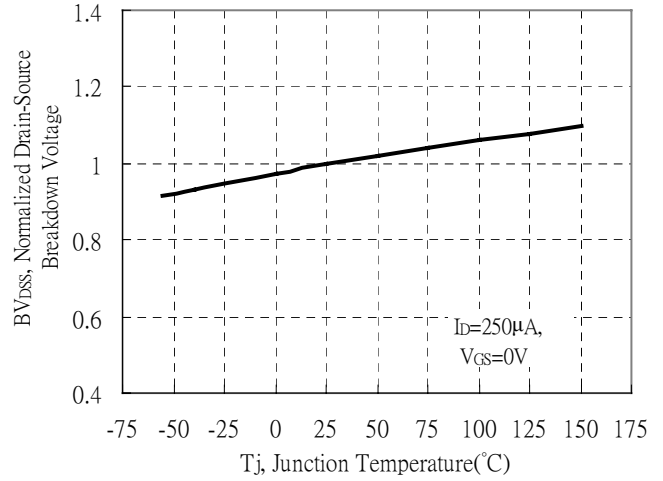


Typical Characteristics

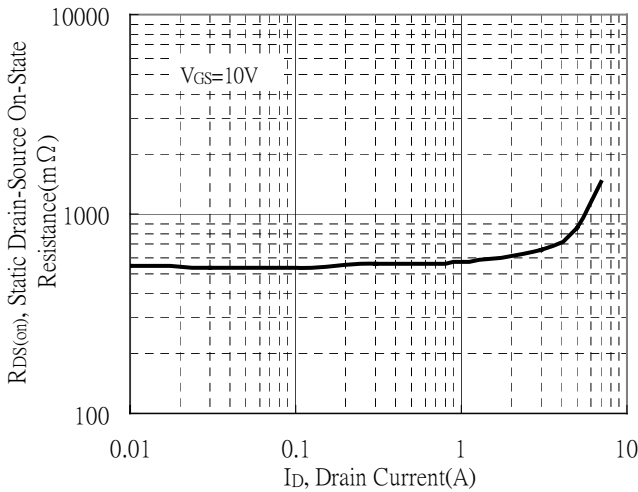
Typical Output Characteristics



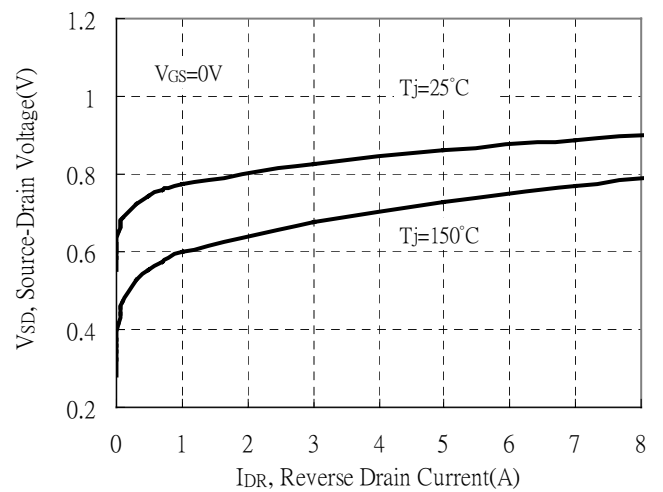
Brekdown Voltage vs Ambient Temperature



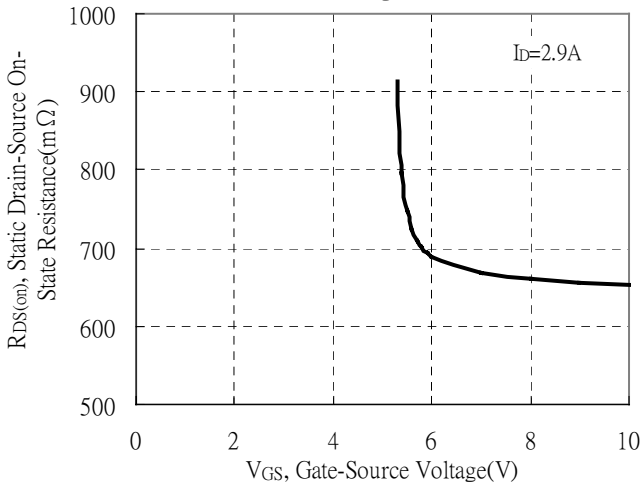
Static Drain-Source On-State resistance vs Drain Current



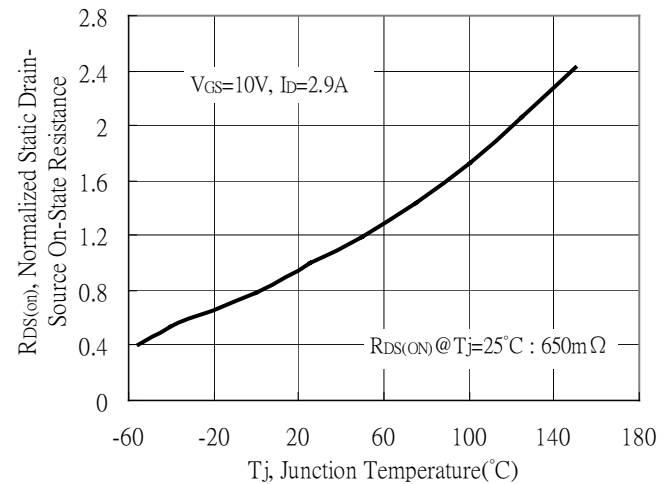
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

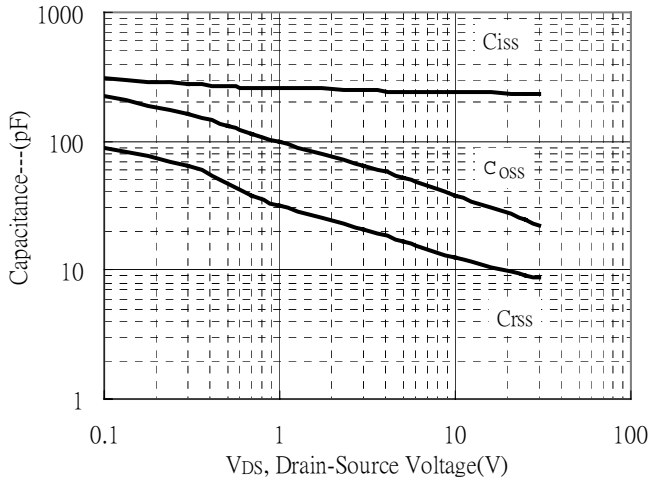


Drain-Source On-State Resistance vs Junction Temperature

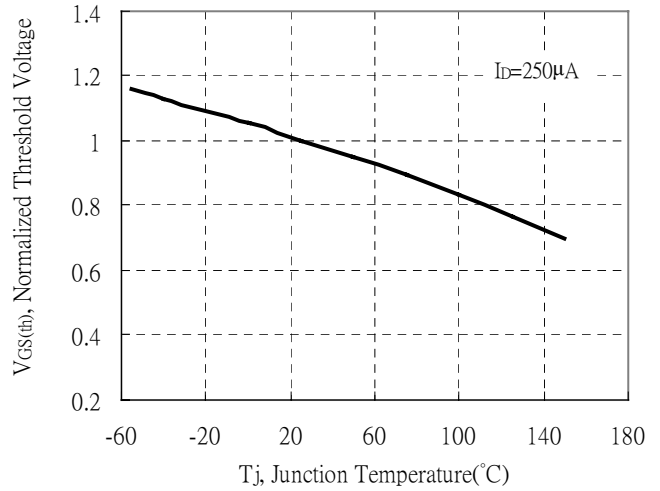


Typical Characteristics(Cont.)

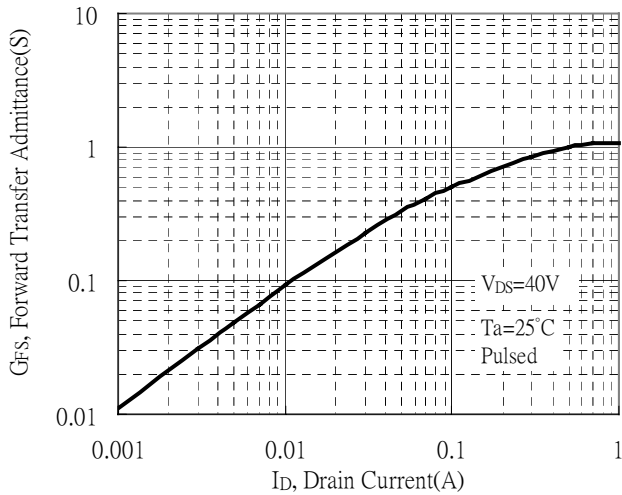
Capacitance vs Drain-to-Source Voltage



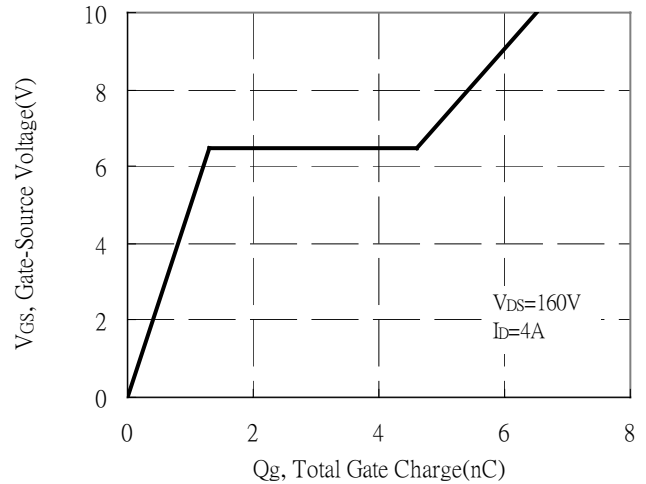
Threshold Voltage vs Junction Temperature



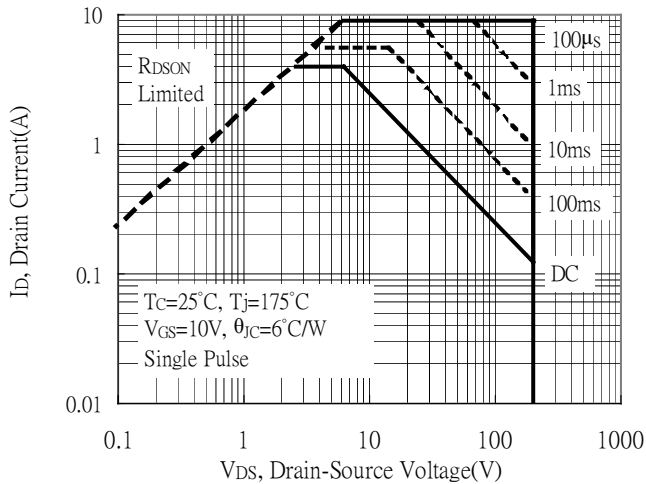
Forward Transfer Admittance vs Drain Current



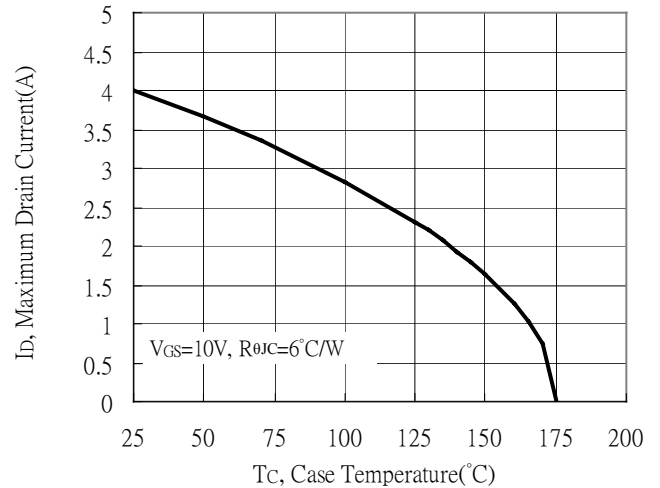
Gate Charge Characteristics



Maximum Safe Operating Area



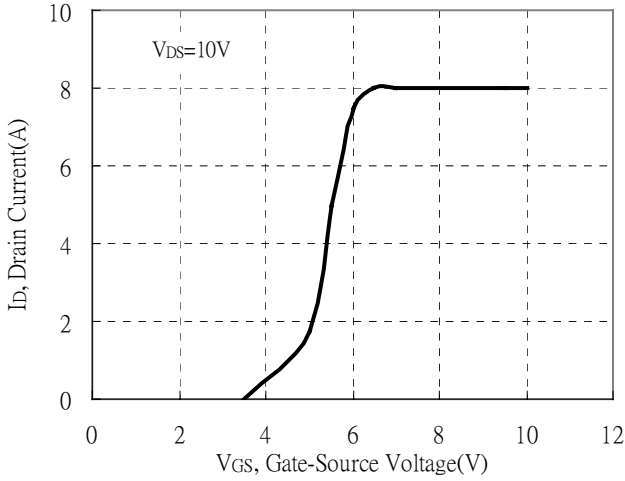
Maximum Drain Current vs Case Temperature



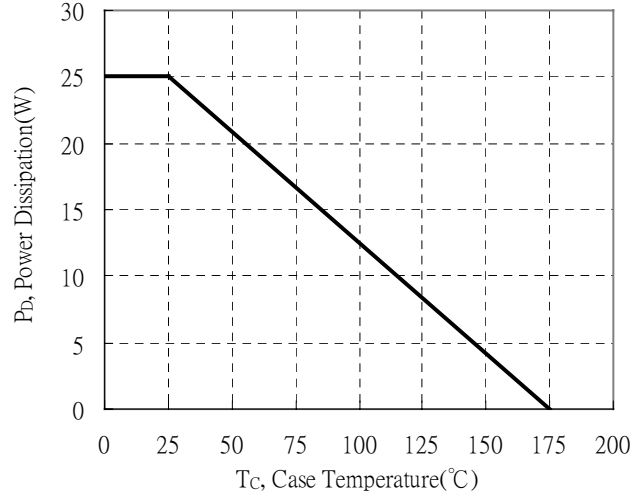


Typical Characteristics(Cont.)

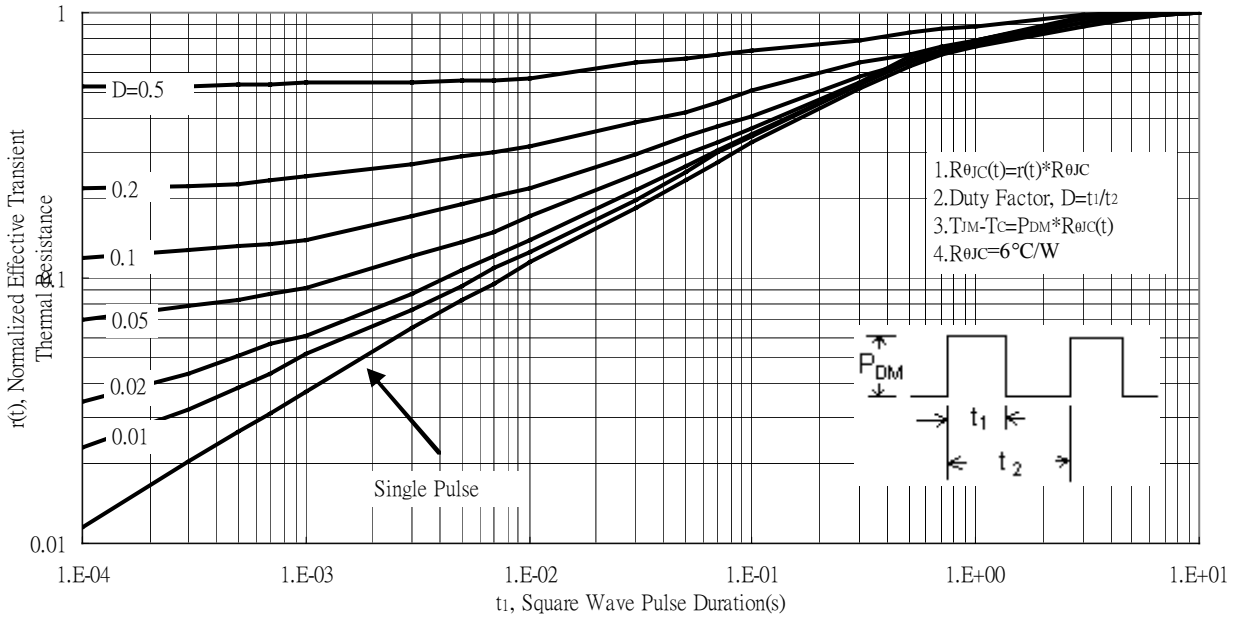
Typical Transfer Characteristics



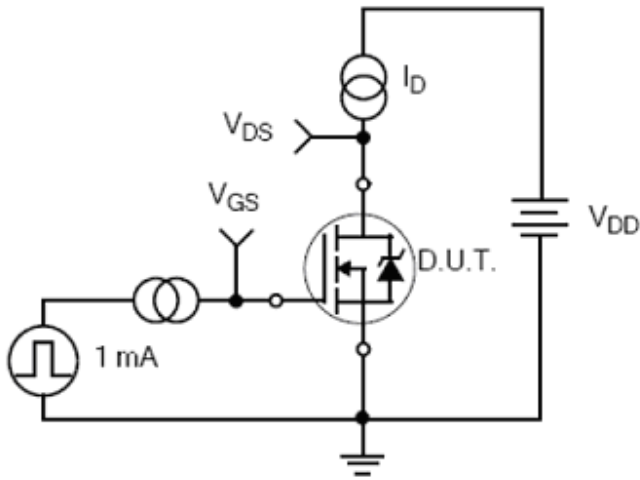
Power Derating Curve



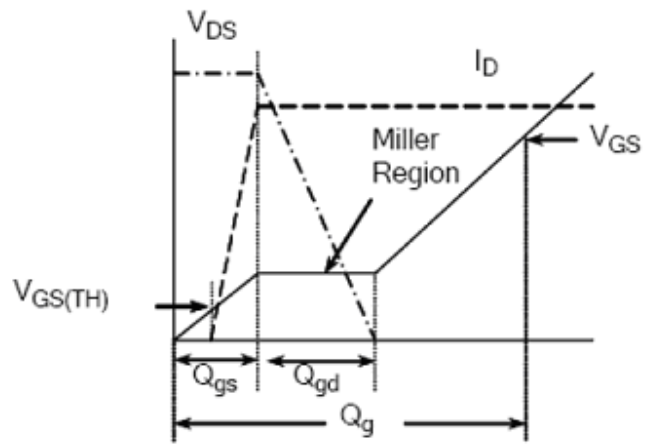
Transient Thermal Response Curves



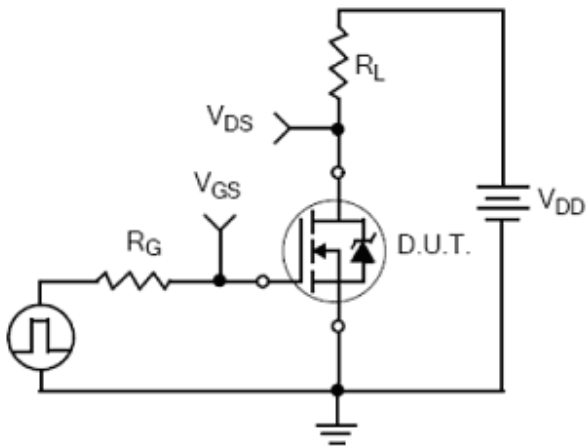
Test Circuit and Waveforms



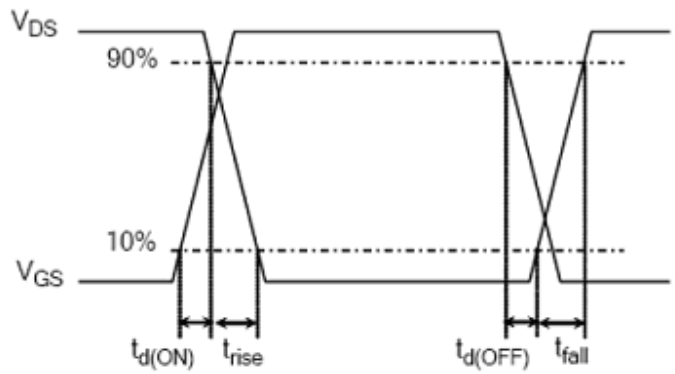
Gate Charge Test Circuit



Gate Charge Waveform

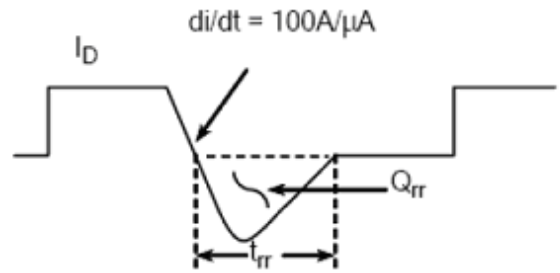
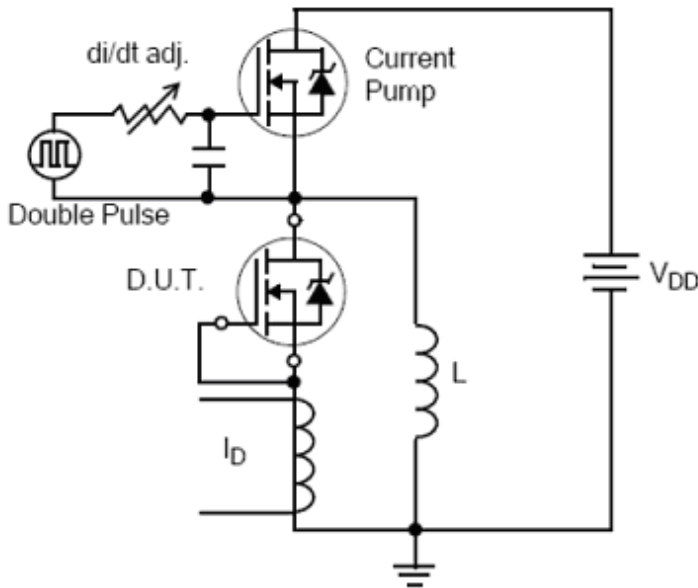


Resistive Switching Test Circuit



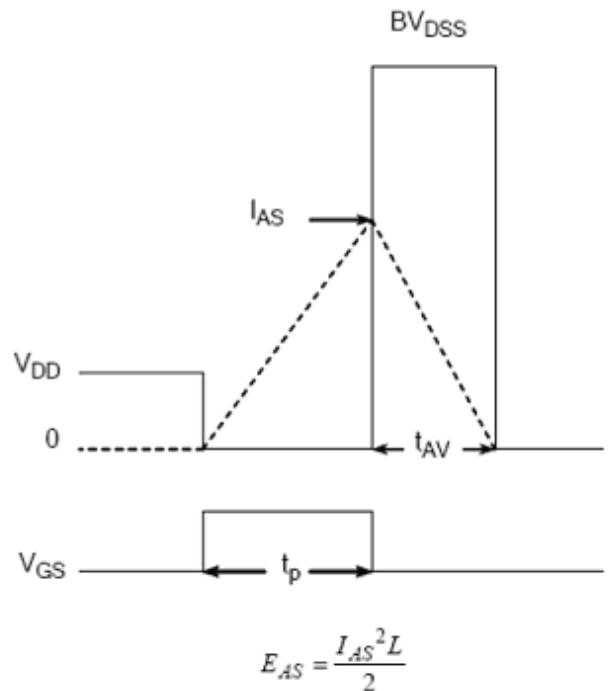
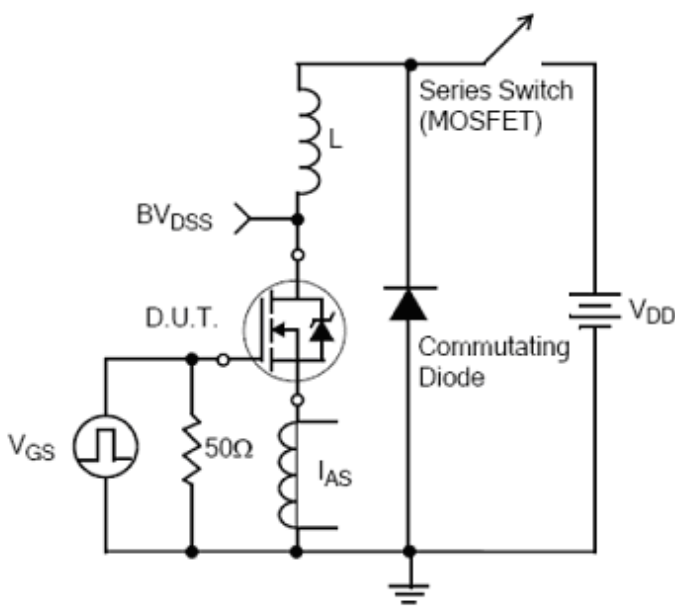
Resistive Switching Waveforms

Test Circuit and Waveforms(Cont.)



Diode Reverse Recovery Waveform

Diode Reverse Recovery Test Circuit



$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

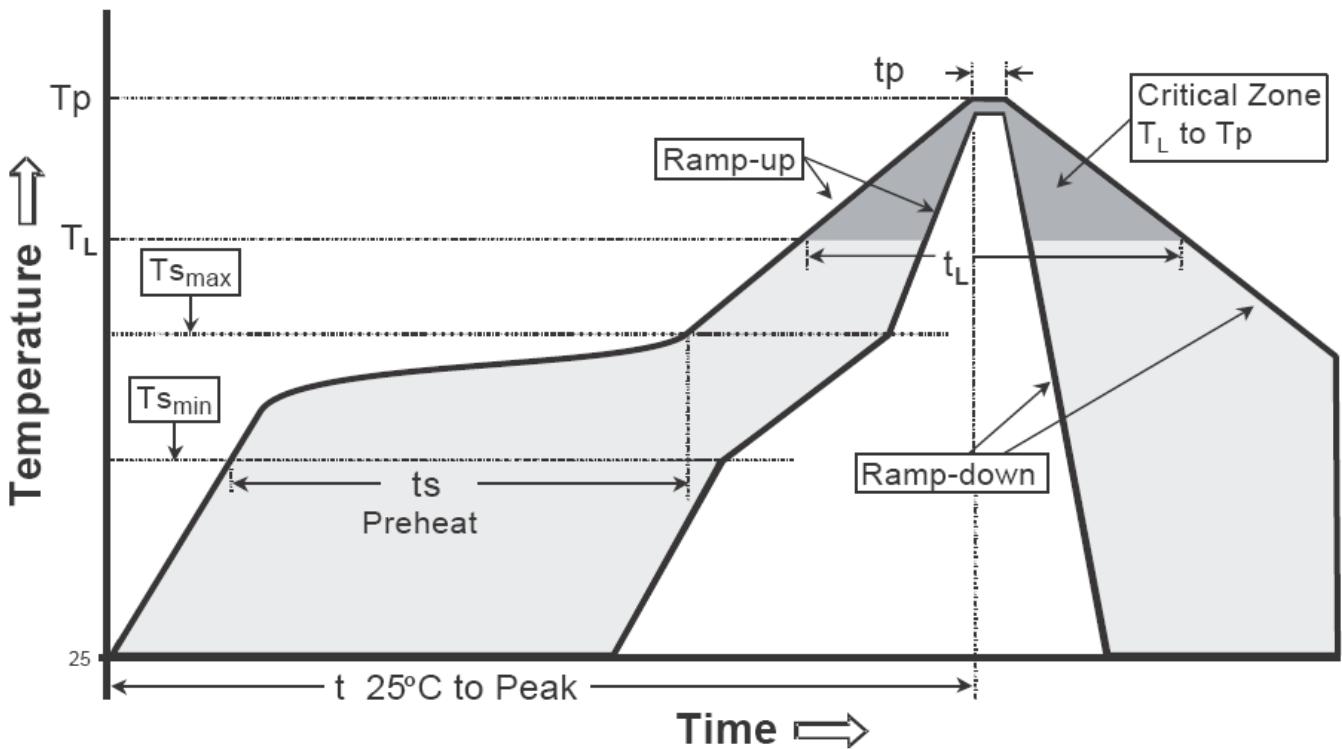
Unclamped Inductive Switching Test Circuit

Unclamped Inductive Switching Waveforms

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

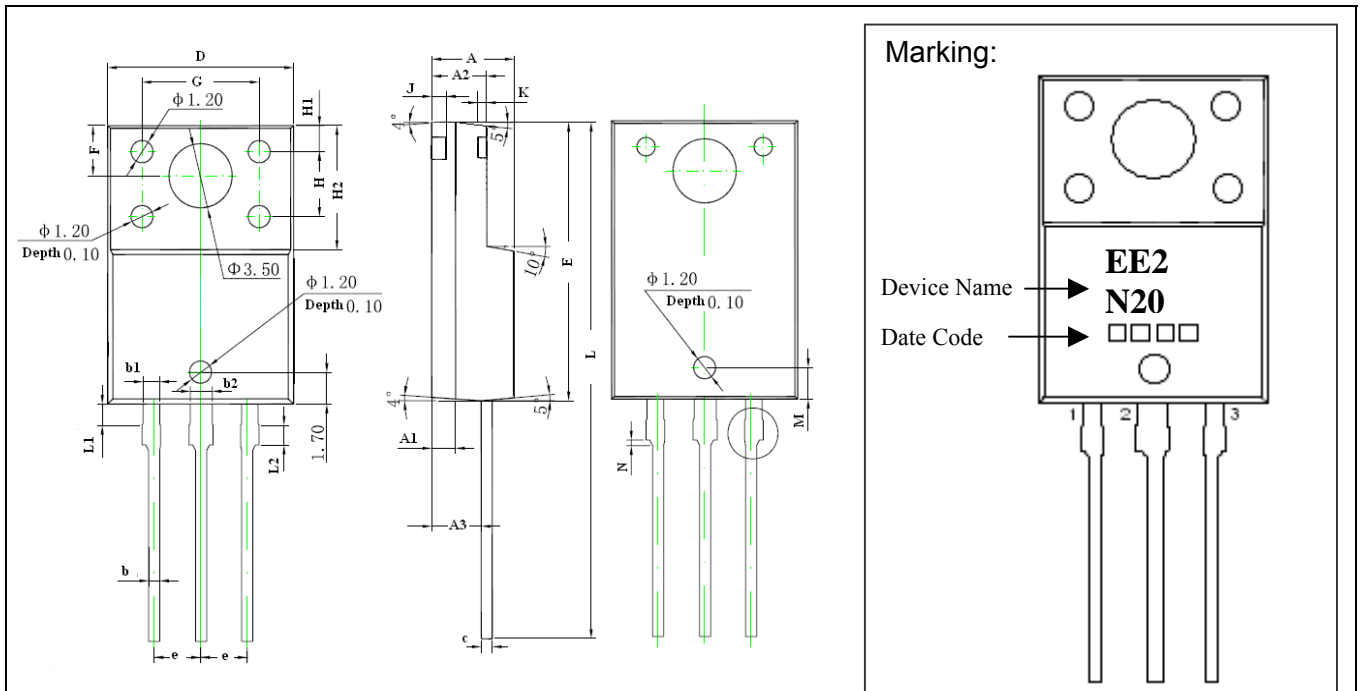
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-220FP Dimension



3-Lead TO-220FP Plastic Package
 CYStek Package Code: FP

Marking:

Device Name → **EE2**
 N20
 Date Code → □□□□

Style: Pin 1.Gate 2.Drain 3.Source

*Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.171	0.183	4.35	4.65	G	0.246	0.258	6.25	6.55
A1	0.051 REF		1.300 REF		H	0.138 REF	3.50 REF		
A2	0.112	0.124	2.85	3.15	H1	0.055 REF	1.40 REF		
A3	0.102	0.110	2.60	2.80	H2	0.256	0.272	6.50	6.90
b	0.020	0.030	0.50	0.75	J	0.031 REF		0.80 REF	
b1	0.031	0.041	0.80	1.05	K	0.020		0.50 REF	
b2	0.047 REF		1.20 REF		L	1.102	1.118	28.00	28.40
c	0.020	0.030	0.500	0.750	L1	0.043	0.051	1.10	1.30
D	0.396	0.404	10.06	10.26	L2	0.036	0.043	0.92	1.08
E	0.583	0.598	14.80	15.20	M	0.067 REF		1.70 REF	
e	0.100 *		2.54*		N	0.012 REF		0.30 REF	
F	0.106 REF		2.70 REF						

- Notes:** 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.