

N-Channel Enhancement Mode Power MOSFET

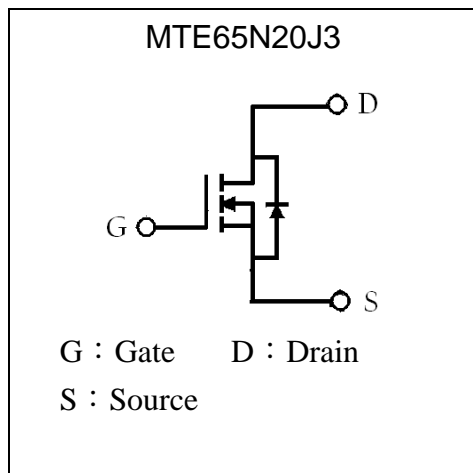
MTE65N20J3

BV_{DSS}	200V	
$I_D@V_{GS}=10V, T_C=25^\circ C$	25A	
$R_{DS(on)(TYP)}$	$V_{GS}=10V, I_D=11A$	61mΩ
	$V_{GS}=6V, I_D=5A$	66mΩ

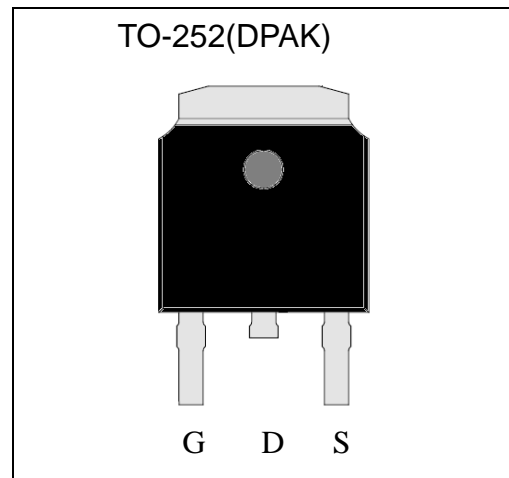
Features

- Low Gate Charge
- Simple Drive Requirement
- Pb-free lead plating and halogen-free package

Equivalent Circuit

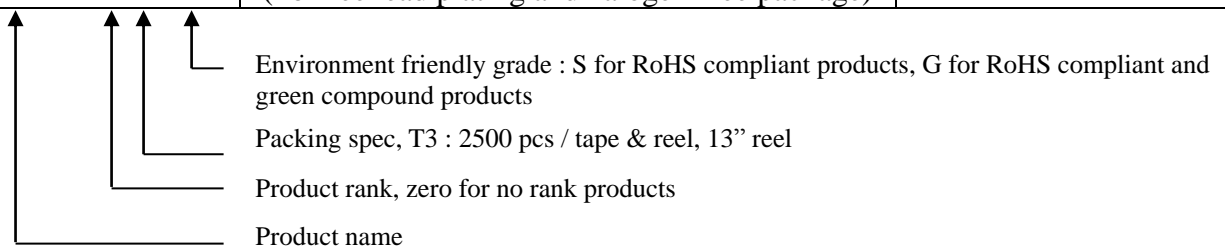


Outline



Ordering Information

Device	Package	Shipping
MTE65N20J3-0-T3-X	TO-252 (Pb-free lead plating and halogen-free package)	2500 pcs / Tape & Reel





Absolute Maximum Ratings (Tc=25°C, unless otherwise noted)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V _{DS}	200	V
Gate-Source Voltage	V _{GS}	±20	
Continuous Drain Current @ T _C =25°C, V _{GS} =10V	I _D	25	A
Continuous Drain Current @ T _C =100°C, V _{GS} =10V		18	
Pulsed Drain Current *1	I _{DM}	60	
Avalanche Current	I _{AS}	20	
Avalanche Energy @ L=1.6mH, I _D =20A, R _G =25Ω	E _{AS}	320	mJ
Repetitive Avalanche Energy @ L=0.1mH (Note 2)	E _{AR}	4.6	
Total Power Dissipation @ T _C =25°C	P _d	107	W
Total Power Dissipation @ T _A =25°C		1.14	
Operating Junction and Storage Temperature Range	T _j , T _{stg}	-55~+175	°C

Note : *1. Pulse width limited by maximum junction temperature
 *2. Duty cycle ≤ 1%

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	R _{th,j-c}	1.4	°C/W
Thermal Resistance, Junction-to-ambient, max	R _{th,j-a}	110	

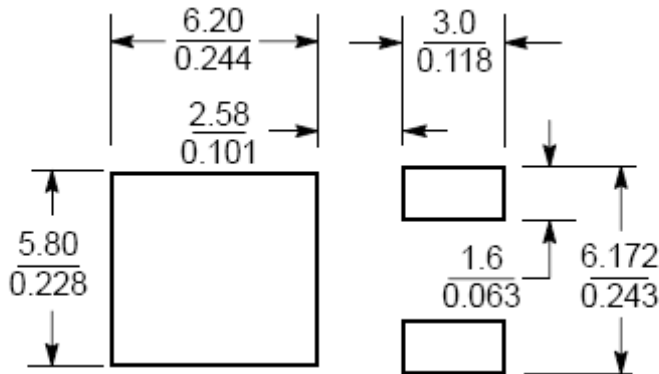
Characteristics (Tc=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	200	-	-	V	V _{GS} =0V, I _D =250μA
V _{GS(th)}	2	-	4		V _{DS} =V _{GS} , I _D =250μA
I _{GSS}	-	-	±100	nA	V _{GS} =±20V, V _{DS} =0V
I _{DSS}	-	-	1	μA	V _{DS} =180V, V _{GS} =0V
	-	-	25		V _{DS} =180V, V _{GS} =0V, T _J =125°C
R _{DS(ON)} *1	-	61	80	mΩ	V _{GS} =10V, I _D =11A
	-	66	100		V _{GS} =6V, I _D =5A
G _{FS} *1	-	15	-	S	V _{DS} =15V, I _D =11A
Dynamic					
Q _g *1,2	-	60	-	nC	V _{DS} =160V, I _D =25A, V _{GS} =10V
Q _{gs} *1,2	-	12.1	-		
Q _{gd} *1,2	-	24.2	-		
t _{d(ON)} *1,2	-	62	-	ns	V _{DS} =100V, I _D =20A, V _{GS} =10V,
t _r *1,2	-	62	-		

$t_{d(OFF)}$ *1, 2	-	200	-		$R_G=25\ \Omega$
t_f *1, 2	-	100	-		
C_{iss}	-	2447	-	pF	$V_{GS}=0V, V_{DS}=25V, f=1MHz$
C_{oss}	-	180	-		
C_{rss}	-	102	-		
Source-Drain Diode					
I_S *1	-	-	20	A	
I_{SM} *3	-	-	40		
V_{SD} *1	-	0.82	1.3	V	$I_F=I_S, V_{GS}=0V$
t_{rr}	-	120	-	ns	$I_F=20A, dI_F/dt=100A/\mu s$
Q_{rr}	-	400	-	nC	

Note : *1.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
 *2.Independent of operating temperature
 *3.Pulse width limited by maximum junction temperature.

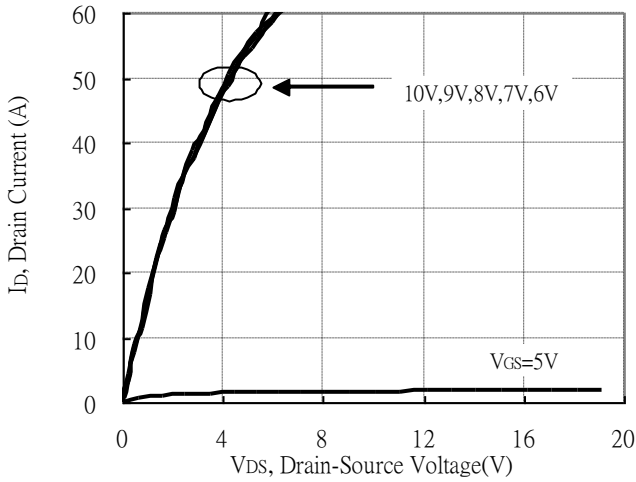
Recommended soldering footprint



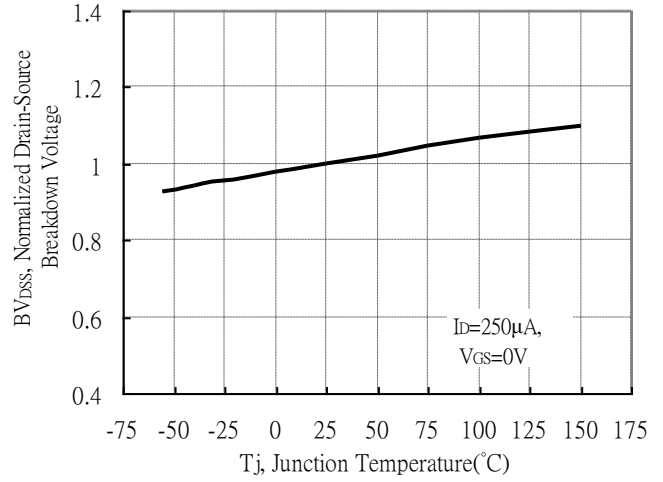
Unit ($\frac{mm}{inch}$)

Typical Characteristics

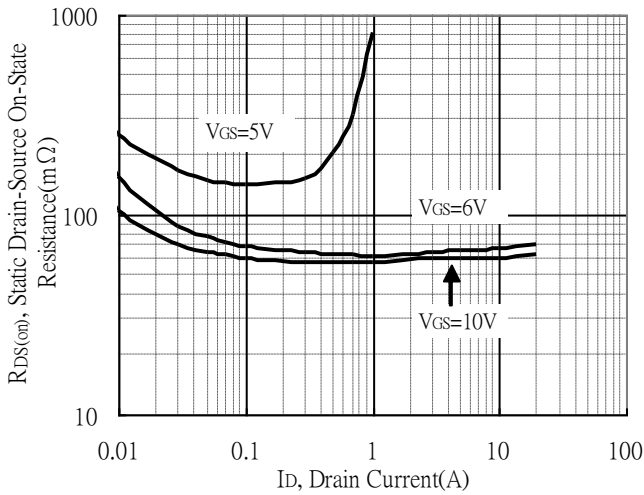
Typical Output Characteristics



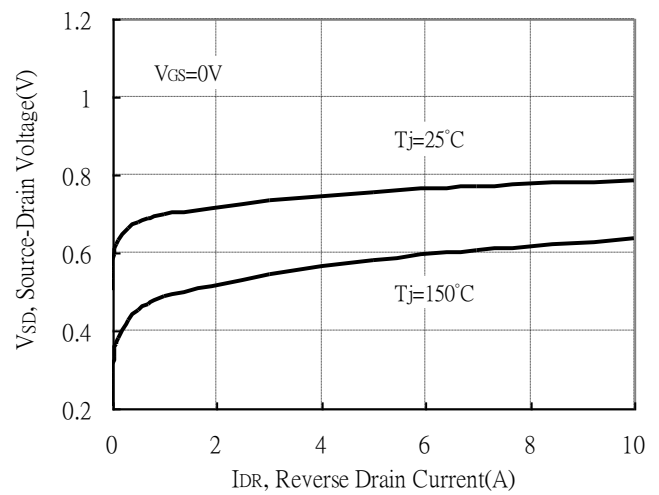
Brekdown Voltage vs Ambient Temperature



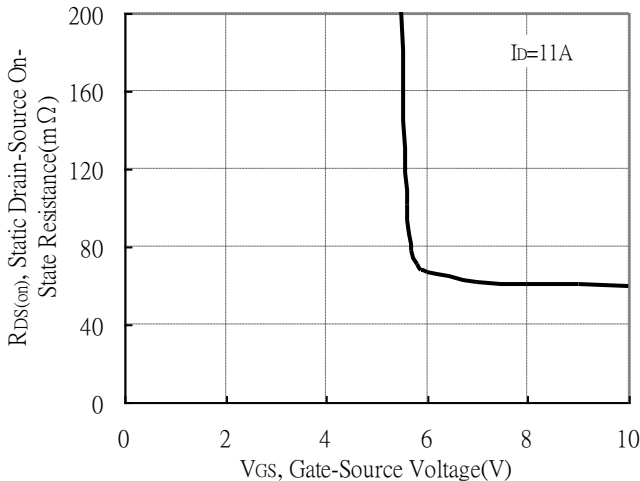
Static Drain-Source On-State resistance vs Drain Current



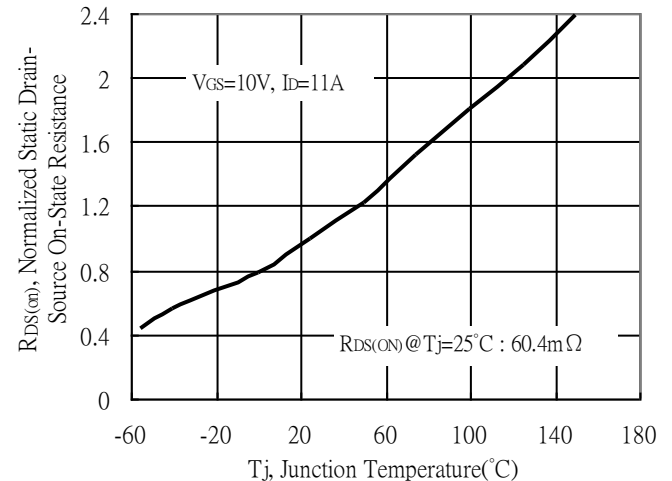
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

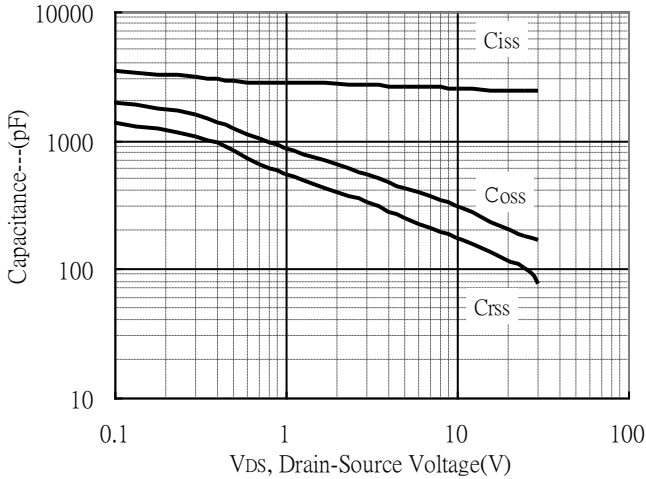


Drain-Source On-State Resistance vs Junction Temperature

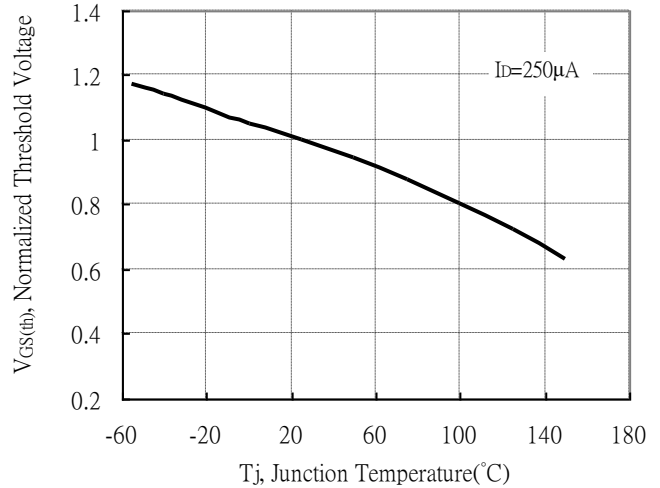


Typical Characteristics(Cont.)

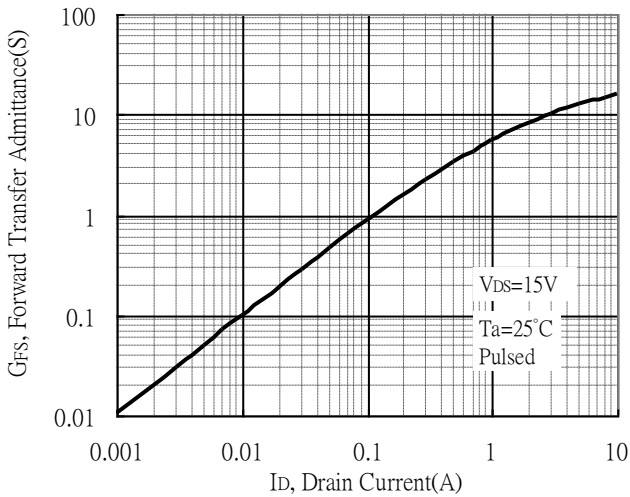
Capacitance vs Drain-to-Source Voltage



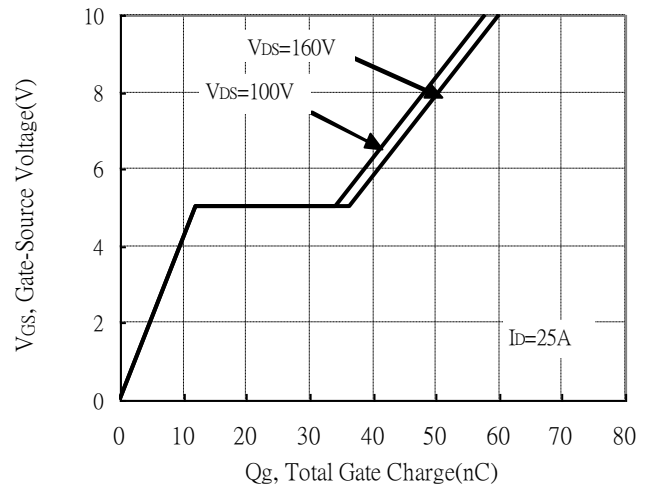
Threshold Voltage vs Junction Temperature



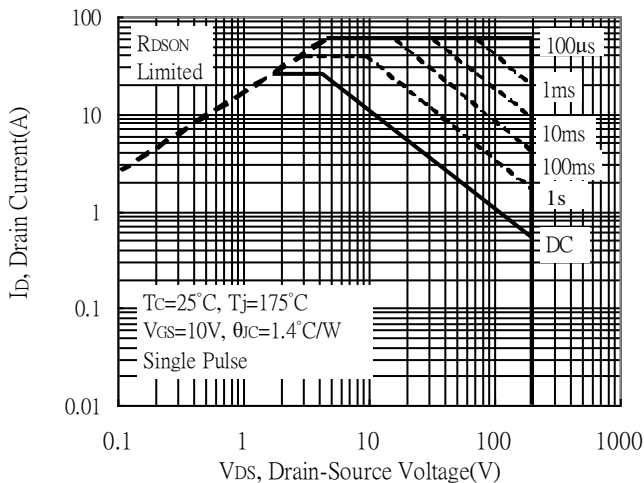
Forward Transfer Admittance vs Drain Current



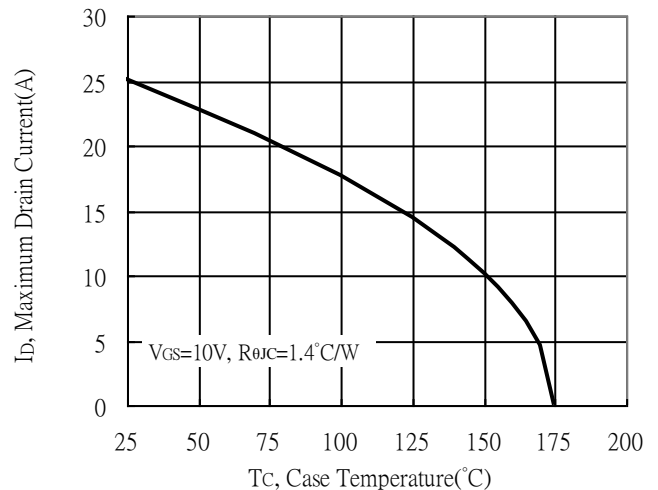
Gate Charge Characteristics



Maximum Safe Operating Area



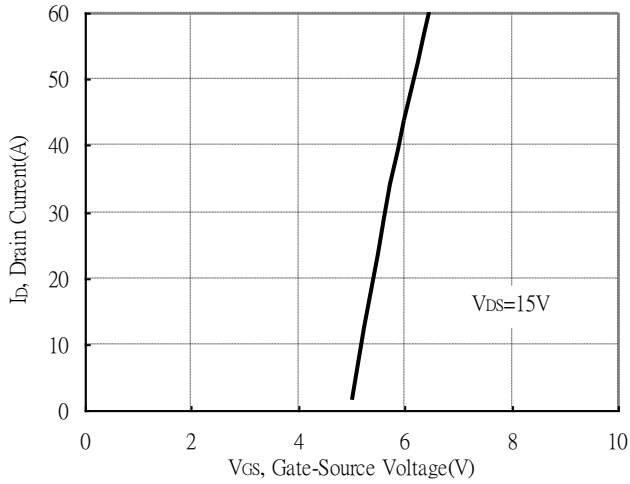
Maximum Drain Current vs Case Temperature



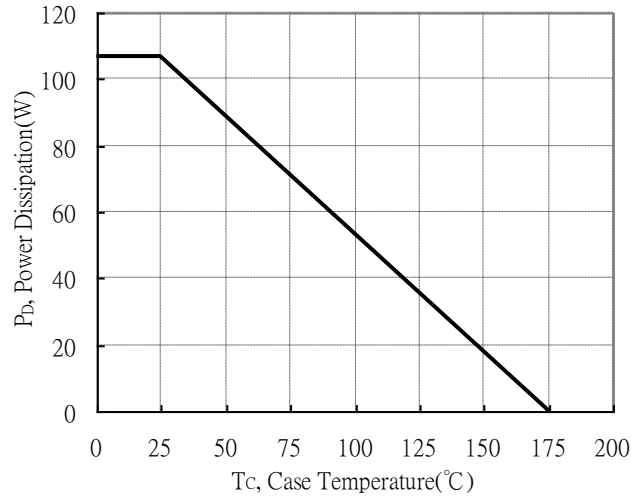


Typical Characteristics(Cont.)

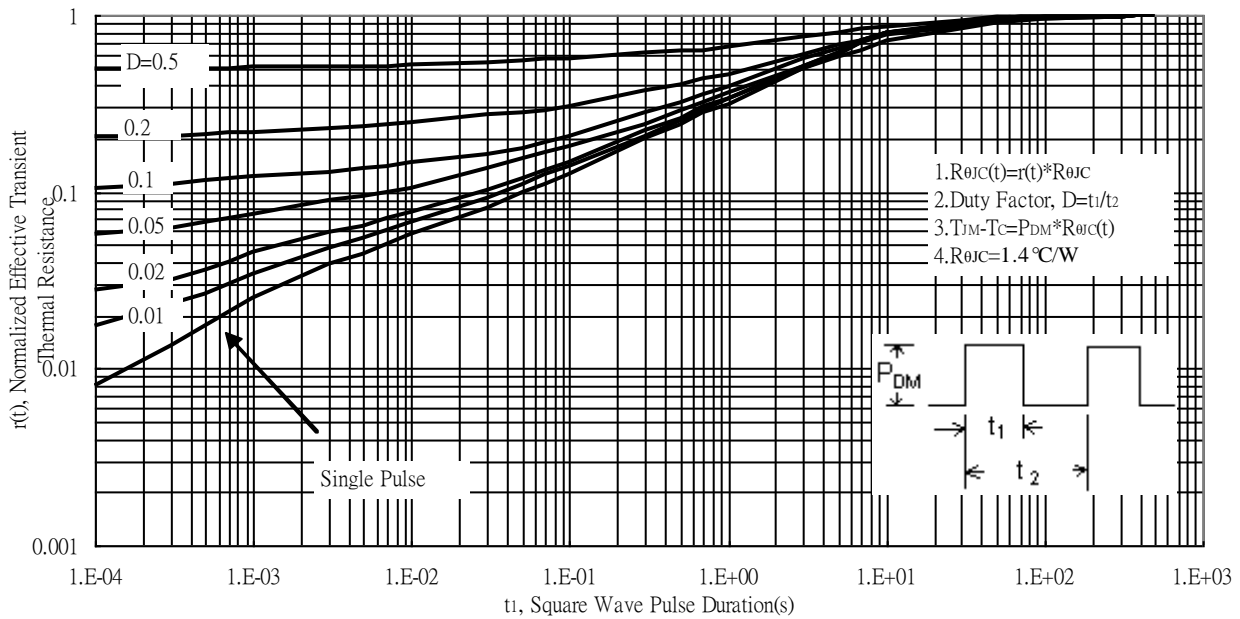
Typical Transfer Characteristics



Power Derating Curve



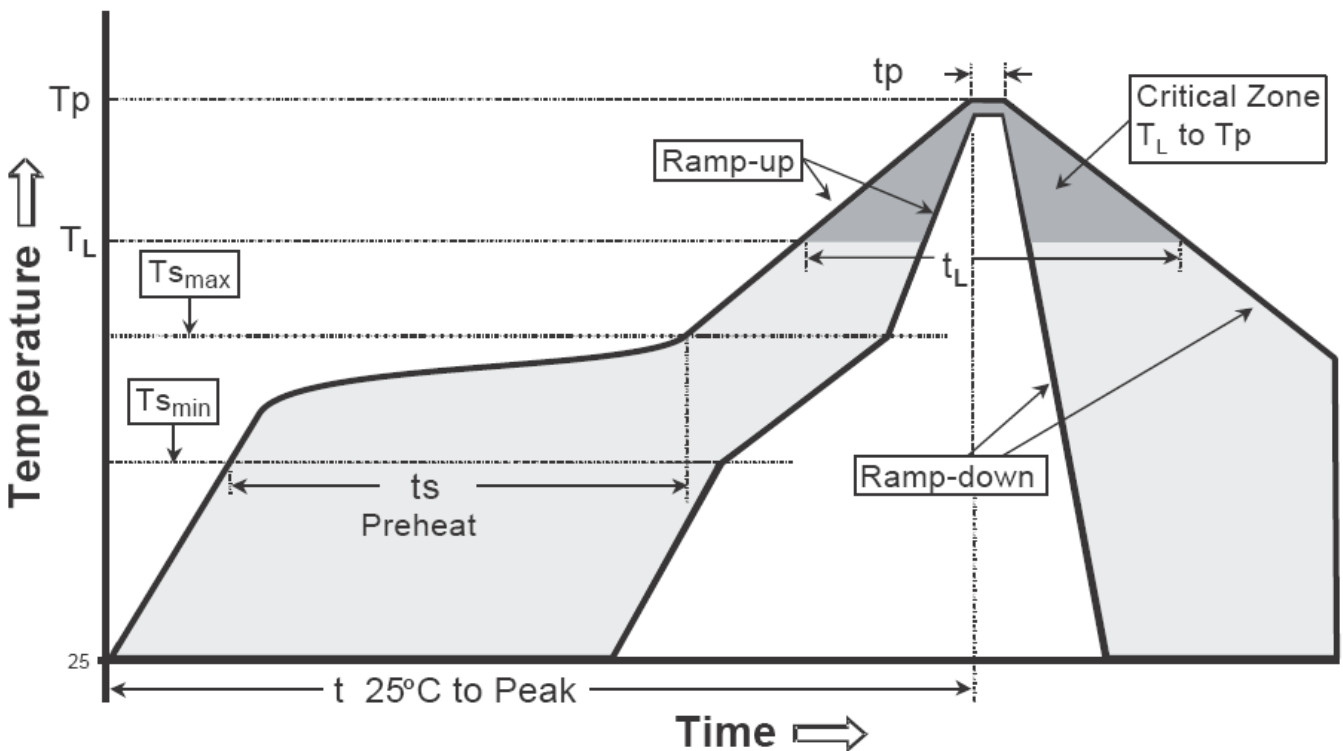
Transient Thermal Response Curves



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

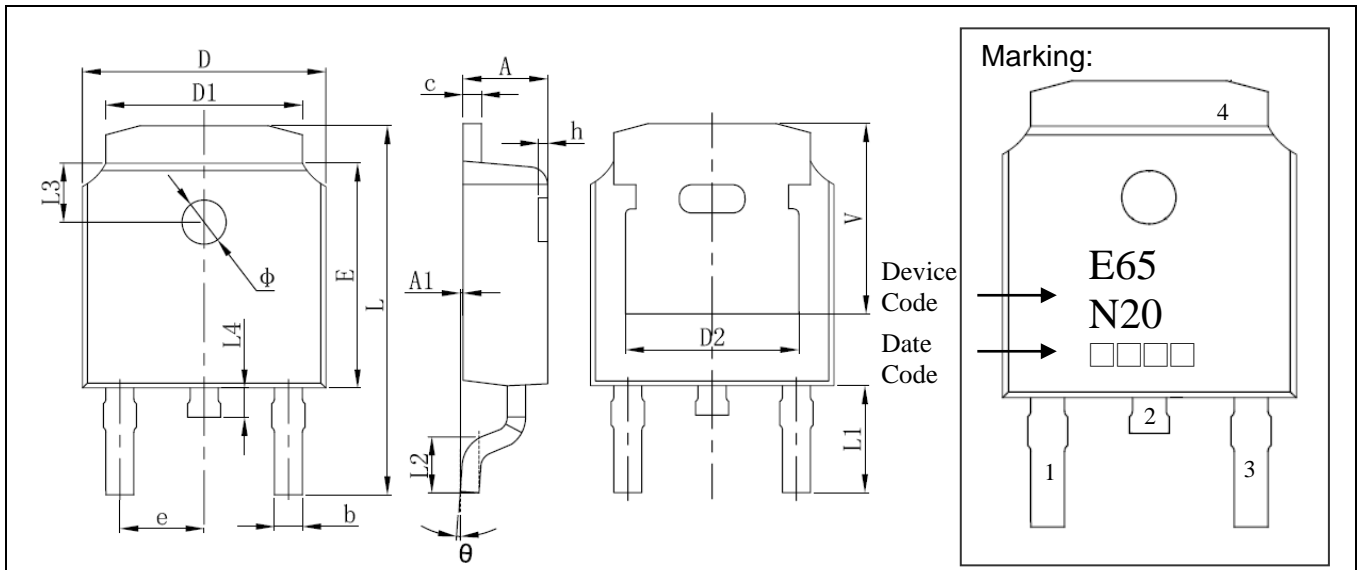
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-252 Dimension



3-Lead TO-252 Plastic Surface Mount Package
 CYStek Package Code: J3

Style: Pin 1.Gate 2.Drain 3.Source 4.Drain

Date Code :
 First Code : Last digit of Christian Year
 Second Code : Month Code : Jan→A, Feb→B, Mar→C, Apr→D, May→E, Jun→F, Jul→G,
 Aug→H, Sep→J, Oct→K, Nov→L, Dec→M
 Last Two Codes : Production Serial Code, 01~99

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.087	0.094	2.200	2.400	L	0.382	0.406	9.712	10.312
A1	0.000	0.005	0.000	0.127	L1	0.114	REF	2.900	REF
b	0.025	0.030	0.635	0.770	L2	0.055	0.067	1.400	1.700
c	0.018	0.023	0.460	0.580	L3	0.063	REF	1.600	REF
D	0.256	0.264	6.500	6.700	L4	0.024	0.039	0.600	1.000
D1	0.201	0.215	5.100	5.460	Φ	0.043	0.051	1.100	1.300
D2	0.190	REF	4.830	REF	θ	0°	8°	0°	8°
E	0.236	0.244	6.000	6.200	h	0.000	0.012	0.000	0.300
e	0.086	0.094	2.186	2.386	v	0.207	REF	5.250	REF

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead : Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.