

N-Channel Enhancement Mode Power MOSFET

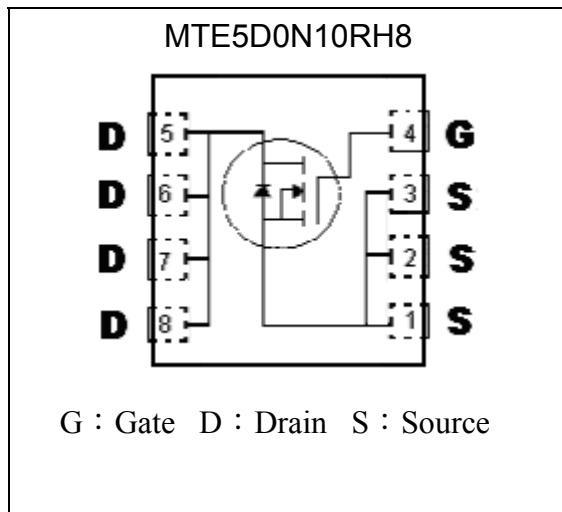
MTE5D0N10RH8

BV_{DSS}	100V
$I_D@V_{GS}=10V, T_C=25^\circ C$	81A
$I_D@V_{GS}=10V, T_A=25^\circ C$	21A
$R_{DS(on)(TYP)}$ $V_{GS}=10V, I_D=30A$	6mΩ

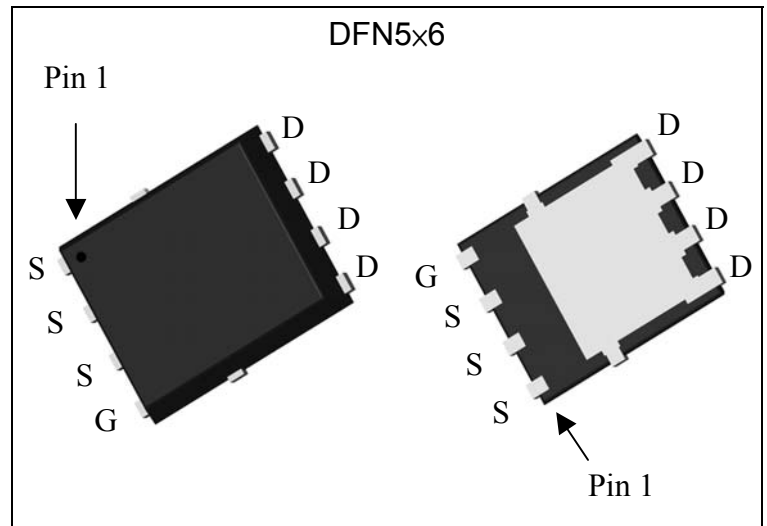
Features

- Simple Drive Requirement
- Low On-resistance
- Fast Switching Characteristic
- Pb-free lead plating and Halogen-free package

Symbol

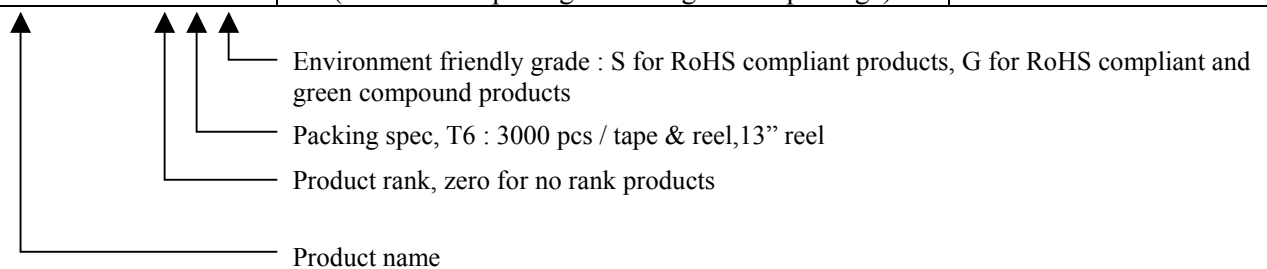


Outline



Ordering Information

Device	Package	Shipping
MTE5D0N10RH8-0-T6-G	DFN 5 × 6 (Pb-free lead plating and halogen-free package)	3000 pcs / tape & reel



**Absolute Maximum Ratings** (Ta=25°C)

Parameter	Symbol	10s	Steady State	Unit	
Drain-Source Voltage	V _{DS}	100		V	
Gate-Source Voltage	V _{GS}	±20			
Continuous Drain Current @ T _C =25°C, V _{GS} =10V (Note 1)	I _D	81		A	
Continuous Drain Current @ T _C =100°C, V _{GS} =10V (Note 1)		57.3			
Continuous Drain Current @ T _A =25°C, V _{GS} =10V (Note 2)	I _{DSM}	21	14		
Continuous Drain Current @ T _A =70°C, V _{GS} =10V (Note 2)		17.6	11.7		
Continuous Drain Current @ T _A =85°C, V _{GS} =10V (Note 2)		16.3	10.8		
Pulsed Drain Current (Note 3)		I _{DM}	324 *1		
Avalanche Current @ L=0.1mH (Note 3)	I _{AS}	90			mJ
Avalanche Energy @ L=1mH, I _D =36A, V _{DD} =50V (Note 4)	E _{AS}	648			
Repetitive Avalanche Energy @ L=0.05mH (Note 3)	E _{AR}	5 *2			
Total Power Dissipation	P _D	T _C =25°C (Note 1)	100		W
		T _C =100°C (Note 1)	50		
	P _{DSM}	T _A =25°C (Note 2)	6.8	3	
		T _A =70°C (Note 2)	4.8	2.1	
		T _A =85°C (Note 2)	4.1	1.8	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55~+175		°C	

Thermal Data

Parameter	Symbol	Typical	Maximum	Unit	
Thermal Resistance, Junction-to-ambient (Note 2)	R _{θJA}	t≤10s	18	22	°C/W
		Steady State	42	50	
Thermal Resistance, Junction-to-case	R _{θJC}	1.3	1.5		

- Note : 1. The power dissipation P_D is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
2. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2 oz. copper, in a still air environment with T_A=25°C. The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 175°C. The value in any given application depends on the user's specific board design.
3. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175°C. Ratings are based on low frequency and low duty cycles to keep initial T_J=25°C.
4. 100% tested by conditions of L=0.1mH, I_{AS}=30A, V_{GS}=10V, V_{DD}=50V



Characteristics (Tc=25°C, unless otherwise specified)

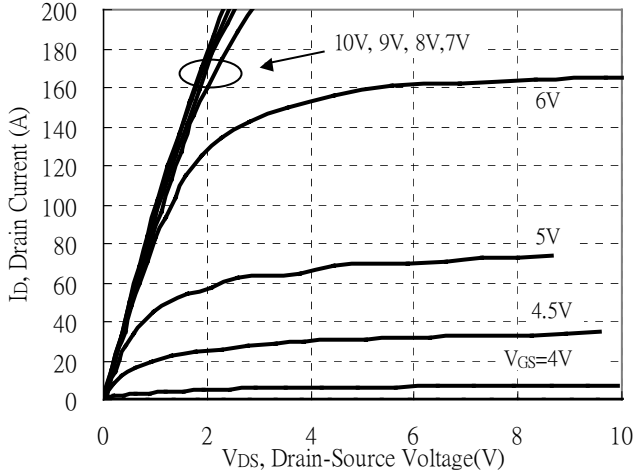
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	100	-	-	V	V _{GS} =0V, I _D =250μA
V _{GS(th)}	2	-	4		V _{DS} = V _{GS} , I _D =250μA
G _{FS} *1	-	30.9	-	S	V _{DS} =10V, I _D =20A
I _{GSS}	-	-	±100	nA	V _{GS} =±20V, V _{DS} =0V
I _{DSS}	-	-	1	μA	V _{DS} =80V, V _{GS} =0V
	-	-	25		V _{DS} =80V, V _{GS} =0V, T _j =125°C
R _{DS(ON)} *1	-	6	8.2	mΩ	V _{GS} =10V, I _D =30A
Dynamic					
C _{iss}	-	4829	6278	pF	V _{GS} =0V, V _{DS} =50V, f=1MHz
C _{oss}	-	504	655		
C _{rss}	-	22	33		
Q _g *1, 2	-	66.7	87	nC	V _{DS} =80V, V _{GS} =10V, I _D =30A
Q _{gs} *1, 2	-	21	-		
Q _{gd} *1, 2	-	13	-		
t _{d(ON)} *1, 2	-	33.6	-	ns	V _{DD} =50V, I _D =30A, V _{GS} =10V, R _G =1 Ω
t _r *1, 2	-	20.4	-		
t _{d(OFF)} *1, 2	-	63.2	-		
t _f *1, 2	-	13	-		
R _g	-	2.1	-	Ω	f=1MHz
Source-Drain Diode					
I _S *1	-	-	81	A	
I _{SM} *3	-	-	324		
V _{SD} *1	-	0.81	1.2	V	I _S =20A, V _{GS} =0V
t _{rr}	-	45.9	60	ns	I _F =20A, dI _F /dt=100A/μs
Q _{rr}	-	87.8	-	nC	
I _{RRM}	-	3.5	-	A	

Note : *1.Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%
 *2.Independent of operating temperature
 *3.Pulse width limited by maximum junction temperature.

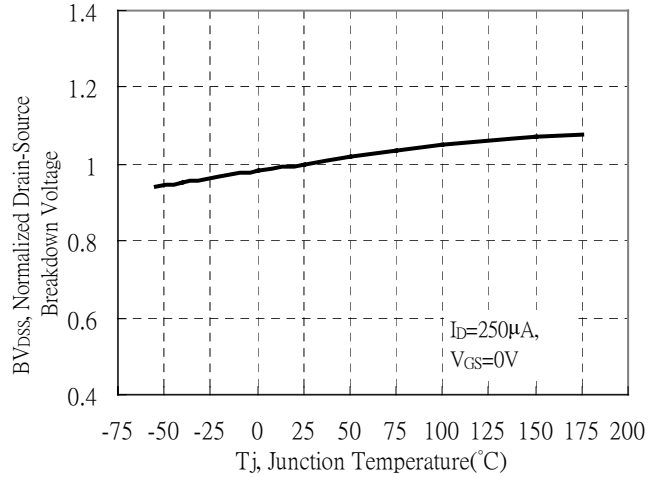


Typical Characteristics

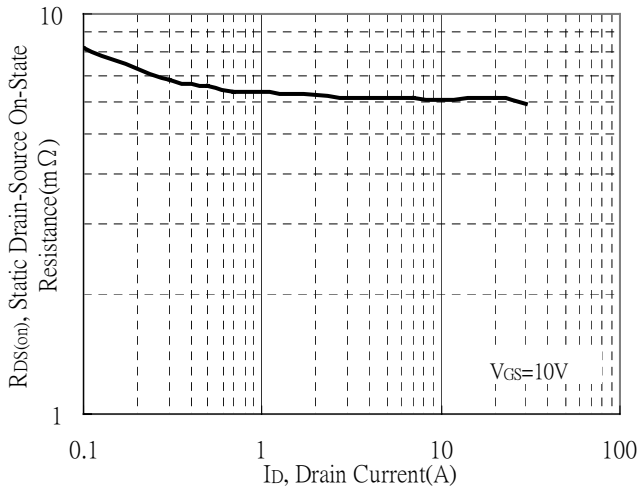
Typical Output Characteristics



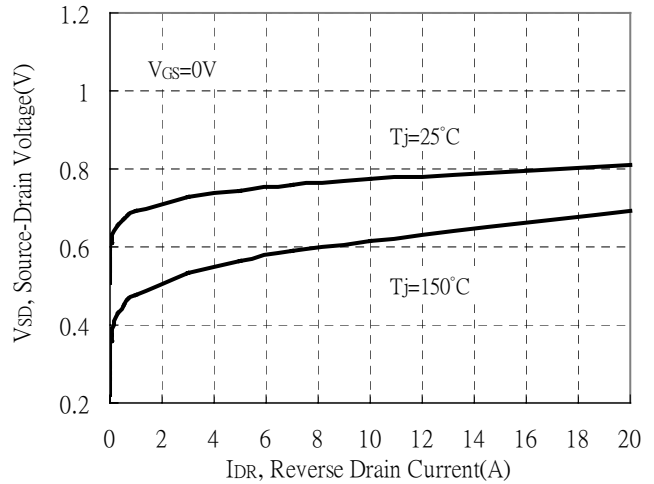
Brekdown Voltage vs Ambient Temperature



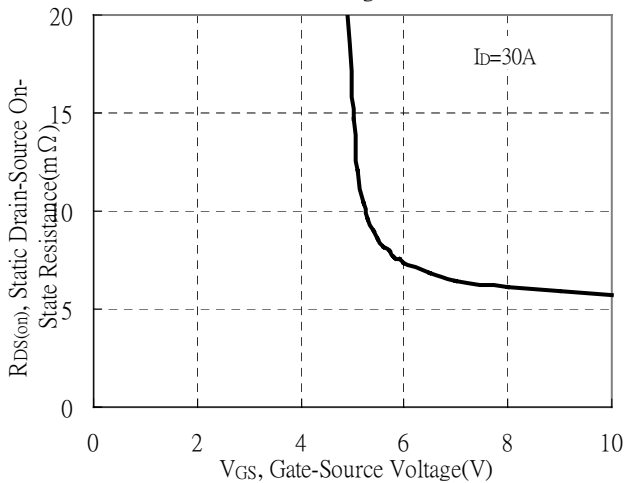
Static Drain-Source On-State resistance vs Drain Current



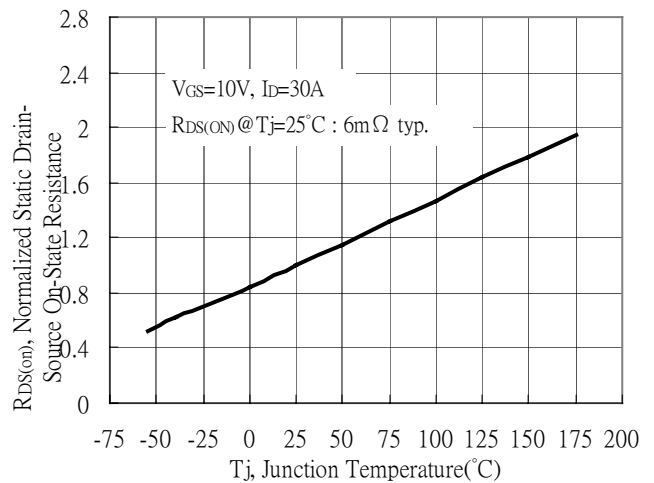
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

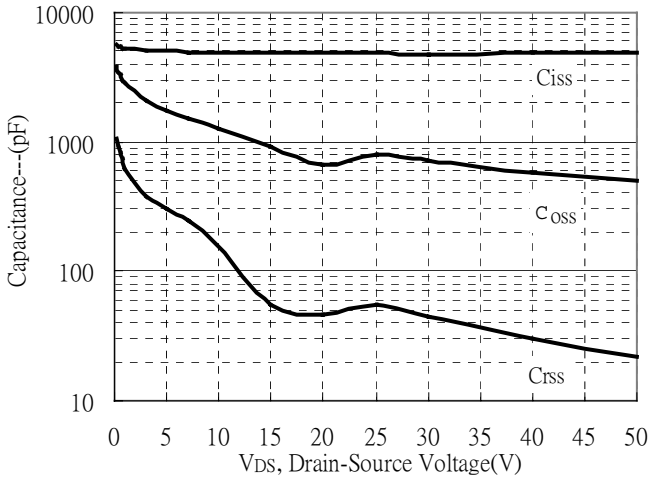


Drain-Source On-State Resistance vs Junction Temperature

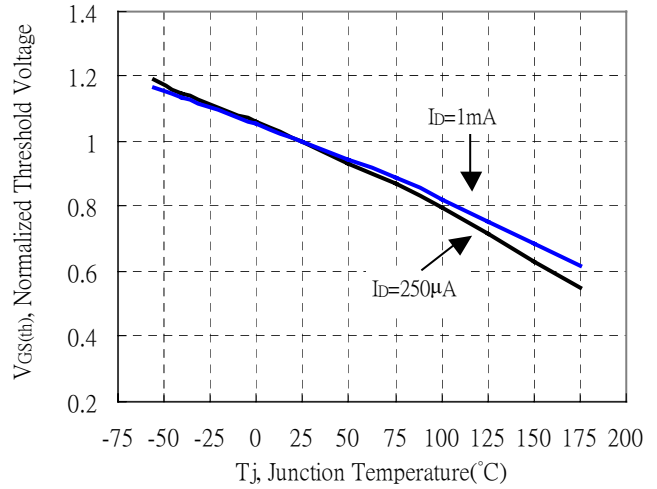


Typical Characteristics(Cont.)

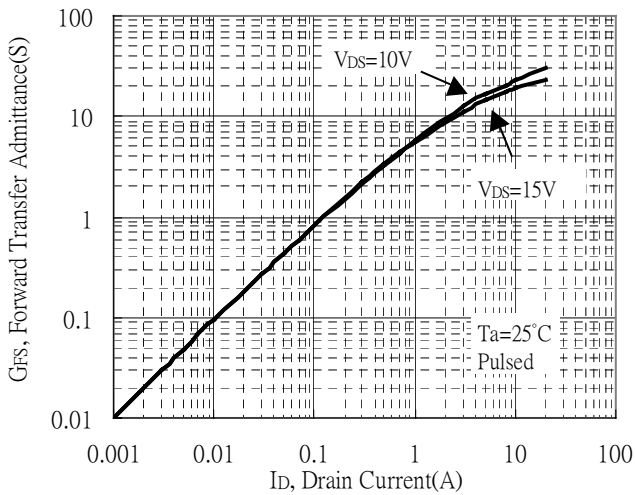
Capacitance vs Drain-to-Source Voltage



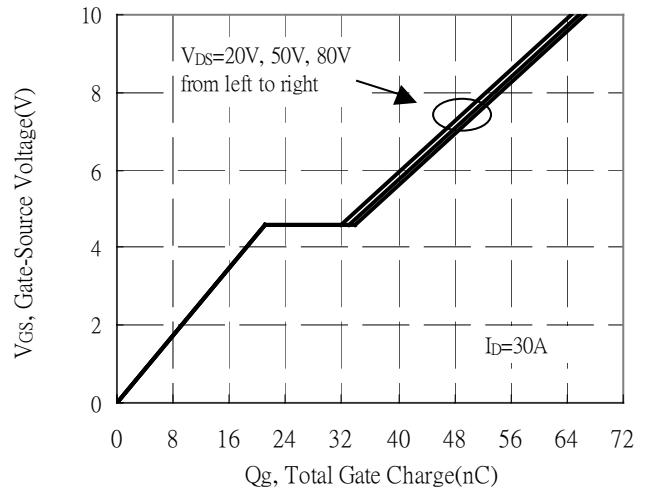
Threshold Voltage vs Junction Temperature



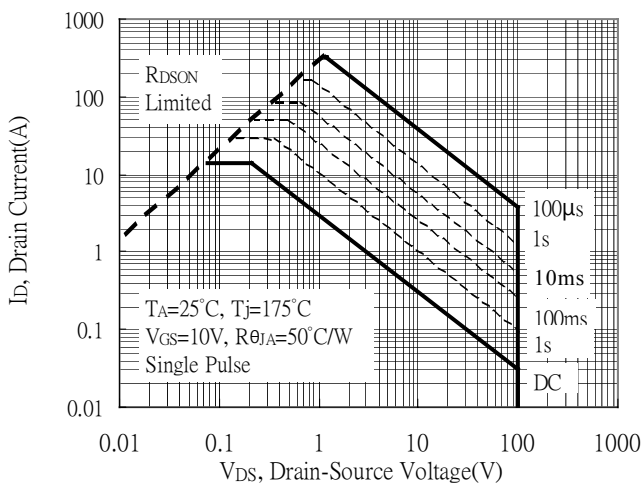
Forward Transfer Admittance vs Drain Current



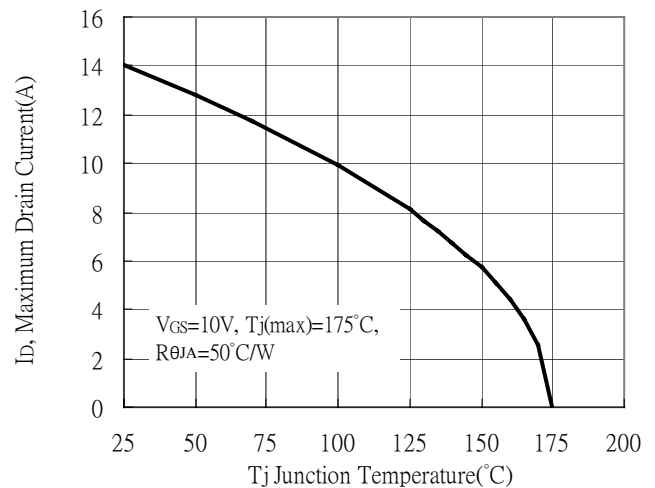
Gate Charge Characteristics



Maximum Safe Operating Area



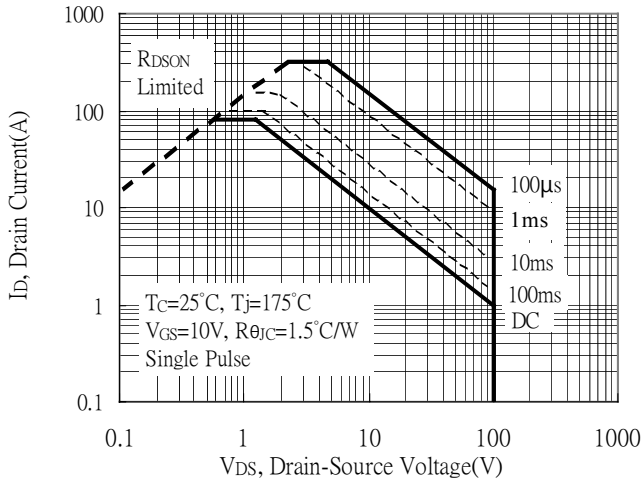
Maximum Drain Current vs Junction Temperature



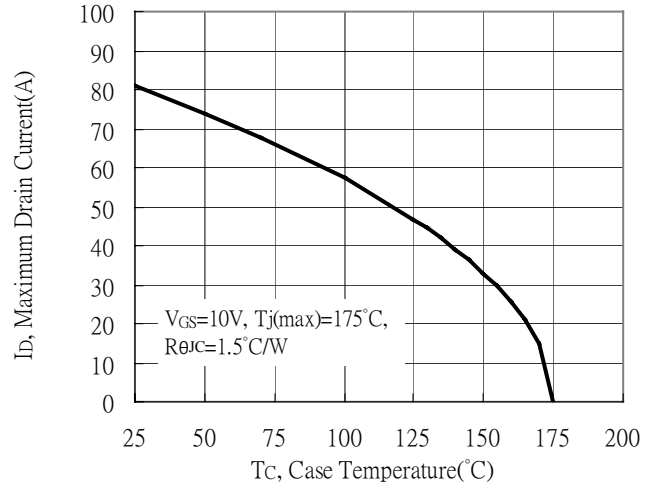


Typical Characteristics(Cont.)

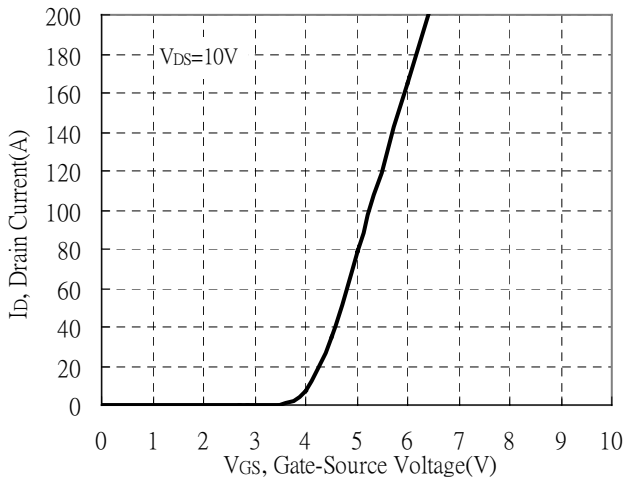
Maximum Safe Operating Area



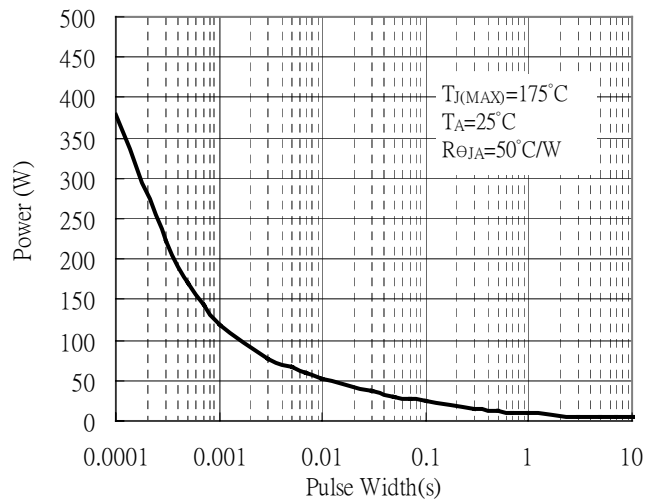
Maximum Drain Current vs Case Temperature



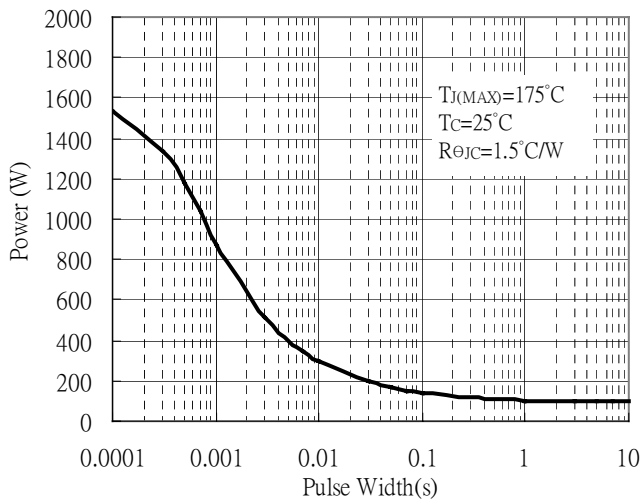
Typical Transfer Characteristics



Single Pulse Power Rating, Junction to Case

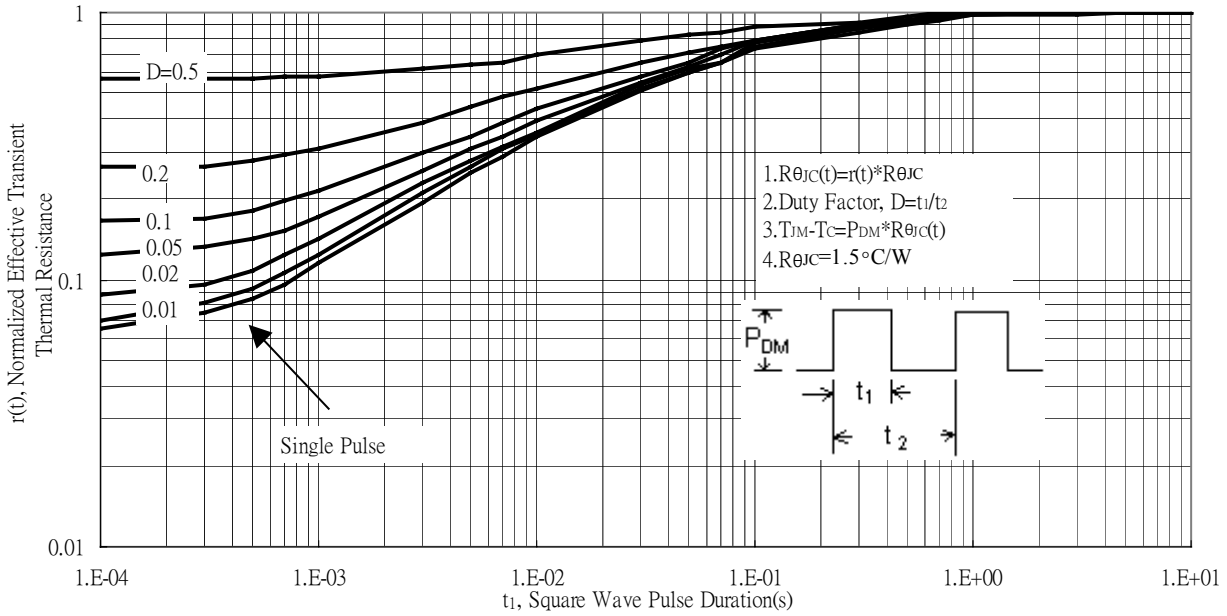


Single Pulse Power Rating, Junction to Case

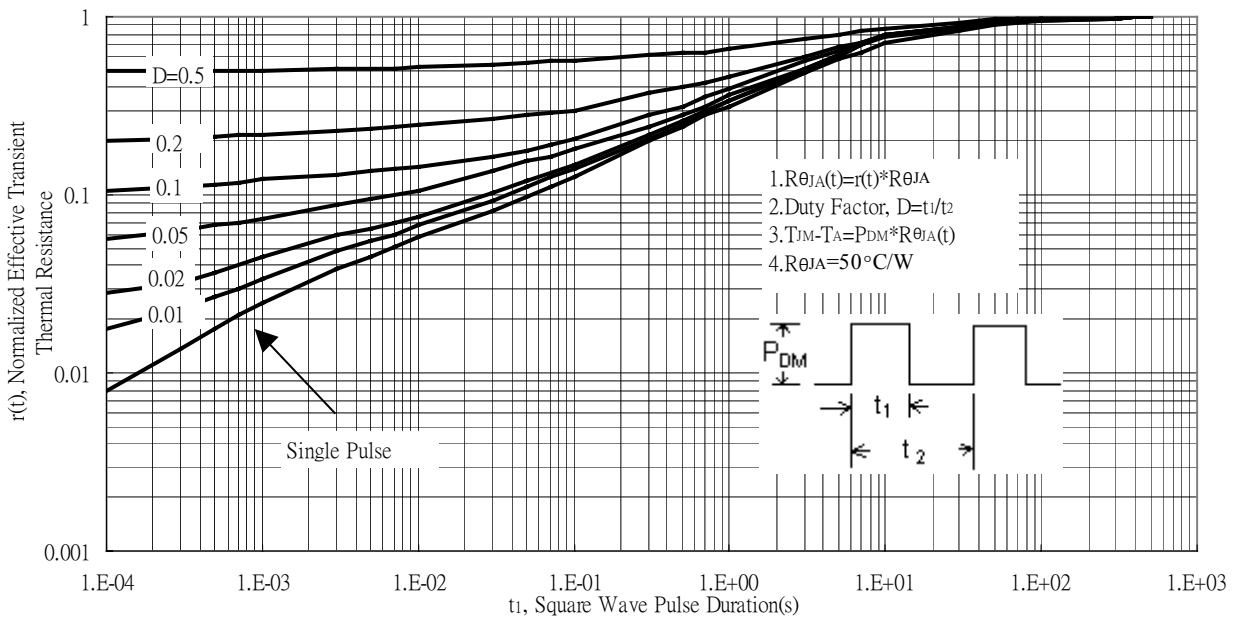


Typical Characteristics(Cont.)

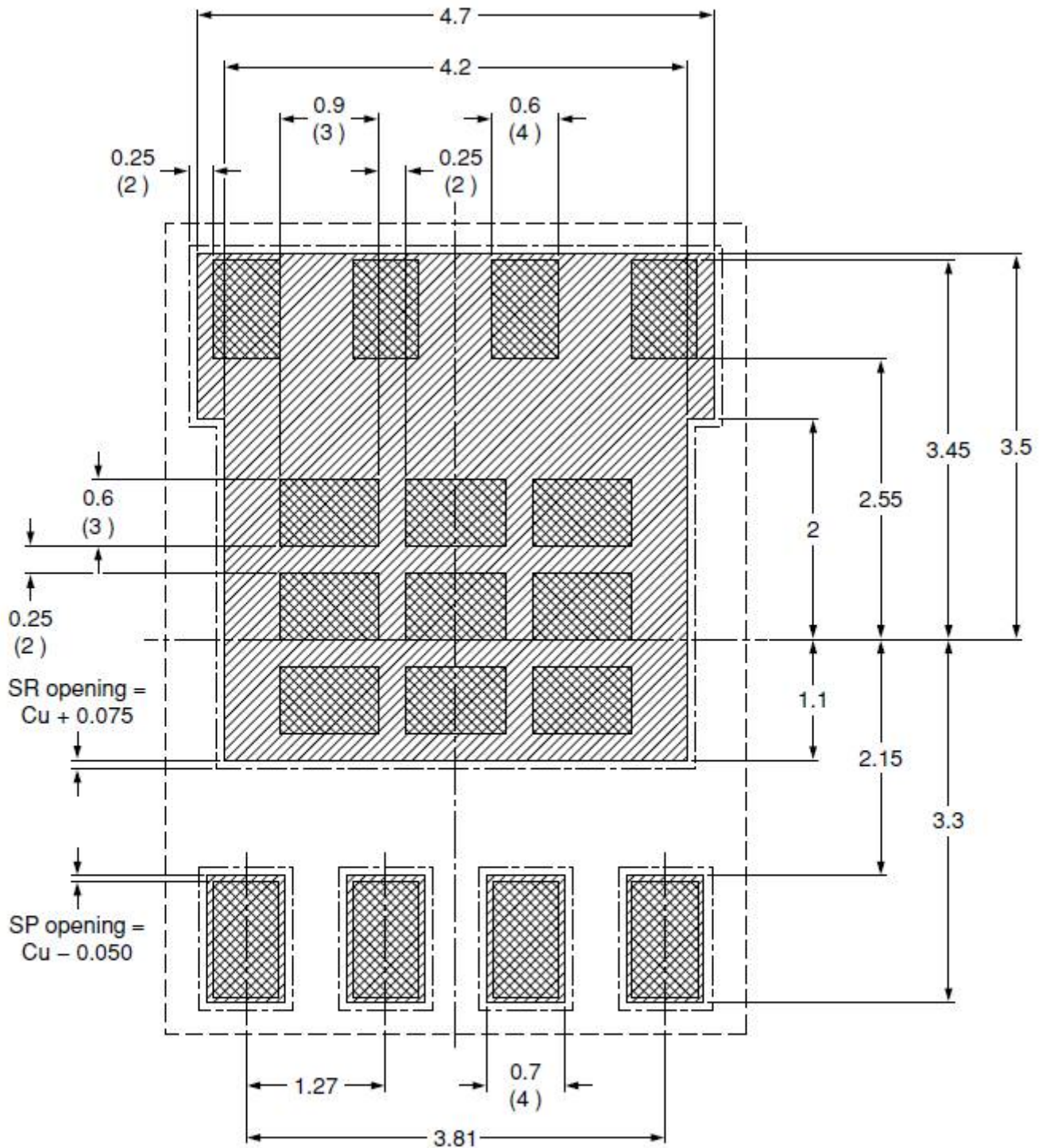
Transient Thermal Response Curves



Transient Thermal Response Curves

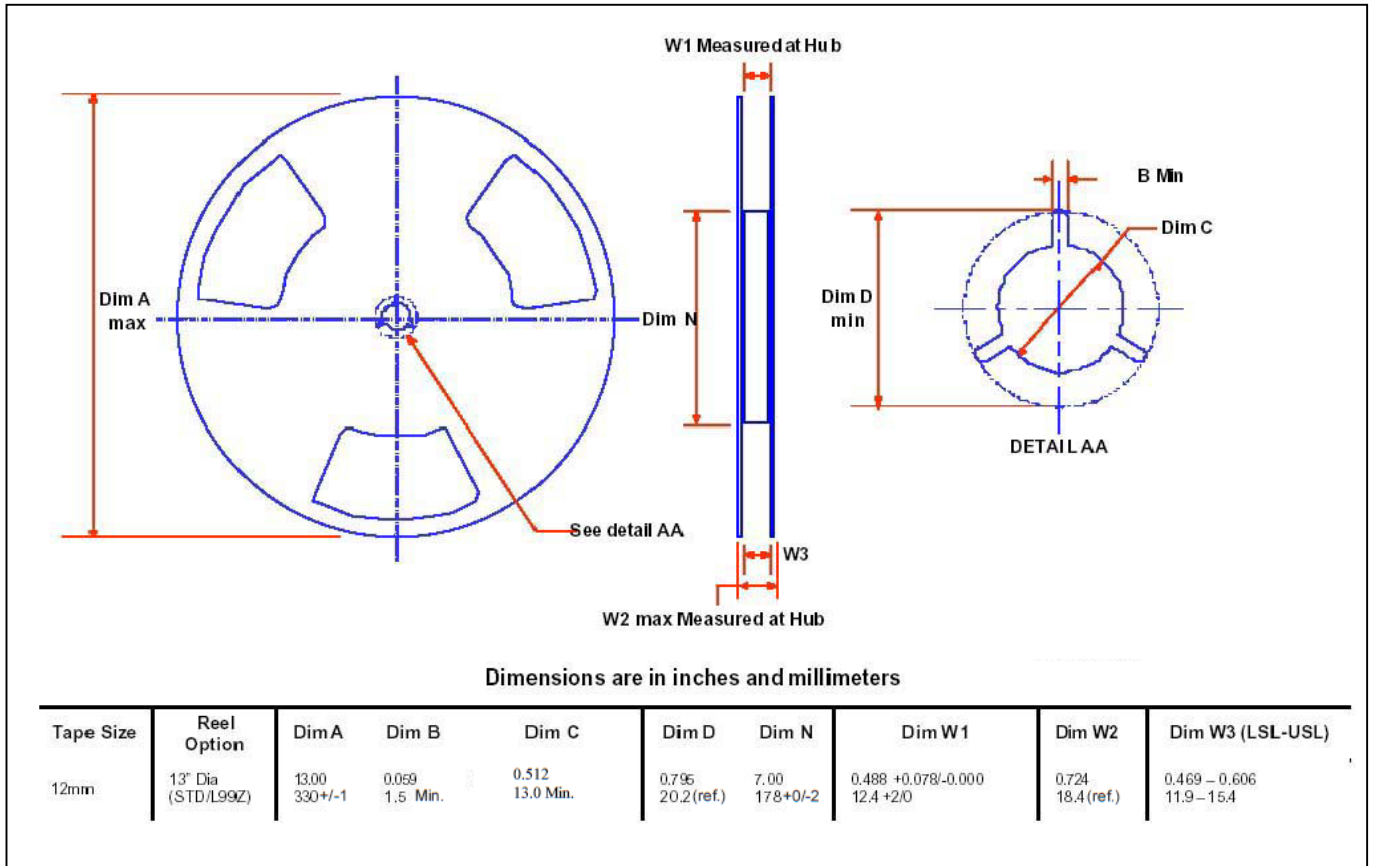


Recommended Soldering Footprint & Stencil Design

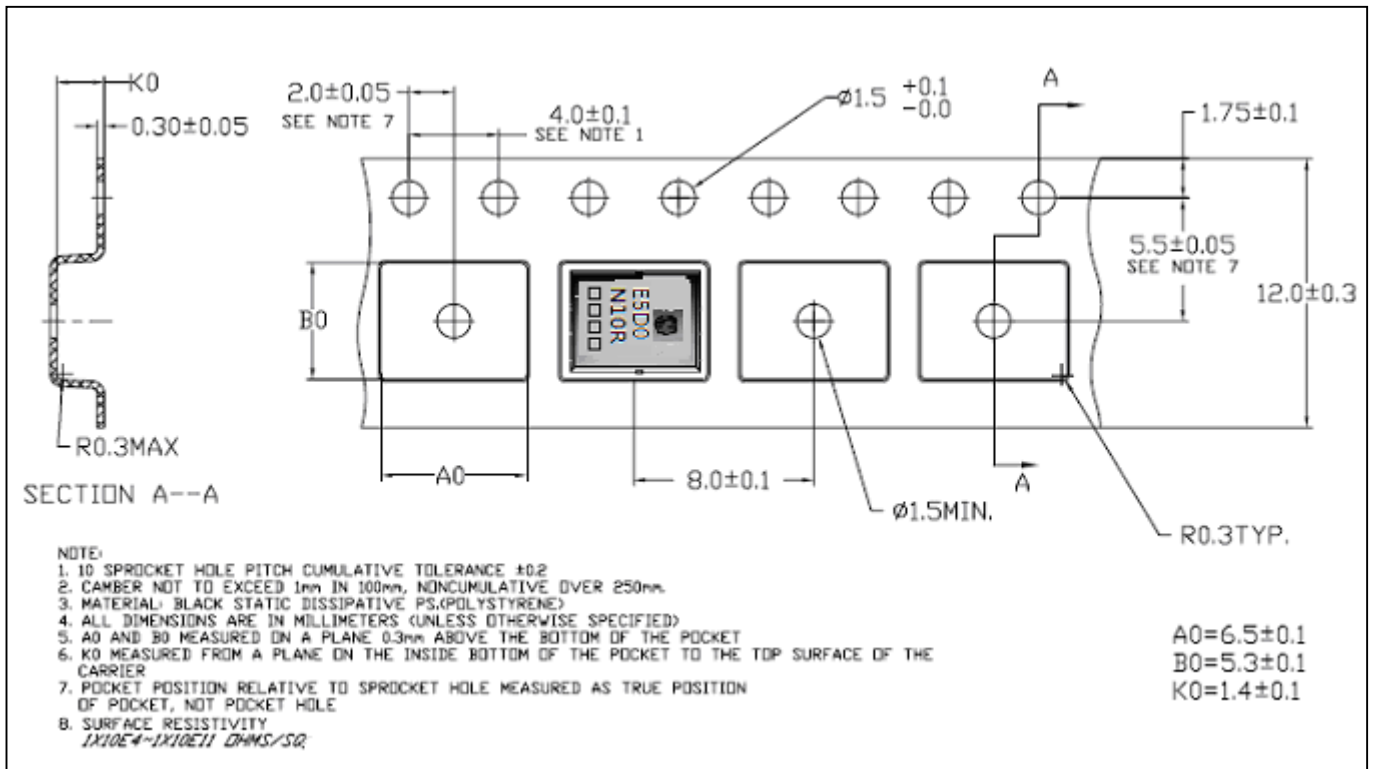


unit : mm

Reel Dimension

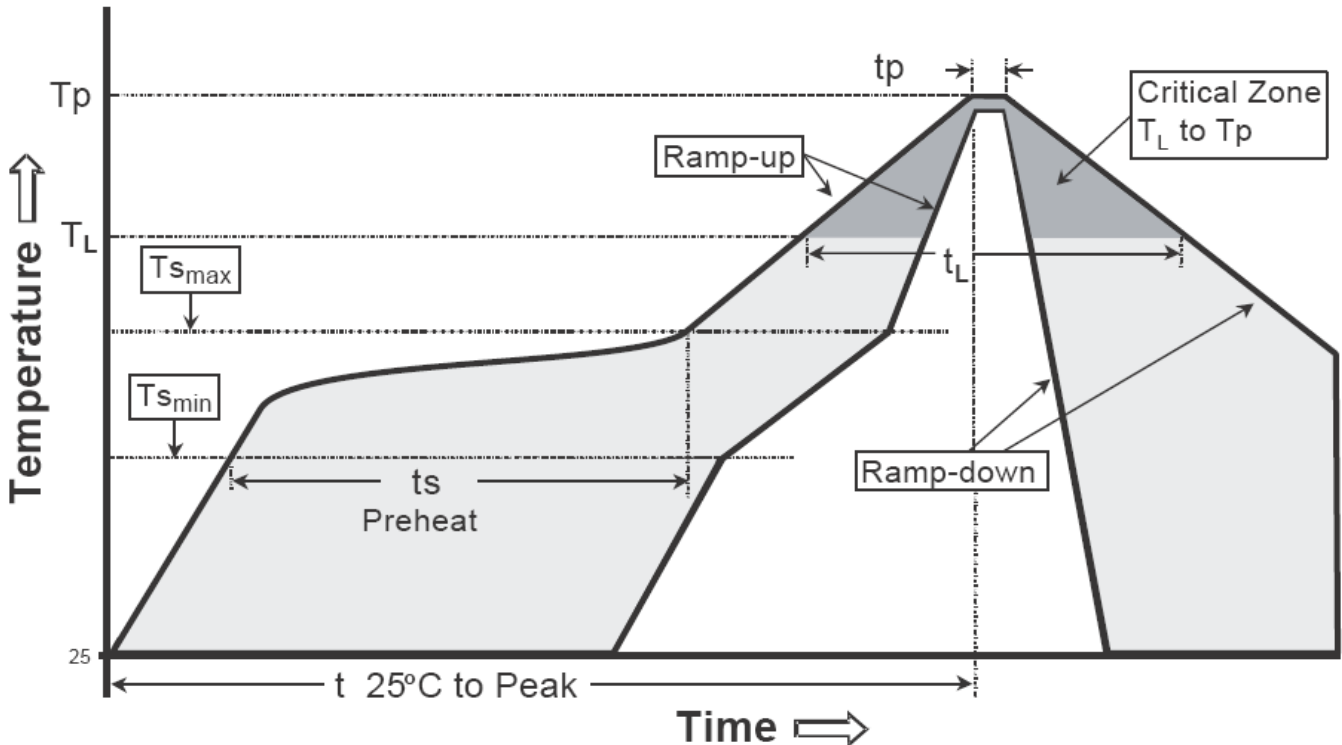


Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

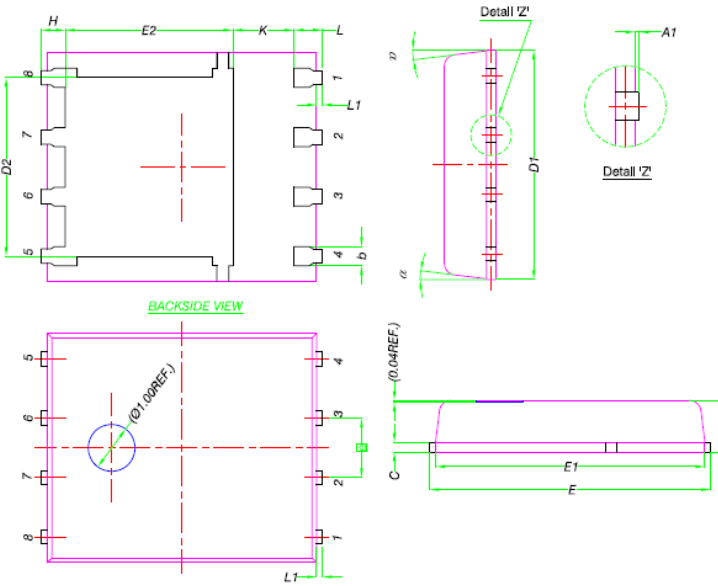
Recommended temperature profile for IR reflow


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note :1. All temperatures refer to topside of the package, measured on the package body surface.

2.For devices mounted on FR-4 PCB of 1.6mm or equivalent grade PCB. If other grade PCB is used, care should be taken to match the coefficients of thermal expansion between components and PCB. If they are not matched well, the solder joints may crack or the bodies of the parts may crack or shatter as the assembly cools.

DFN5x6 Dimension



The diagram shows the DFN5x6 package dimensions. It includes a top view with dimensions A, A1, b, C, E, E1, E2, H, K, L, L1, and L. A 'BACKSIDE VIEW' shows the lead thickness dimension D2. Two 'Detail 'Z'' views show the lead profile with dimensions D1 and A. A circular feature is labeled '(0.100REF.)'. The marking area shows the device name 'E5D0 N10R' and a date code consisting of four squares.

Marking :

Device Name → E5D0
 N10R
 Date Code → □□□□

8-Lead DFN5x6 Plastic Package
 CYS Package Code : H8

Date Code(counting from left to right) :
 1st code: year code, the last digit of Christian year
 2nd code : month code, Jan→A, Feb→B, Mar→C, Apr→D, May→E, Jun→F, Jul→G, Aug→H, Sep→J, Oct→K, Nov→L, Dec→M
 3rd and 4th codes : production serial number, 01~99

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.90	1.10	0.035	0.043	E2	3.38	3.78	0.133	0.149
A1	0.00	0.05	0.000	0.002	e	1.27 BSC		0.050	BSC
b	0.33	0.51	0.013	0.020	H	0.41	0.61	0.016	0.024
C	0.20	0.30	0.008	0.012	K	1.10	-	0.043	-
D1	4.80	5.00	0.189	0.197	L	0.51	0.71	0.020	0.028
D2	3.61	3.96	0.142	0.156	L1	0.06	0.20	0.002	0.008
E	5.90	6.10	0.232	0.240	θ	8°	12°	8°	12°
E1	5.70	5.80	0.224	0.228					

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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