

N-Channel Enhancement Mode Power MOSFET

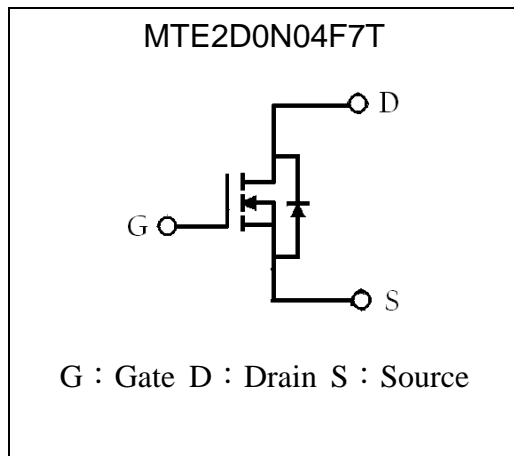
MTE2D0N04F7T

BV_{DSS}	40V
I_D @ $V_{GS}=10V, T_c=25^\circ C$	168A
$R_{DS(on)(TYP)}$ @ $V_{GS}=10V, I_D=20A$	1.7m Ω

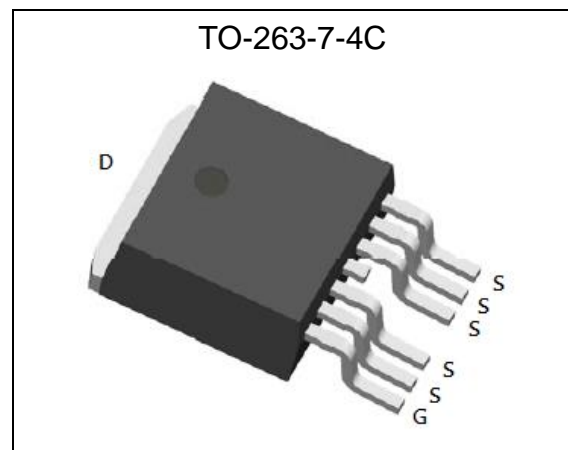
Features

- Simple Drive Requirement
- Fast Switching Characteristic
- RoHS compliant package

Symbol

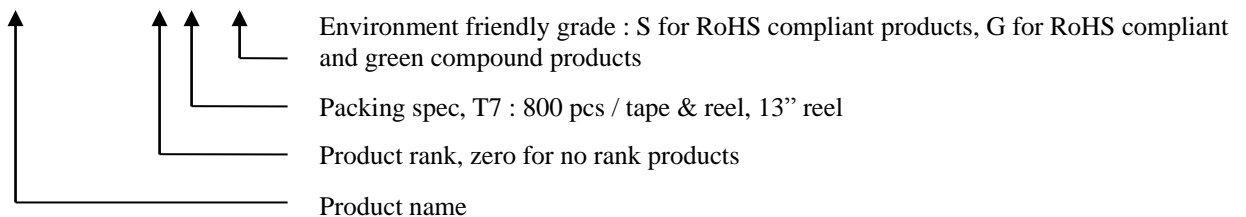


Outline



Ordering Information

Device	Package	Shipping
MTE2D0N04F7T-0-T7-X	TO-263-7-4C (Pb-free lead plating and RoHS compliant package)	800 pcs / Tape & Reel



**Absolute Maximum Ratings** ($T_C=25^{\circ}\text{C}$, unless otherwise noted)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current @ $T_C=25^{\circ}\text{C}$ (silicon limit)	I_D	208	A
Continuous Drain Current @ $T_C=100^{\circ}\text{C}$ (silicon limit)		147	
Continuous Drain Current @ $T_C=25^{\circ}\text{C}$ (package limit) (Note 1)		168	
Pulsed Drain Current (Note 3)	I_{DM}	772	
Continuous Drain Current @ $T_A=25^{\circ}\text{C}$ (Note 2)	I_{DSM}	24.6	
Continuous Drain Current @ $T_A=70^{\circ}\text{C}$ (Note 2)		19.7	
Avalanche Current @ $L=0.1\text{mH}$ (Note 3)	I_{AS}	80	
Avalanche Energy @ $L=1\text{mH}$, $I_D=50\text{A}$, $V_{DD}=40\text{V}$ (Note 4)	E_{AS}	1250	mJ
Power Dissipation	P_D	$T_C=25^{\circ}\text{C}$ (Note 1)	166
		$T_C=100^{\circ}\text{C}$ (Note 1)	83
Power Dissipation	P_{DSM}	$T_A=25^{\circ}\text{C}$ (Note 2)	2
		$T_A=70^{\circ}\text{C}$ (Note 2)	1.3
Operating Junction and Storage Temperature	T_j, T_{stg}	-55~+175	$^{\circ}\text{C}$

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{\theta JC}$	0.9	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-ambient, max, (Note 2)	$R_{\theta JA}$	62.5	

- Note : 1.The power dissipation P_D is based on $T_{J(MAX)}=175^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- 2.The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2 oz. copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.
3. Pulse width limited by junction temperature $T_{J(MAX)}=175^{\circ}\text{C}$. Ratings are based on low frequency and low duty cycles to keep initial $T_J=25^{\circ}\text{C}$.
4. 100% tested by conditions of $L=1\text{mH}$, $I_{AS}=20\text{A}$, $V_{GS}=10\text{V}$, $V_{DD}=30\text{V}$.
5. The static characteristics are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% maximum.
6. The $R_{\theta JA}$ is the sum of thermal resistance from junction to case $R_{\theta JC}$ and case to ambient.



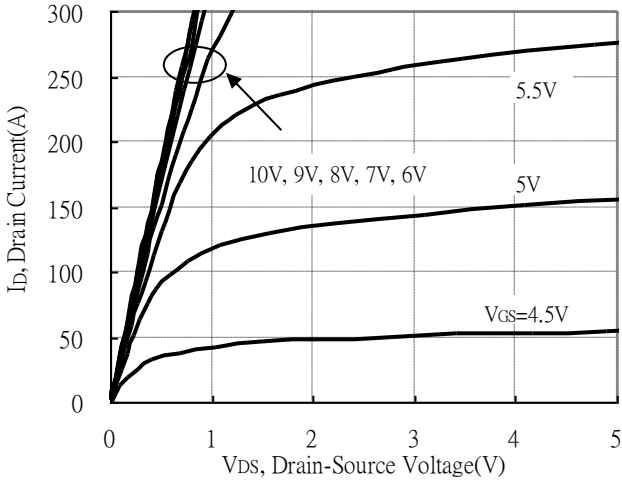
Characteristics (Tc=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	40	-	-	V	V _{GS} =0V, I _D =250μA
V _{GS(th)}	2.0	-	4.0		V _{DS} = V _{GS} , I _D =250μA
G _{FSS}	-	33.8	-	S	V _{DS} =10V, I _D =20A
I _{GSS}	-	-	±100	nA	V _{GS} =±30V, V _{DS} =0V
I _{DSS}	-	-	1	μA	V _{DS} =32V, V _{GS} =0V
	-	-	25		V _{DS} =32V, V _{GS} =0V, T _j =125°C
*R _{DS(ON)}	-	1.7	2.3	mΩ	V _{GS} =10V, I _D =20A
Dynamic					
*Q _g	-	113	-	nC	I _D =20A, V _{DS} =20V, V _{GS} =10V
*Q _{gs}	-	27.5	-		
*Q _{gd}	-	29.4	-		
*t _{d(ON)}	-	40.6	-	ns	V _{DS} =20V, I _D =20A, V _{GS} =10V, R _G =1Ω
*t _r	-	26	-		
*t _{d(OFF)}	-	84.2	-		
*t _f	-	19.6	-		
C _{iss}	-	5831	-	pF	V _{GS} =0V, V _{DS} =30V, f=1MHz
C _{oss}	-	751	-		
C _{rss}	-	345	-		
R _g	-	0.9	-	Ω	f=1MHz
Source-Drain Diode					
*I _S	-	-	196	A	
*I _{SM}	-	-	784		
*V _{SD}	-	0.68	1	V	I _S =1A, V _{GS} =0V
*t _{rr}	-	38.2	-	ns	I _F =1A, V _{GS} =0V, dI _F /dt=100A/μs
*Q _{rr}	-	41.1	-	nC	

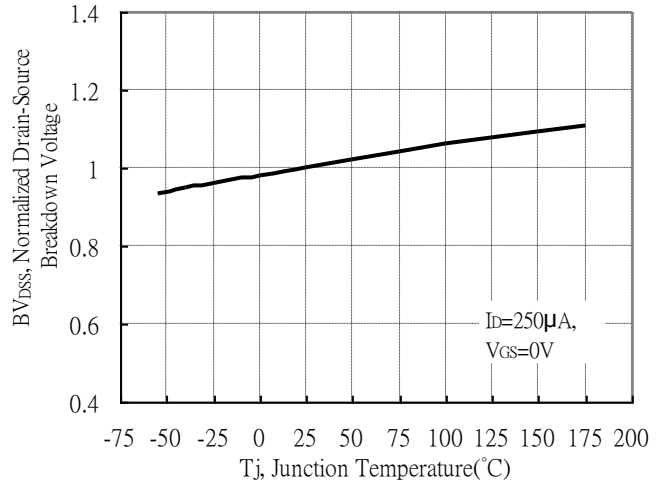
*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Typical Characteristics

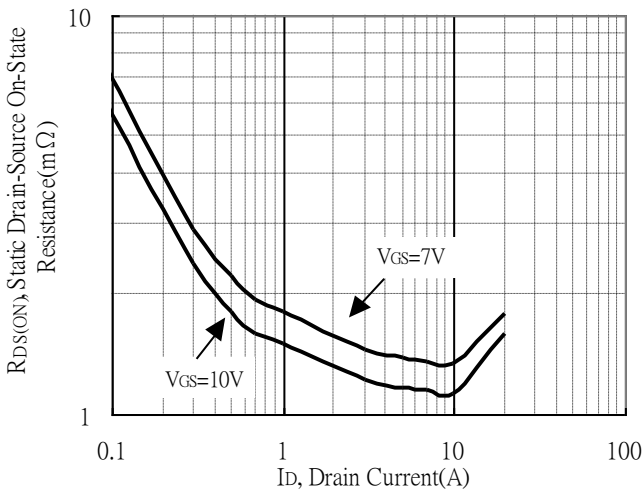
Typical Output Characteristics



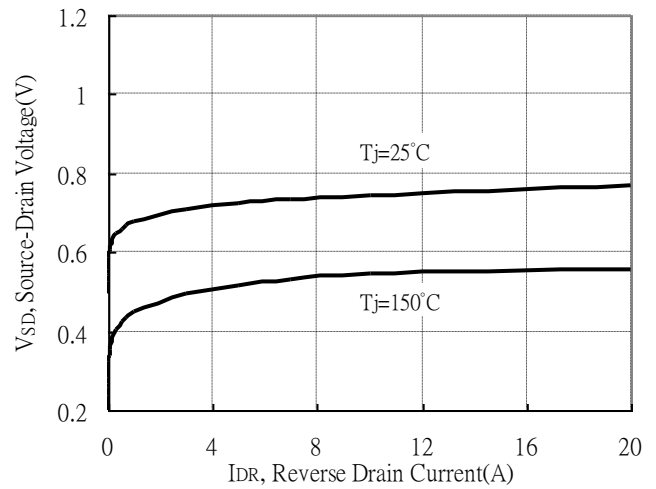
Brekdown Voltage vs Ambient Temperature



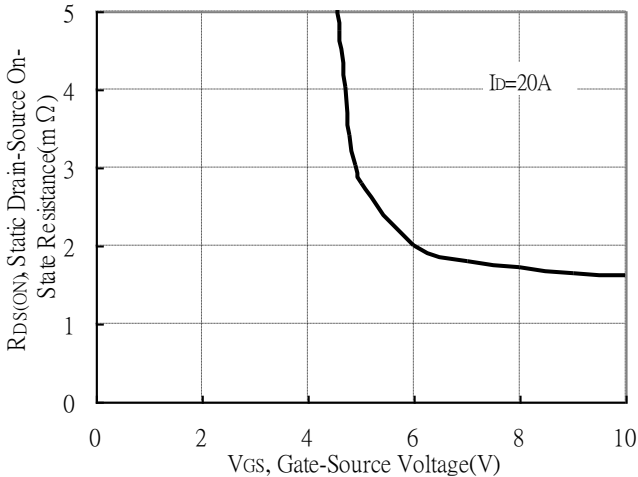
Static Drain-Source On-State resistance vs Drain Current



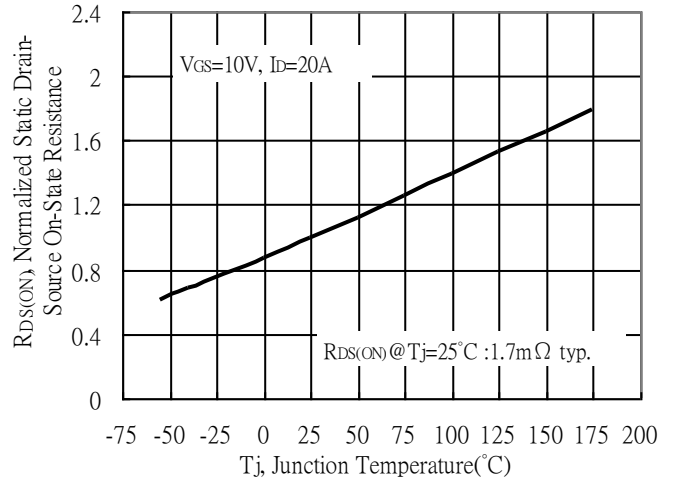
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage



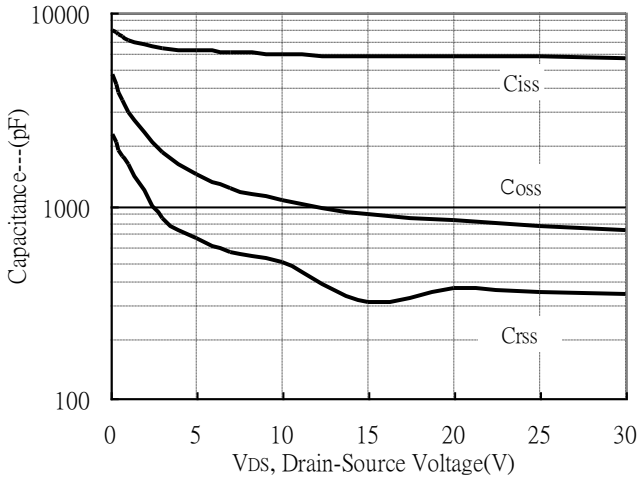
Drain-Source On-State Resistance vs Junction Temperature



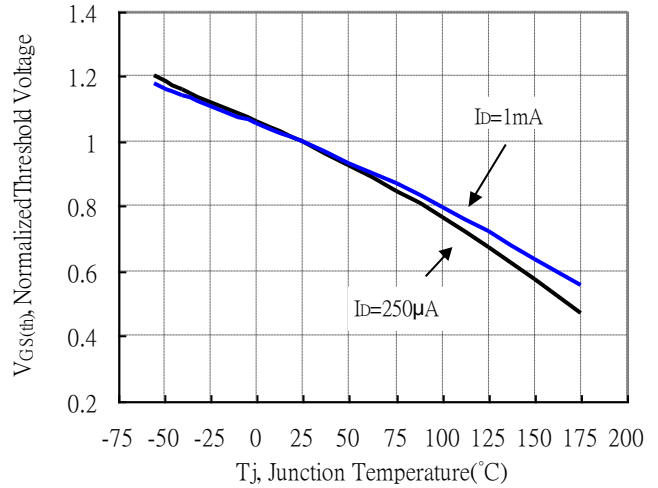


Typical Characteristics(Cont.)

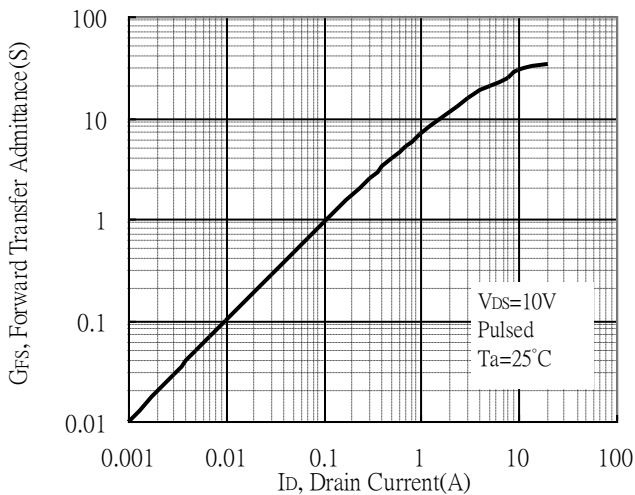
Capacitance vs Drain-to-Source Voltage



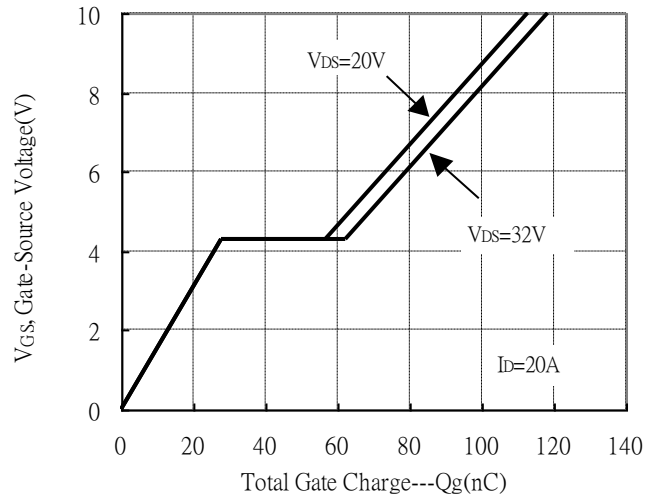
Threshold Voltage vs Junction Temperature



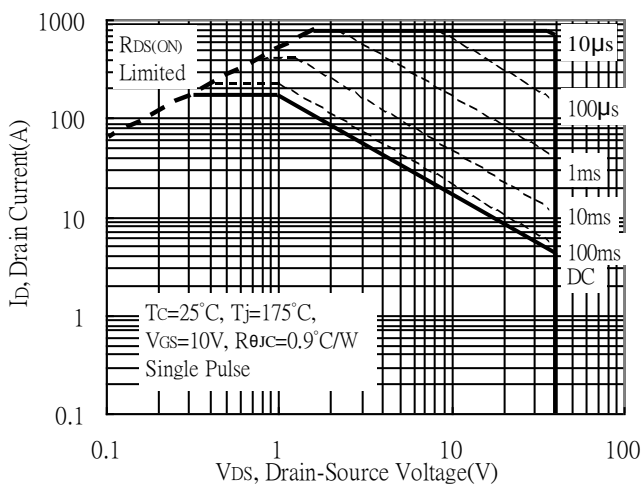
Forward Transfer Admittance vs Drain Current



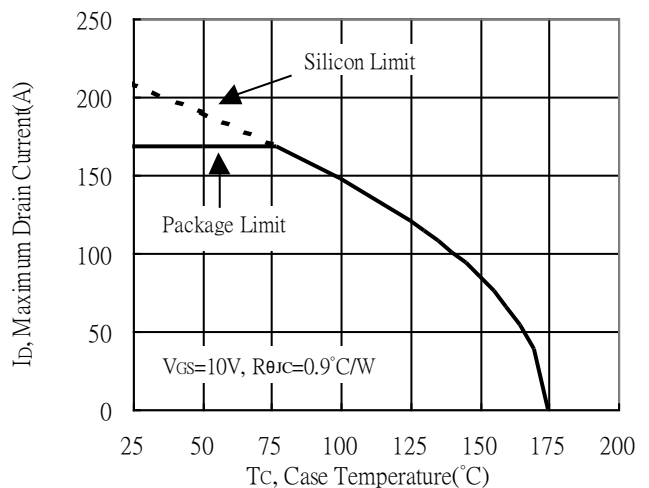
Gate Charge Characteristics



Maximum Safe Operating Area

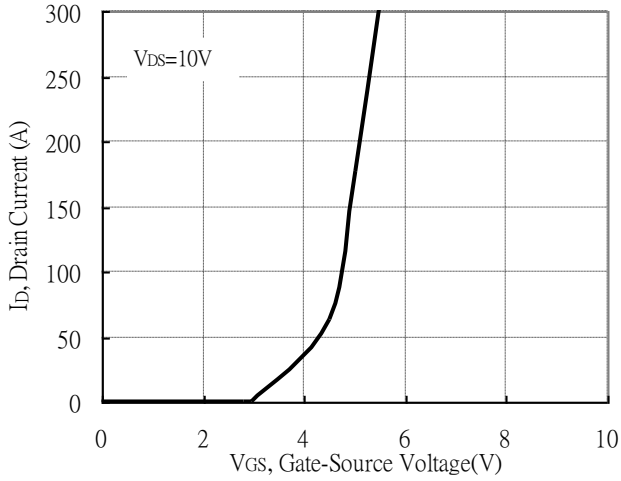


Maximum Drain Current vs Case Temperature

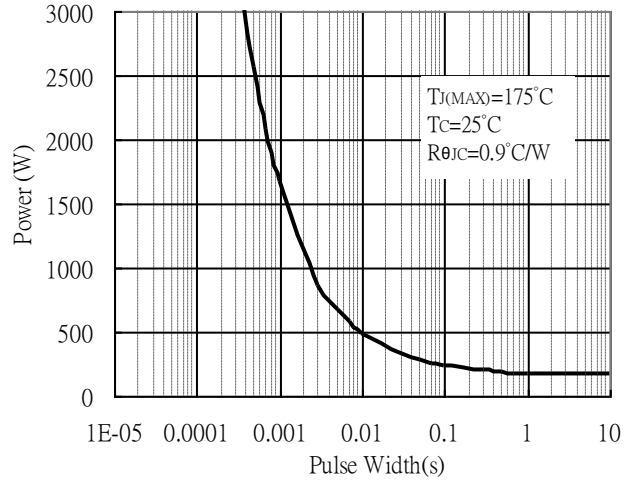


Typical Characteristics(Cont.)

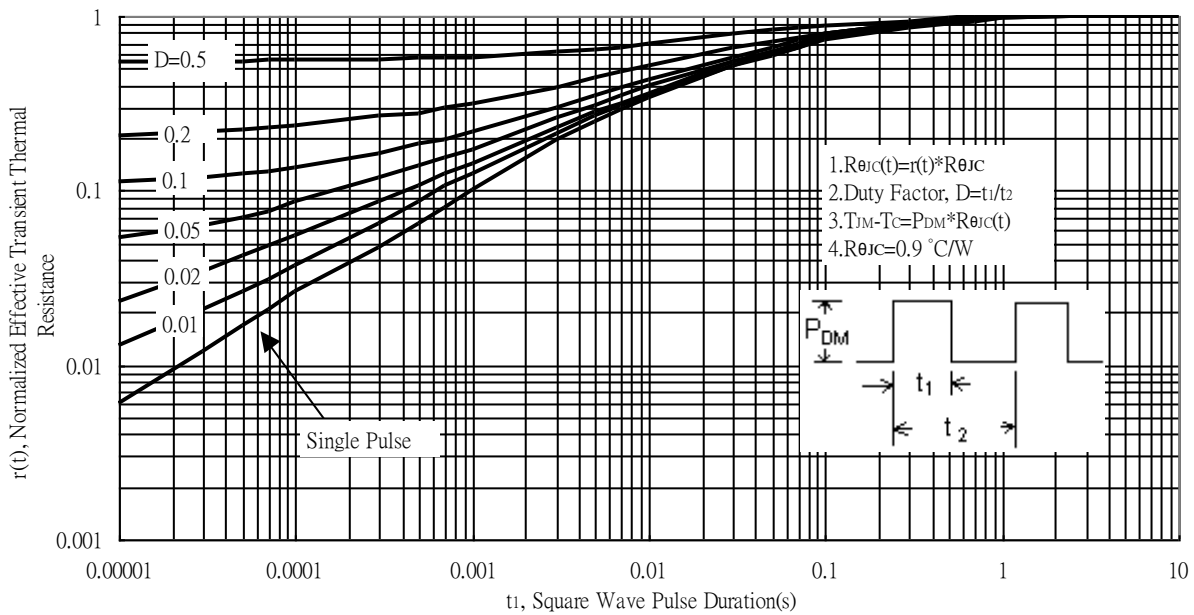
Typical Transfer Characteristics



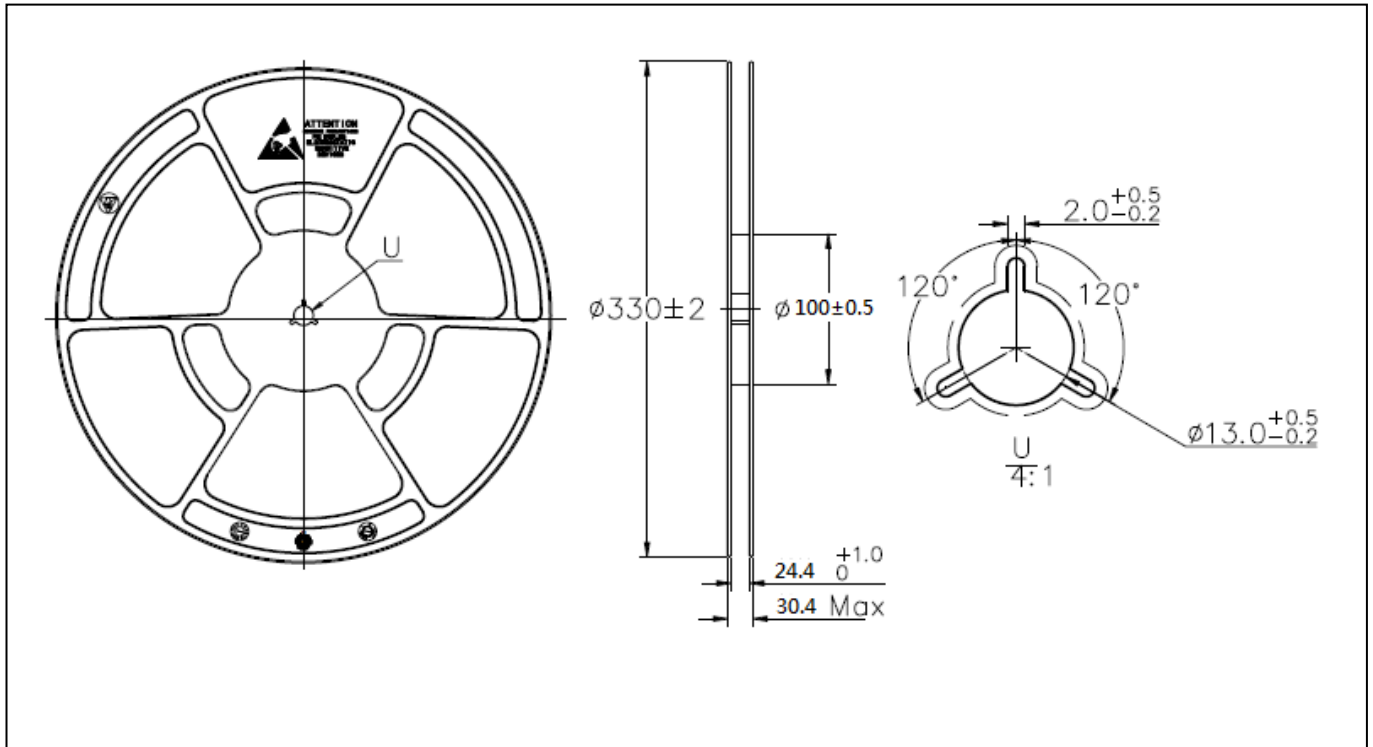
Single Pulse Maximum Power Dissipation



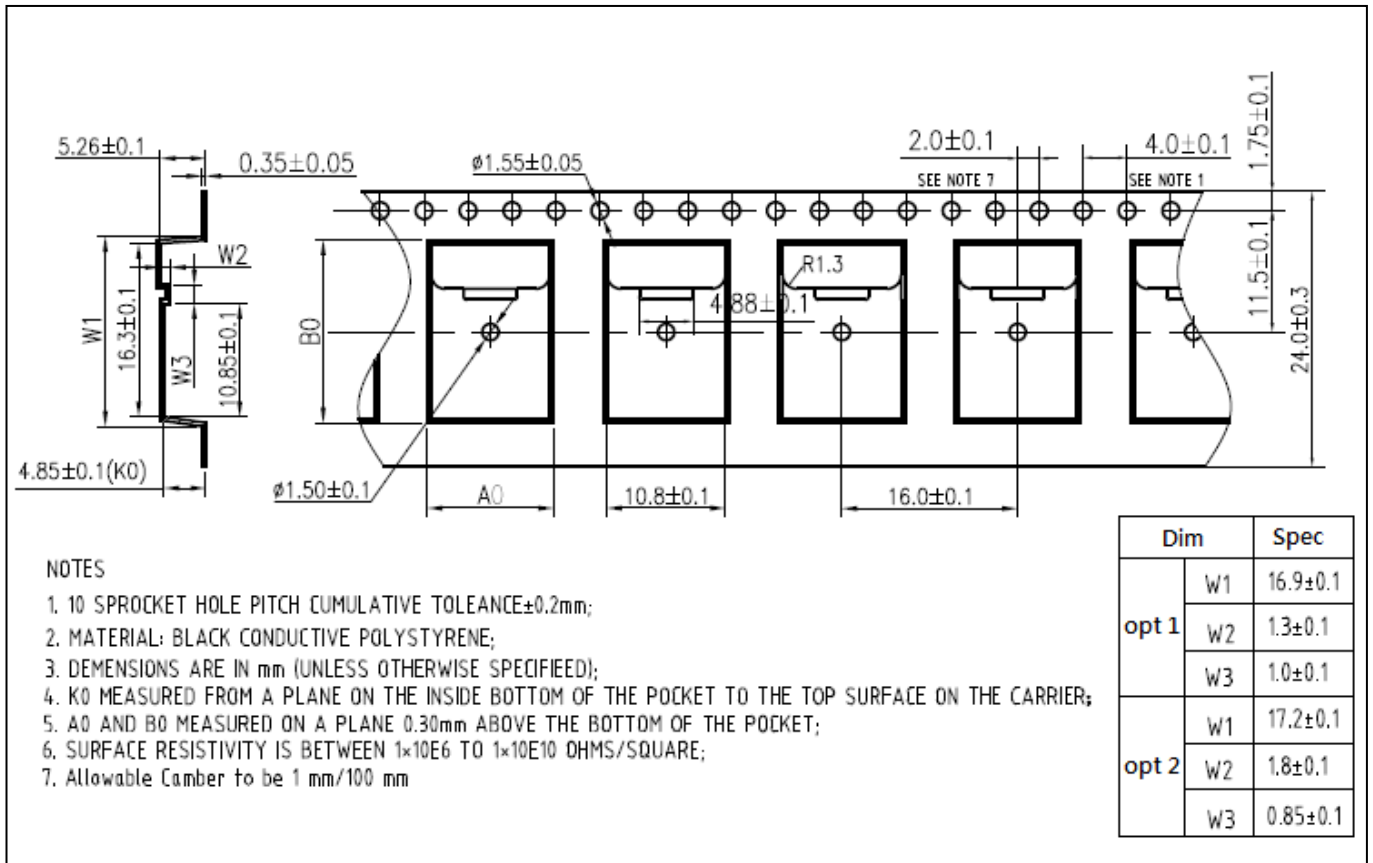
Transient Thermal Response Curves



Reel Dimension

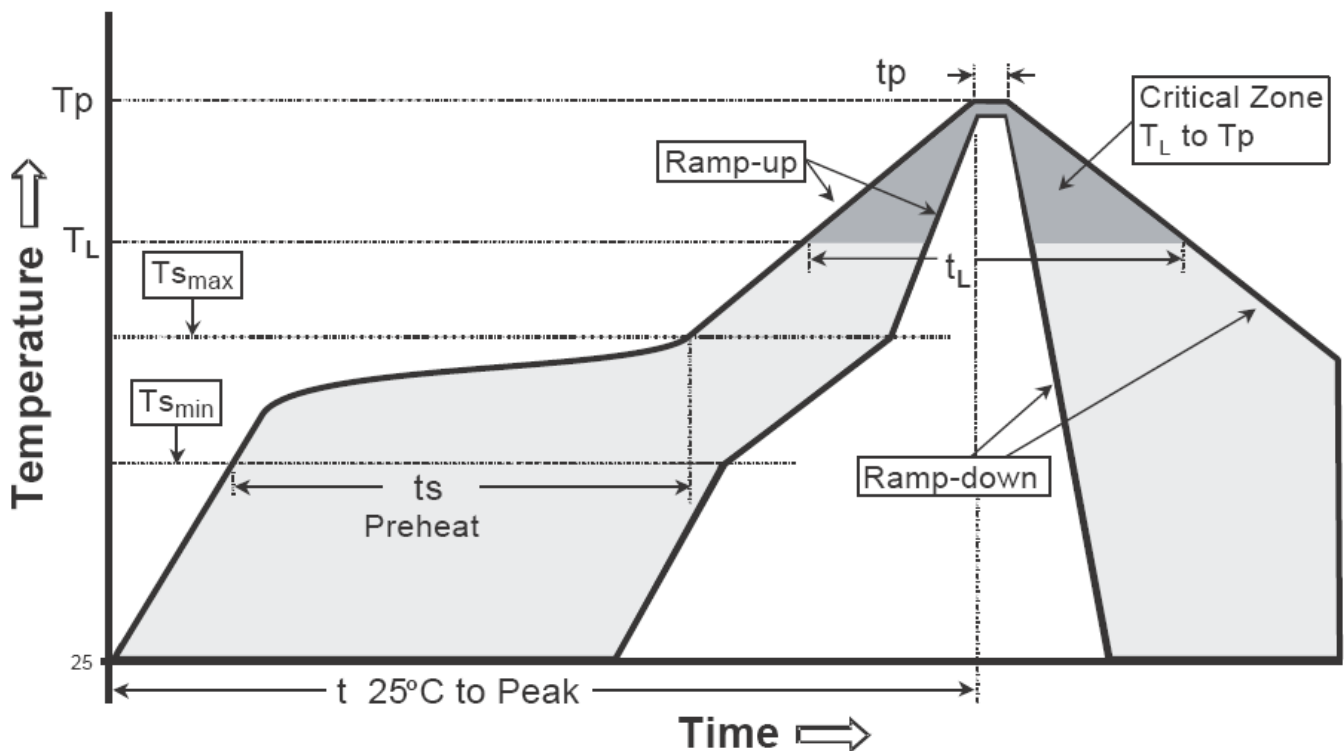


Carrier Tape Dimension



Recommended wave soldering condition

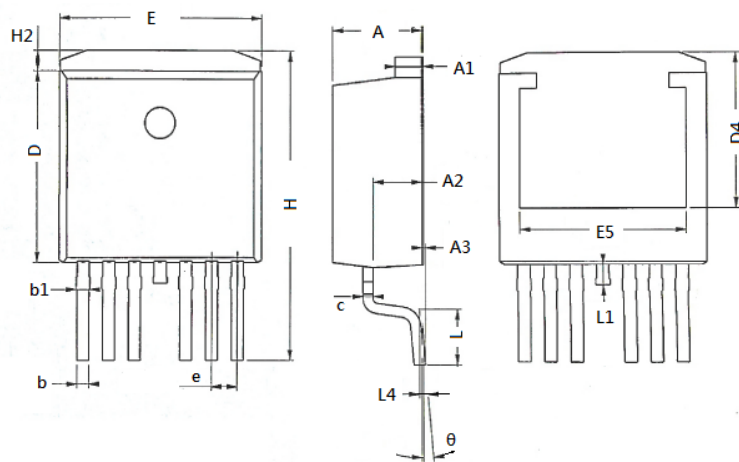
Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

Recommended temperature profile for IR reflow


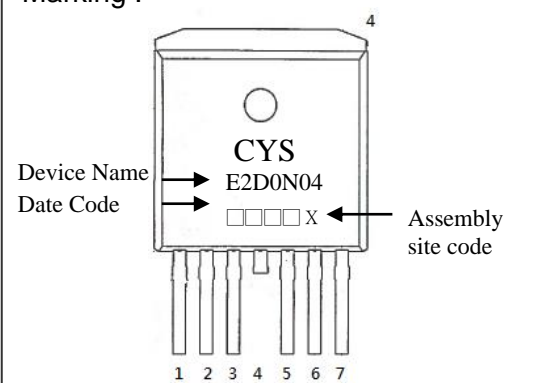
Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(t _p)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-263-7-4C Dimension



Marking :



Device Name → E2D0N04
 Date Code → □□□□ X ← Assembly site code

7-Lead Plastic Surface Mounted TO-263-7L Package
 CYStek Package Code : F7T

Date Code : (From left to right)
 First Code : Year code, the last digit of Christinr year. For example, 2014→4, 2015→, 2016→6, ..., etc.
 Second Code : Month code, Jan→A, Feb→B, Mar→C, Apr→D, May→E, Jun→F, Jul→G, Aug→H, Sep→J,
 Oct→K, Nov→L, Dec→M
 Third and fourth codes : production serial number, 01~99

Style : Pin 1. Gate
 Pin 2, 3, 5, 6, 7 : Source
 Pin 4. Drain

*:Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1673	0.1791	4.25	4.55	E	0.3858	0.4016	9.80	10.20
A1	0.0472	0.0551	1.20	1.40	e	0.0500	BSC	1.27	BSC
A2	0.0886	0.1004	2.25	2.55	E5	0.2854	-	7.25	-
A3	0.0004	0.0098	0.01	0.25	H	0.5768	0.6043	14.65	15.35
b	0.0197	0.0276	0.50	0.70	H2	0.0315	0.0472	0.80	1.20
b1	0.0228	0.0331	0.58	0.84	L	0.0945	0.1181	2.40	3.00
c	0.0157	0.0236	0.40	0.60	L1	0.0335	0.0453	0.85	1.15
D	0.3563	0.3720	9.05	9.45	L4	0.0098	BSC	0.25	BSC
D4	0.2717	-	6.90	-	θ	2°	8°	2°	8°

Notes : 1.Controlling dimension : millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.