

-30V P-Channel Enhancement Mode MOSFET

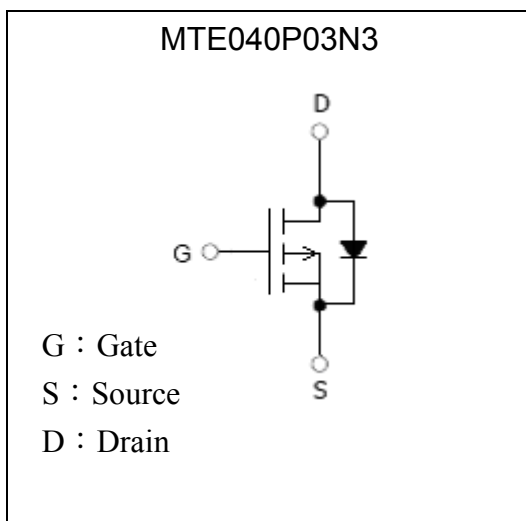
MTE040P03N3

BV _{DSS}	-30V
I _D @ V _{GS} =-10V, T _A =25°C	-4A
R _{DS(on)} @V _{GS} =-10V, I _D =-4.5A	42mΩ (typ)

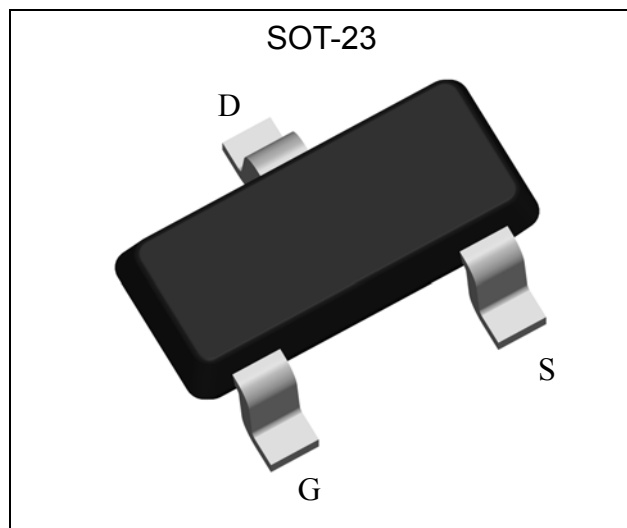
Features

- Compact and low profile SOT-23 package
- Advanced trench process technology
- High density cell design for ultra low on resistance
- Pb-free lead plating package

Symbol

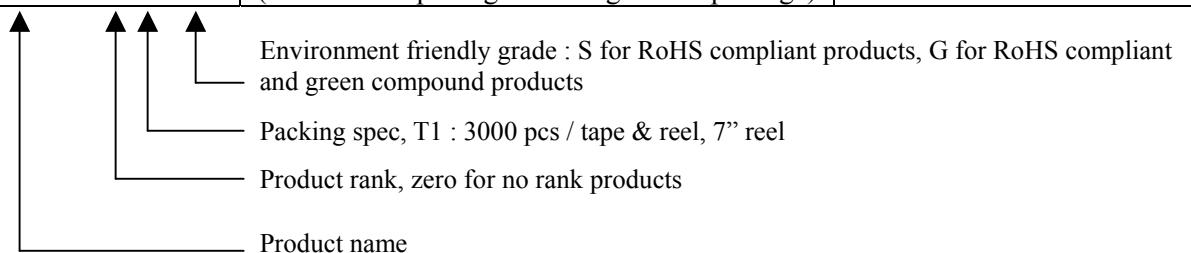


Outline



Ordering Information

Device	Package	Shipping
MTE040P03N3-0-T1-G	SOT-23 (Pb-free lead plating and halogen-free package)	3000 pcs / tape & reel





Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V _{DS}	-30	V
Gate-Source Voltage	V _{GS}	±20	
Continuous Drain Current @ TA=25°C, VGS=-10V (Note 3)	I _D	-4	A
Continuous Drain Current @ TA=70°C, VGS=-10V (Note 3)		-3.2	
Pulsed Drain Current (Notes 1, 2)	I _{DM}	-24	
Maximum Power Dissipation (Note 4)	P _D	1.25	W
Linear Derating Factor		0.01	W/°C
Operating Junction and Storage Temperature Range	T _j ; T _{stg}	-55~+150	°C

- Note : 1. Pulse width limited by maximum junction temperature.
 2. Pulse width ≤ 300μs, duty cycle ≤ 2%.
 3. Surface mounted on 1 in² copper pad of FR-4 board; 270°C/W when mounted on minimum copper pad

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance, Junction-to-Ambient (PCB mounted)	R _{θJA}	100	°C/W
Thermal Resistance, Junction-to-Case, max	R _{θJC}	45	

Note : Surface mounted on 1 in² copper pad of FR-4 board; 270°C/W when mounted on minimum copper pad

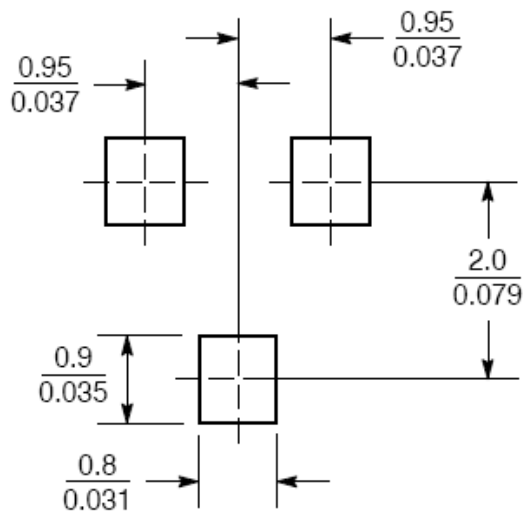
Electrical Characteristics (Tj=25°C, unless otherwise noted)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	-30	-	-	V	V _{GS} =0V, I _D =-250μA
ΔBV _{DSS} /ΔT _j	-	0.01	-	V/°C	Reference to 25°C, I _D =-250μA
V _{GS(th)}	-2	-	-4	V	V _{DS} =V _{GS} , I _D =-250μA
I _{GSS}	-	-	±100	nA	V _{GS} =±20V, V _{DS} =0V
I _{DSS}	-	-	-1	μA	V _{DS} =-24V, V _{GS} =0V
	-	-	-10		V _{DS} =-24V, V _{GS} =0V (T _j =70°C)
*R _{DSON}	-	42	53	mΩ	V _{GS} =-10V, I _D =-4A
*G _{FS}	-	3.4	-	S	V _{DS} =-10V, I _D =-3A
Dynamic					
*Q _g	-	10.3	-	nC	V _{DS} =-24V, I _D =-4A, V _{GS} =-10V
*Q _{gs}	-	2.5	-		
*Q _{gd}	-	2.8	-		
*t _{d(ON)}	-	7.6	-	ns	V _{DS} =-15V, I _D =-4A, V _{GS} =-10V, R _G =1Ω
*t _r	-	15.8	-		
*t _{d(OFF)}	-	34.8	-		
*t _f	-	12.6	-		

Ciss	-	482	-	pF	V _{DS} =-25V, V _{GS} =0V, f=1MHz
Coss	-	65	-		
Crss	-	50	-		
Source-Drain Diode					
*V _{SD}	-	-0.78	-1.2	V	V _{GS} =0V, I _S =-1A
T _{rr}	-	8.2	-	ns	V _{GS} =0V, I _F =-1A, dI _F /dt=100A/μs
Q _{rr}	-	3.3	-	nC	

*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Recommended Soldering Footprint

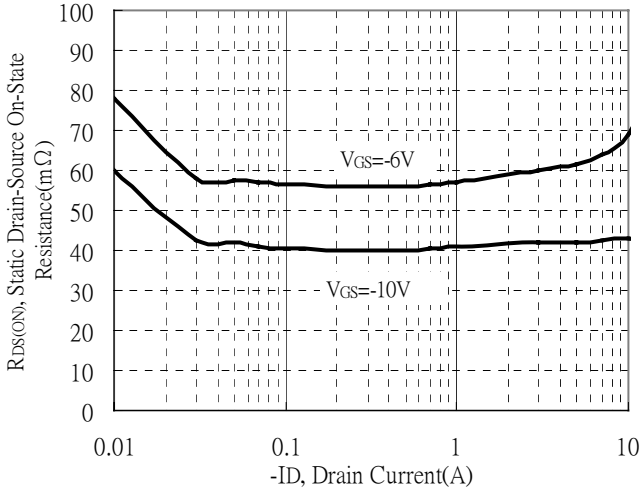


Unit : $\frac{\text{mm}}{\text{inches}}$

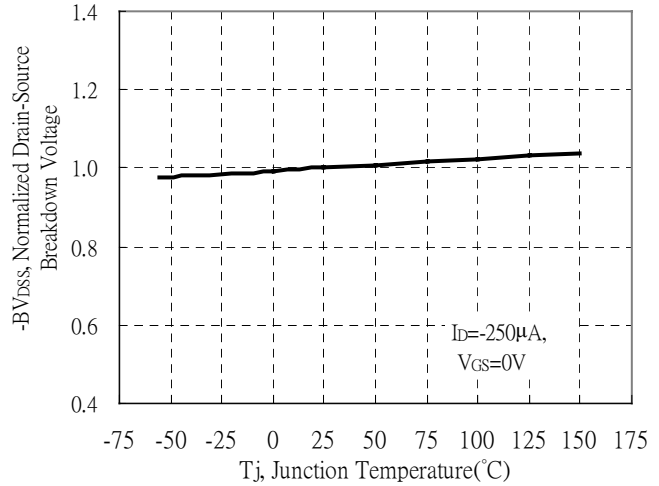


Typical Characteristics

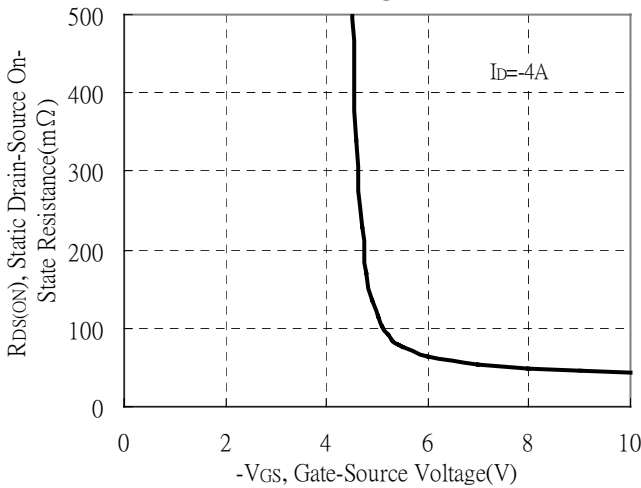
Static Drain-Source On-State resistance vs Drain Current



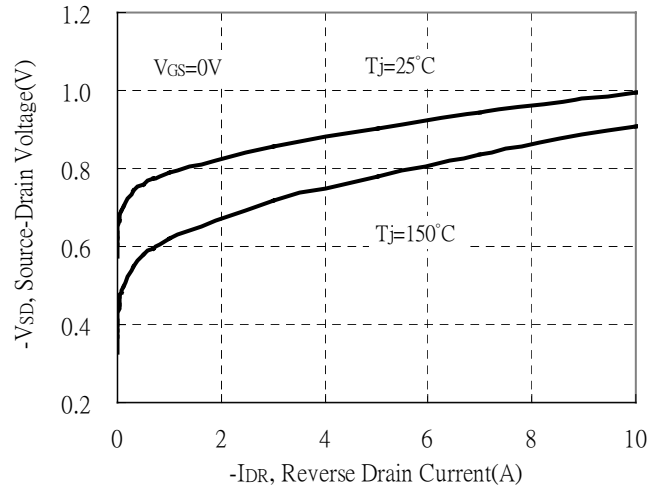
Brekdown Voltage vs Ambient Temperature



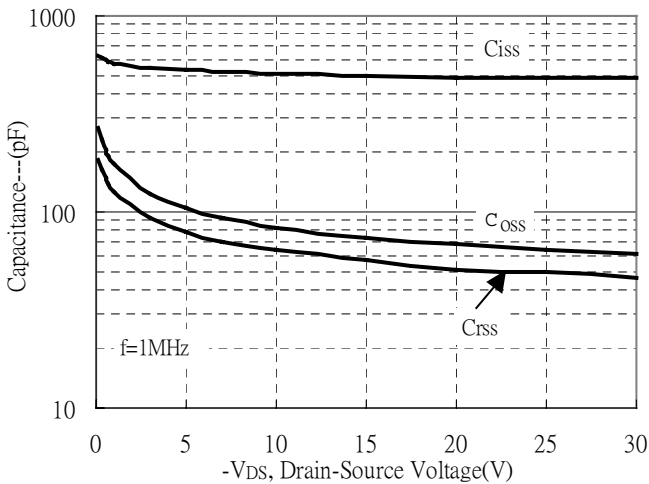
Static Drain-Source On-State Resistance vs Gate-Source Voltage



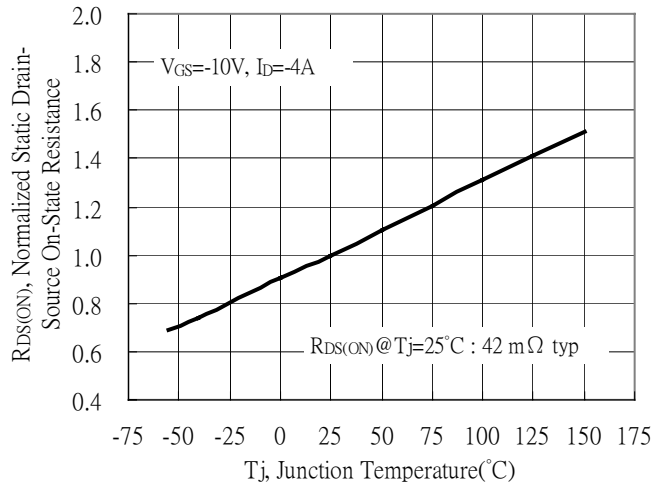
Reverse Drain Current vs Source-Drain Voltage



Capacitance vs Drain-to-Source Voltage

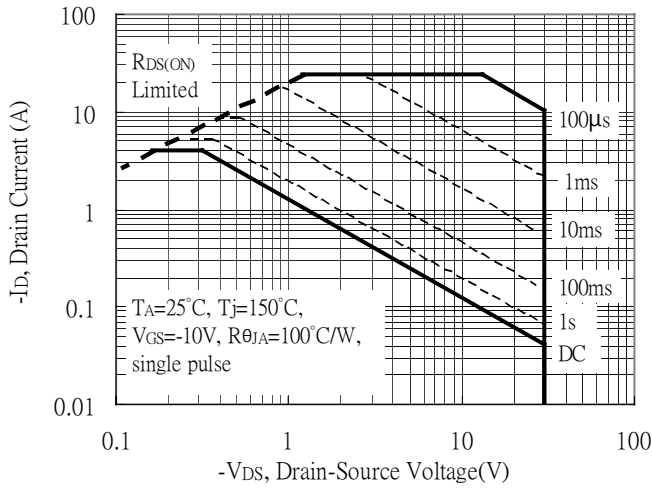


Drain-Source On-State Resistance vs Junction Temperature

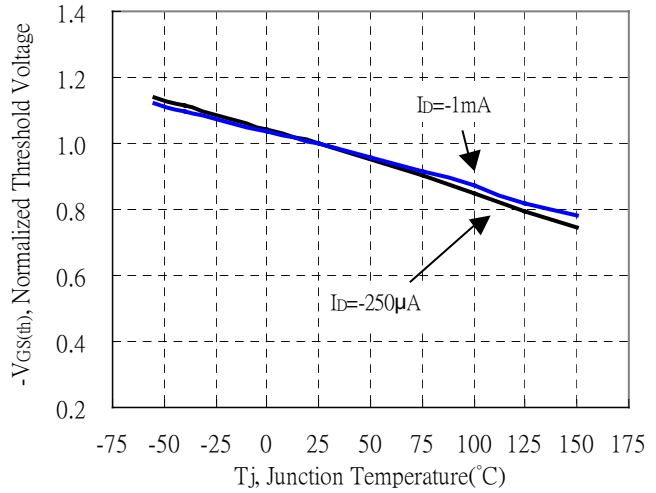


Typical Characteristics(Cont.)

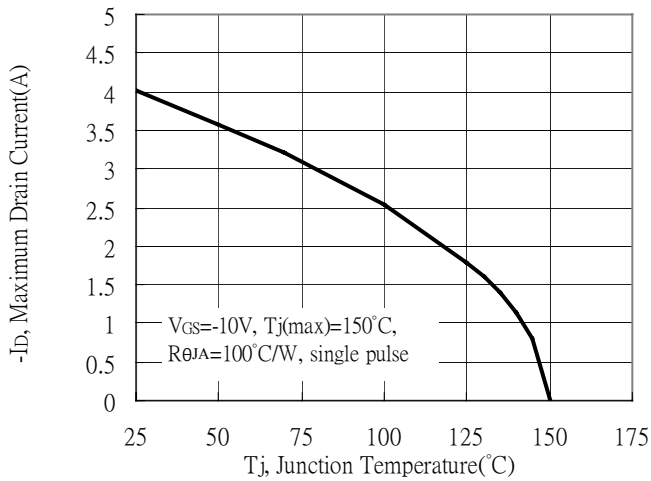
Maximum Safe Operating Area



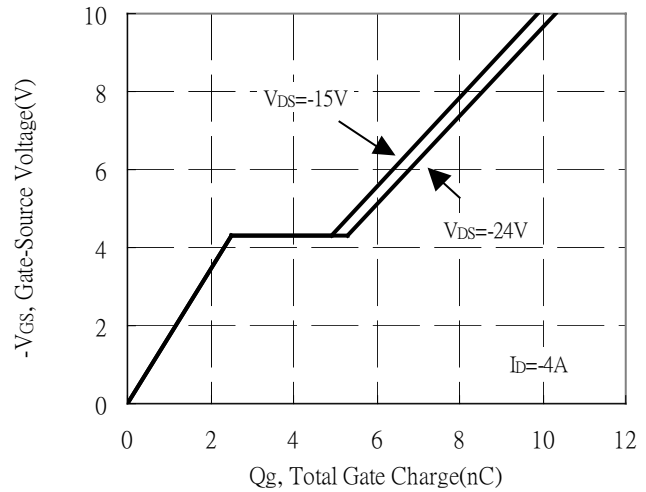
Threshold Voltage vs Junction Temperature



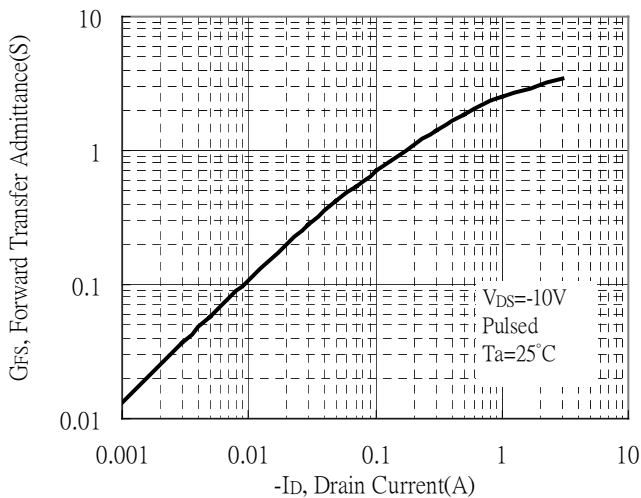
Maximum Drain Current vs Junction Temperature



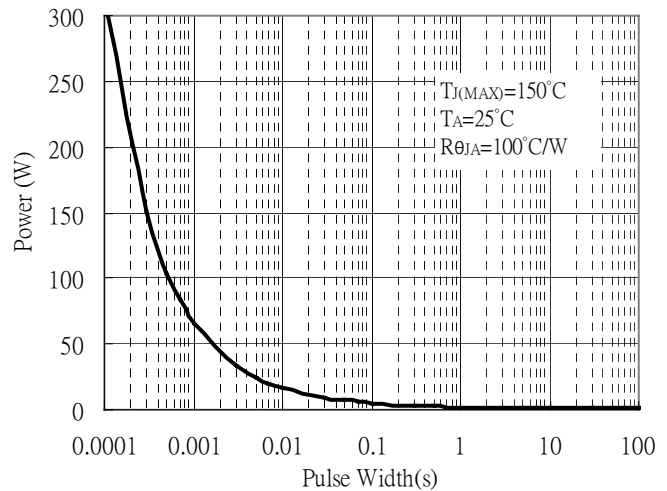
Gate Charge Characteristics



Forward Transfer Admittance vs Drain Current

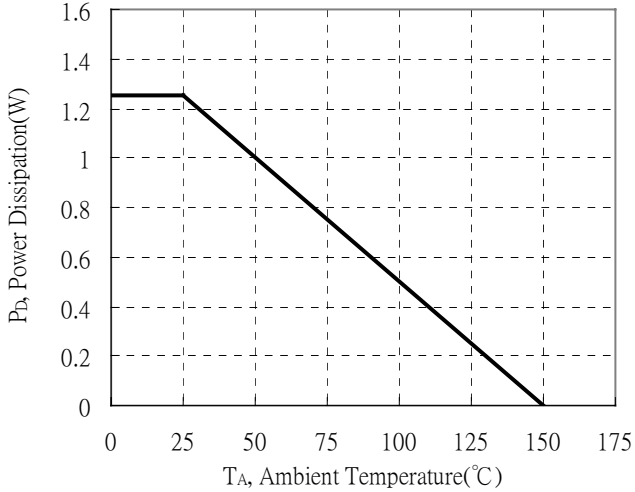


Single Pulse Power Rating, Junction to Case

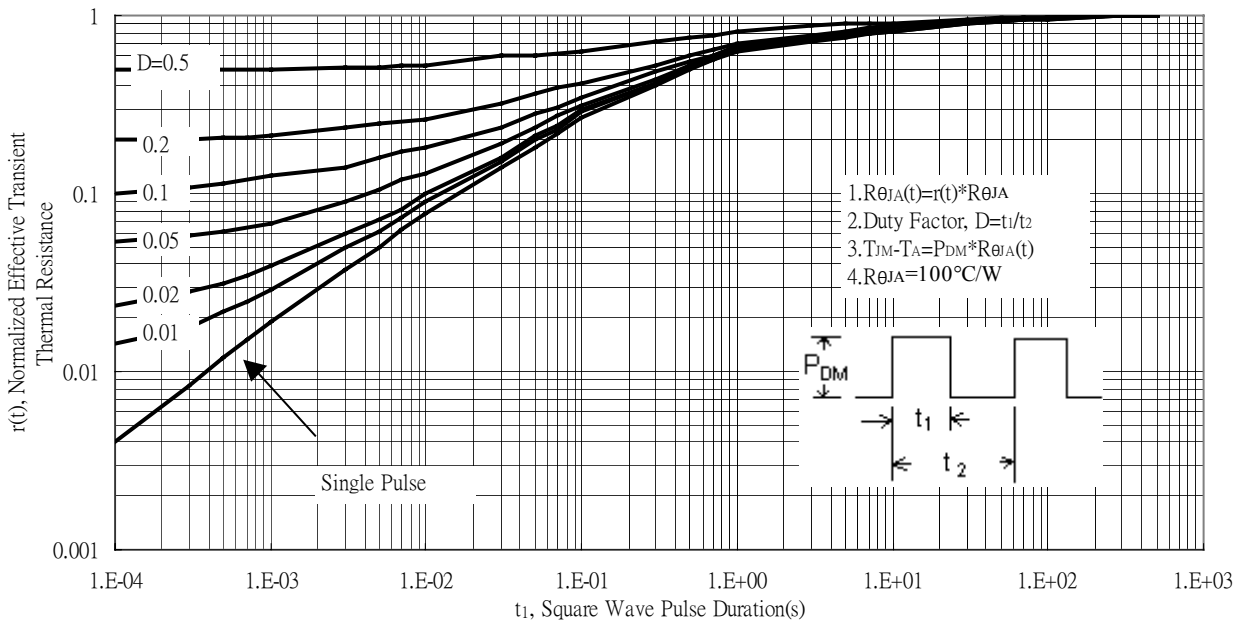


Typical Characteristics(Cont.)

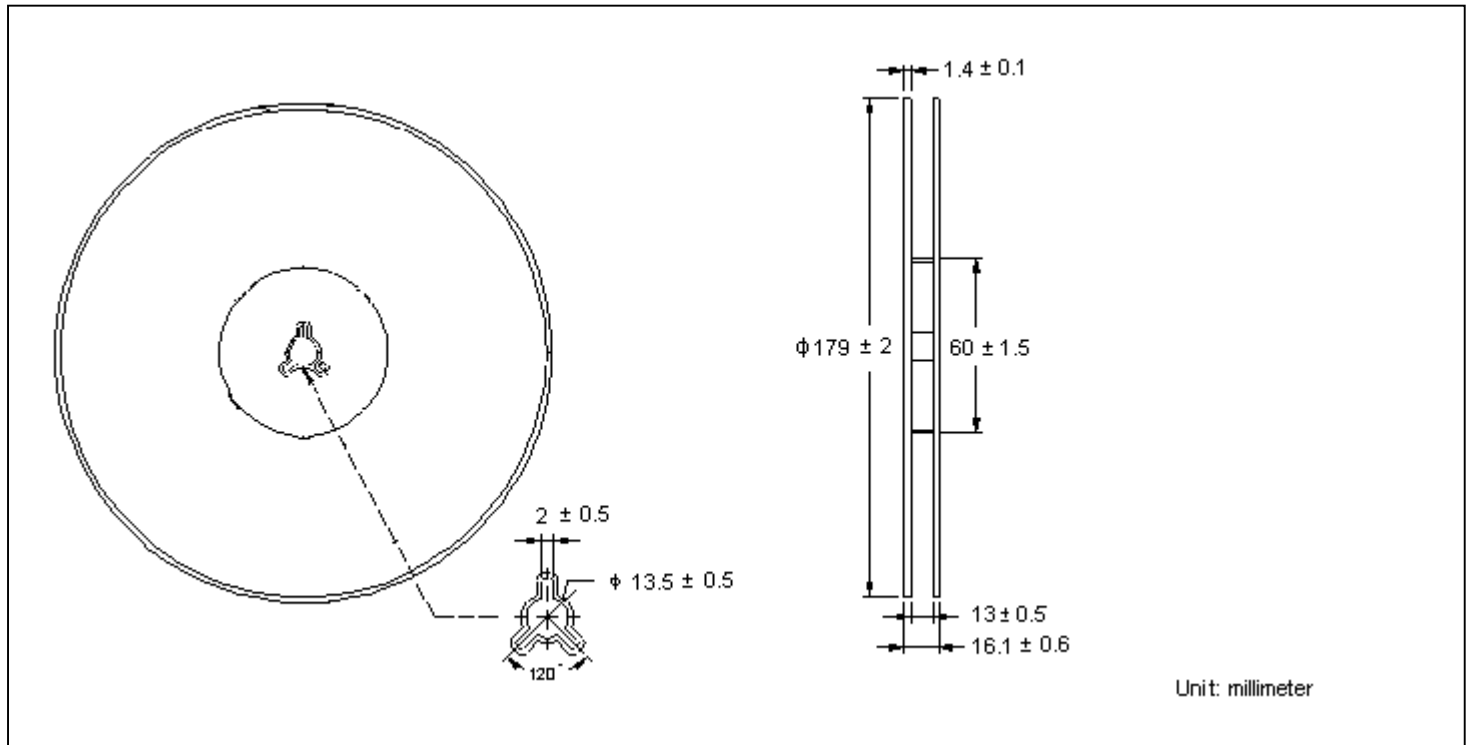
Power Derating Curve



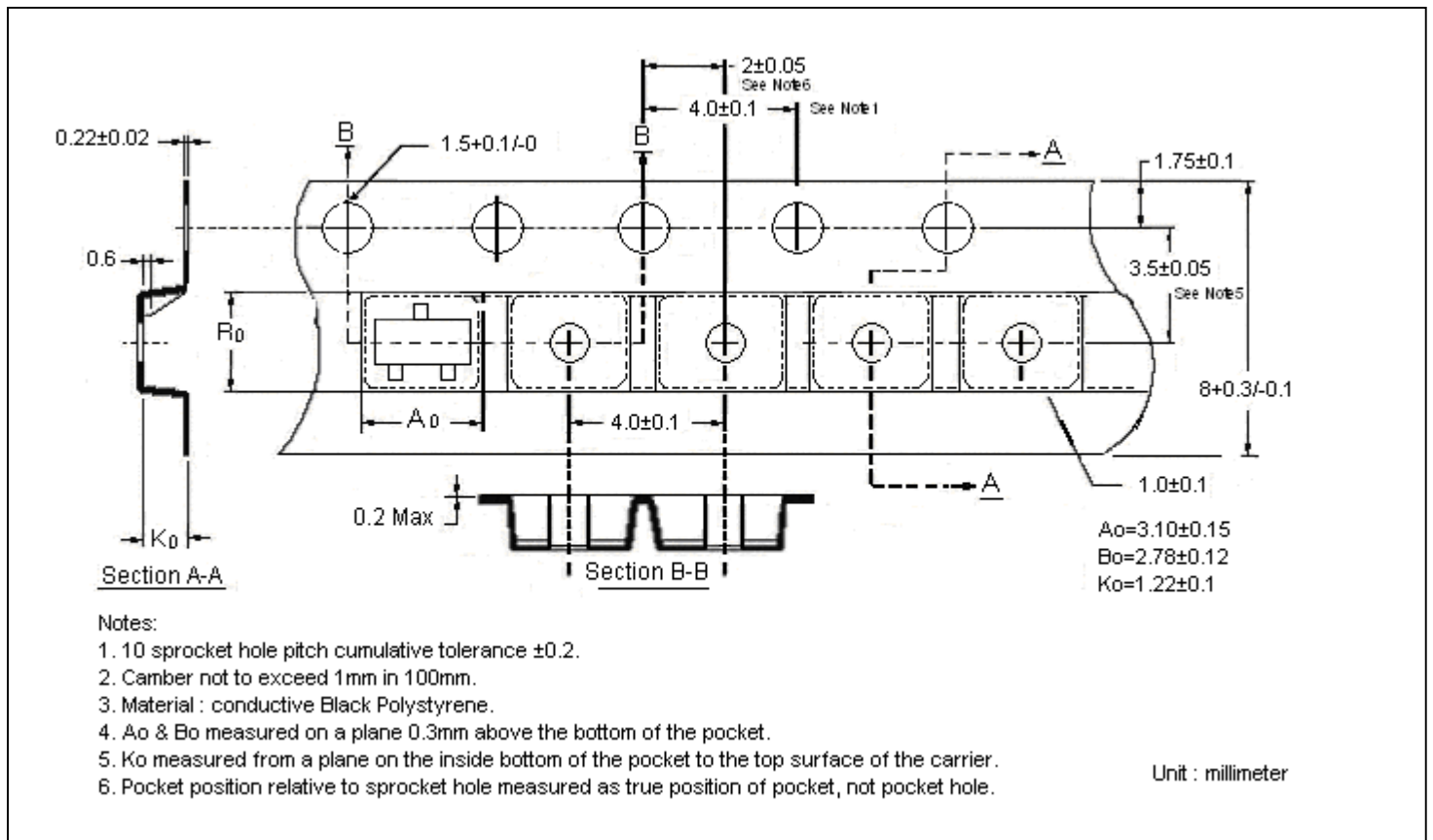
Transient Thermal Response Curves



Reel Dimension

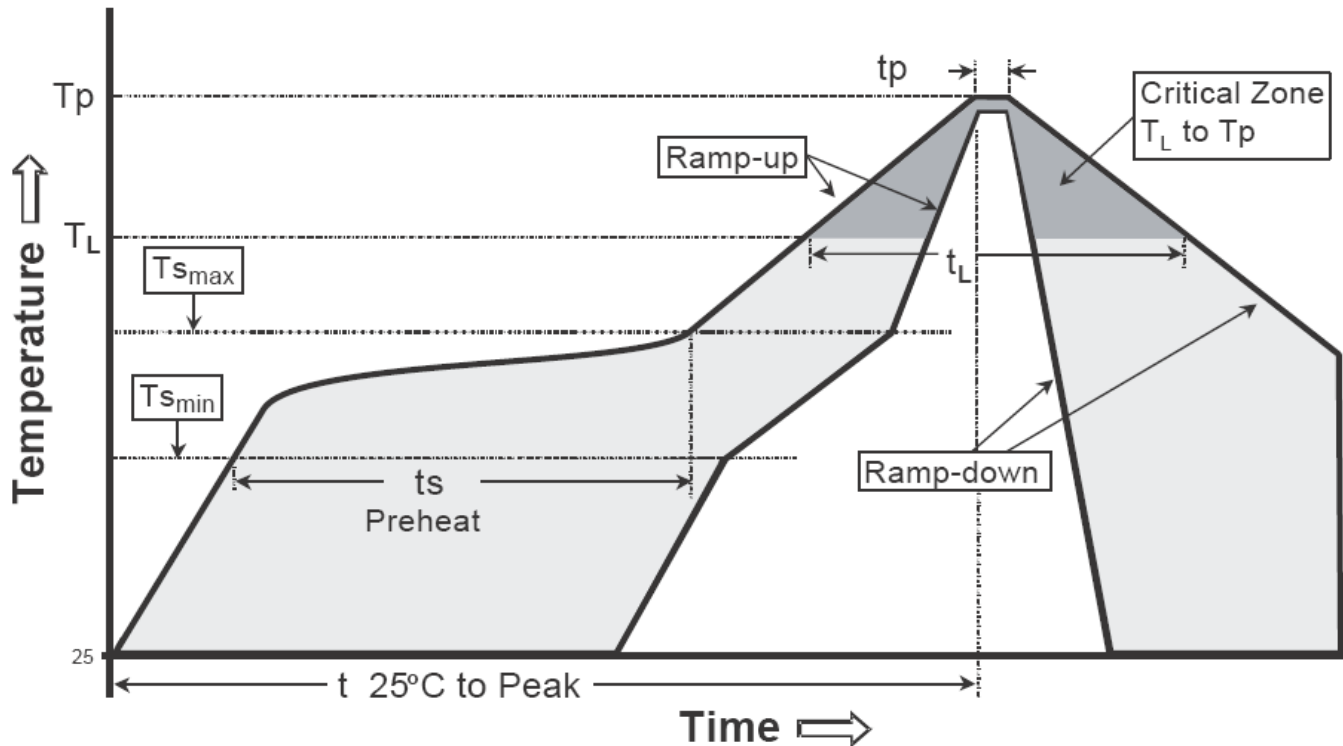


Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

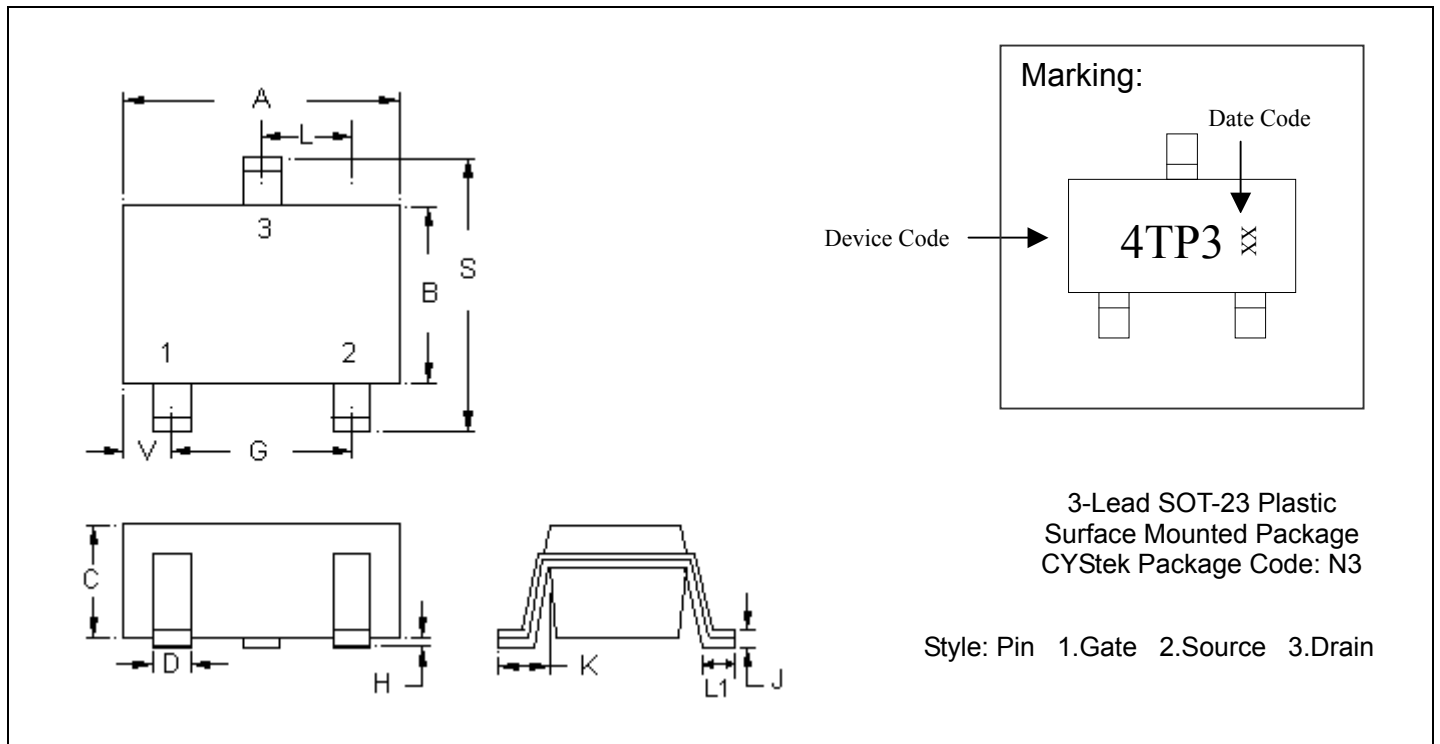
Recommended temperature profile for IR reflow


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _s max to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _s min)	100°C	150°C
-Temperature Max(T _s max)	150°C	200°C
-Time(t _s min to t _s max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note :1. All temperatures refer to topside of the package, measured on the package body surface.

2. For devices mounted on FR-4 PCB of 1.6mm or equivalent grade PCB. If other grade PCB is used, care should be taken to match the coefficients of thermal expansion between components and PCB. If they are not matched well, the solder joints may crack or the bodies of the parts may crack or shatter as the assembly cools.

SOT-23 Dimension



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1102	0.1204	2.80	3.04	J	0.0032	0.0079	0.08	0.20
B	0.0472	0.0669	1.20	1.70	K	0.0118	0.0266	0.30	0.67
C	0.0335	0.0512	0.89	1.30	L	0.0335	0.0453	0.85	1.15
D	0.0118	0.0197	0.30	0.50	S	0.0830	0.1161	2.10	2.95
G	0.0669	0.0910	1.70	2.30	V	0.0098	0.0256	0.25	0.65
H	0.0000	0.0040	0.00	0.10	L1	0.0118	0.0197	0.30	0.50

- Notes:**
- 1.Controlling dimension: millimeters.
 - 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 - 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.