

Dual N-CHANNEL ENHANCEMENT MODE POWER MOSFET

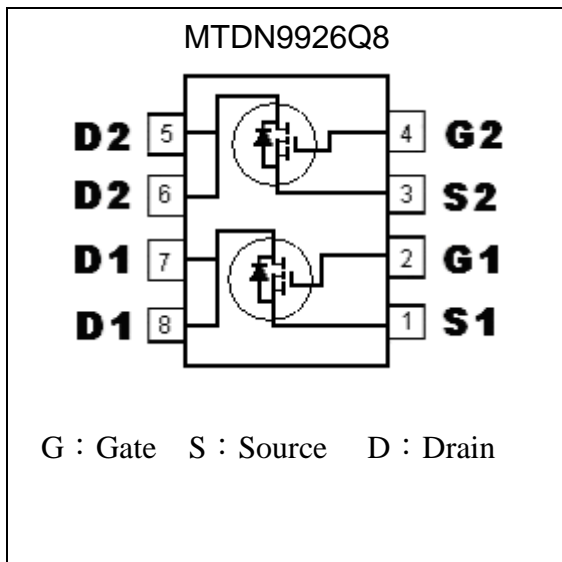
MTDN9926Q8

BV_{DSS}	20V
$I_D @ V_{GS}=4.5V, T_A=25^\circ C$	7.4A
$R_{DS(ON)} @ V_{GS}=4.5V, I_D=6A$	13mΩ (typ.)

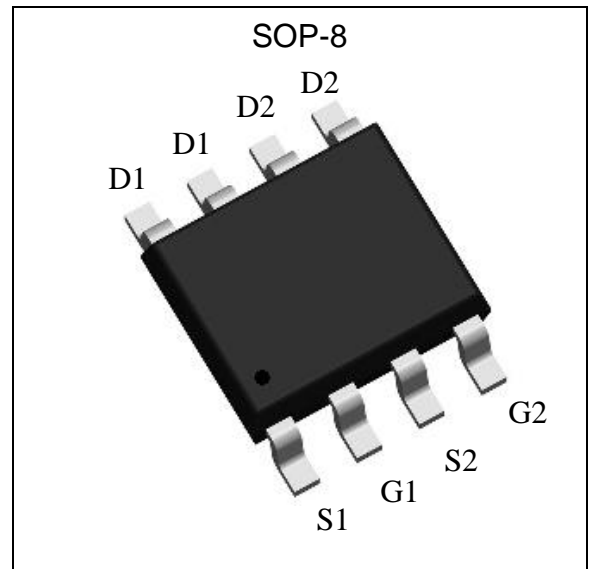
Features

- $R_{DS(ON)}=13m\Omega$ typ. @ $V_{GS}=4.5V, I_D=6A$
- Simple drive requirement
- Low on-resistance
- Fast switching speed
- Capable of 2.5V gate drive
- Pb-free lead plating package

Equivalent Circuit

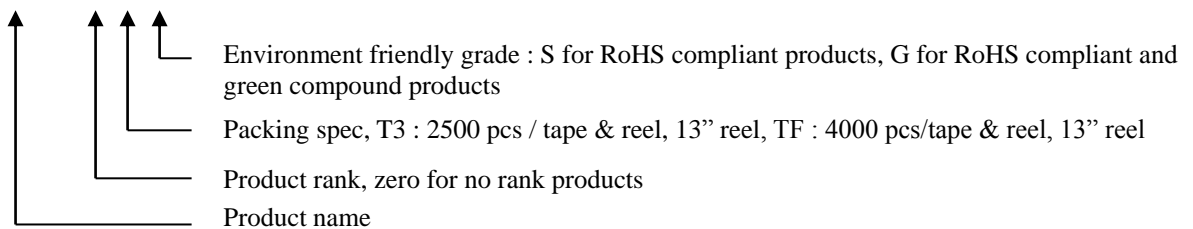


Outline



Ordering Information

Device	Package	Shipping
MTDN9926Q8-0-T3-G	SOP-8 (Pb-free lead plating and halogen-free package)	2500 pcs / tape & reel
MTDN9926Q8-0-TF-G	SOP-8 (Pb-free lead plating and halogen-free package)	4000 pcs / tape & reel





Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	±8	
Continuous Drain Current @ V _{GS} =4.5V, T _A =25 °C (Note 1)	I _D	7.4	A
Continuous Drain Current @ V _{GS} =4.5V, T _A =70 °C (Note 1)		5.9	
Pulsed Drain Current (Note 2&3)	I _{DM}	30	
Total Power Dissipation @ T _A =25 °C Linear Derating Factor	P _d	2	W
			0.016
Operating Junction and Storage Temperature Range	T _j , T _{stg}	-55~+150	°C
Thermal Resistance, Junction-to-Ambient (Note 1)	R _{th,ja}	62.5	°C/W

Note : 1. Surface mounted on 1 in² copper pad of FR-4 board; 135°C/W when mounted on minimum copper pad
 2. Pulse width limited by maximum junction temperature.
 3. Pulse width ≤ 300µs, duty cycle ≤ 2%

Characteristics (Tj=25°C, unless otherwise specified)

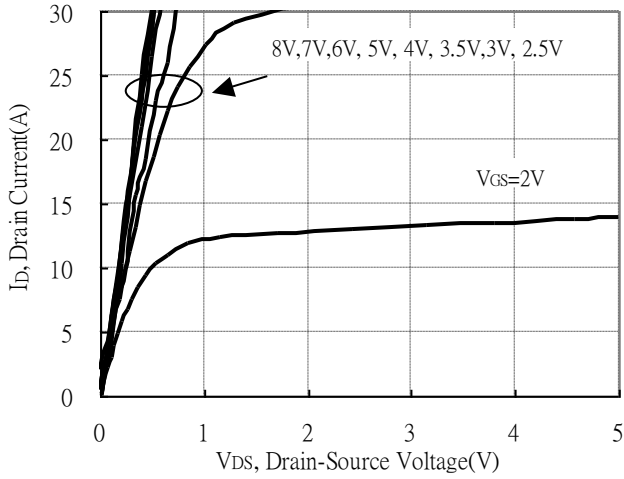
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
B _V D _{SS}	20	-	-	V	V _{GS} =0V, I _D =250µA
ΔB _V D _{SS} /ΔT _j	-	0.02	-	V/°C	Reference to 25°C, I _D =1mA
V _{GS(th)}	0.5	-	1.2	V	V _{DS} = V _{GS} , I _D =250µA
G _{FS}	-	9	-	S	V _{DS} =10V, I _D =6A
I _{GSS}	-	-	±100	nA	V _{GS} =±8V, V _{DS} =0V
I _{DSS}	-	-	1	µA	V _{DS} = 16V, V _{GS} = 0V
	-	-	25		V _{DS} = 16V, V _{GS} = 0V, T _j =70°C
*R _{DS(ON)}	-	13	20	mΩ	I _D =6A, V _{GS} =4.5V
	-	18	32		I _D =5.2A, V _{GS} =2.5V
Dynamic					
*Q _g	-	9.9	-	nC	V _{DS} =10V, I _D =5A, V _{GS} =4.5V
*Q _{gs}	-	1.3	-		
*Q _{gd}	-	3	-		
*t _{d(ON)}	-	8.8	-	ns	V _{DS} =10V, I _D =1A, V _{GS} =4.5V, R _G =10Ω
*t _r	-	21.8	-		
*t _{d(OFF)}	-	59.4	-		
*t _f	-	27	-		
C _{iss}	-	703	-	pF	V _{DS} =20V, V _{GS} =0V, f=1MHz
C _{oss}	-	73	-		
C _{rss}	-	62	-		
Source-Drain Diode					
*V _{SD}	-	0.79	1.2	V	I _S =1.7A, V _{GS} =0V
*I _S	-	-	1.54	A	V _D =V _G =0V, V _S =1.3V
*t _{rr}	-	8.3	-	ns	I _F =1A, dI _F /dt=100A/µs
*Q _{rr}	-	3.1	-	nC	

*Pulse Test : Pulse Width ≤ 300µs, Duty Cycle ≤ 2%

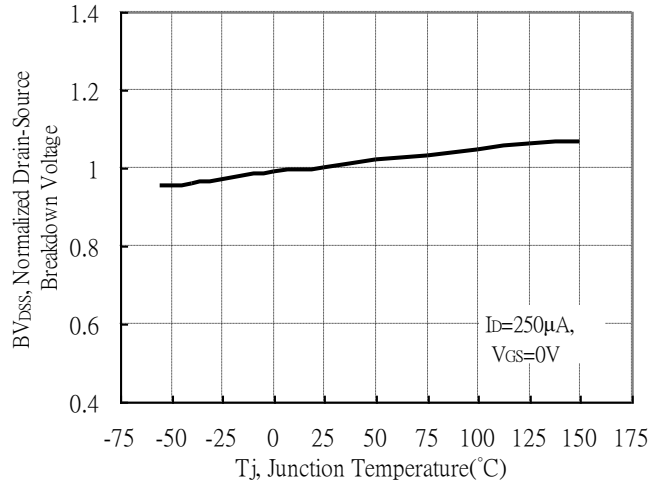


Typical Characteristics

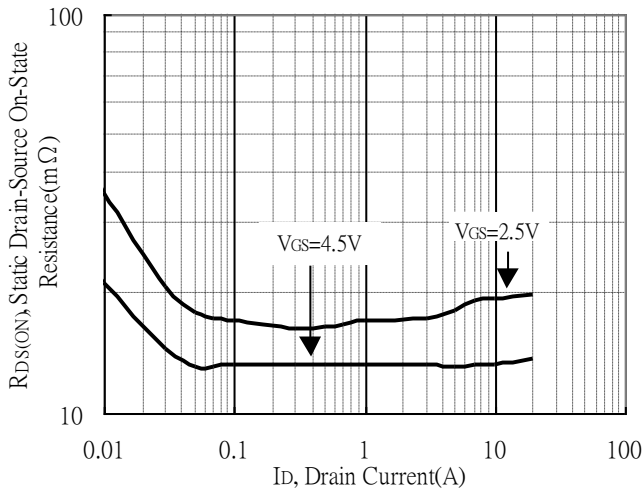
Typical Output Characteristics



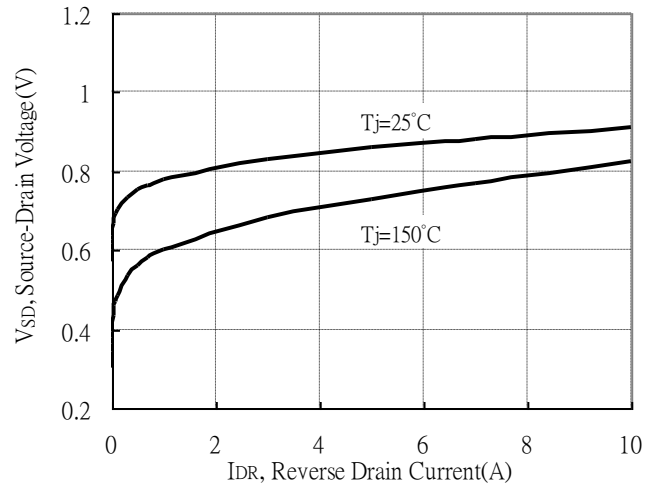
Brekdown Voltage vs Ambient Temperature



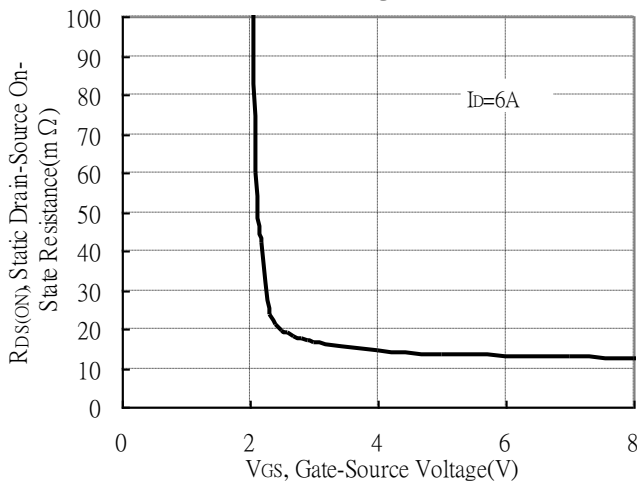
Static Drain-Source On-State resistance vs Drain Current



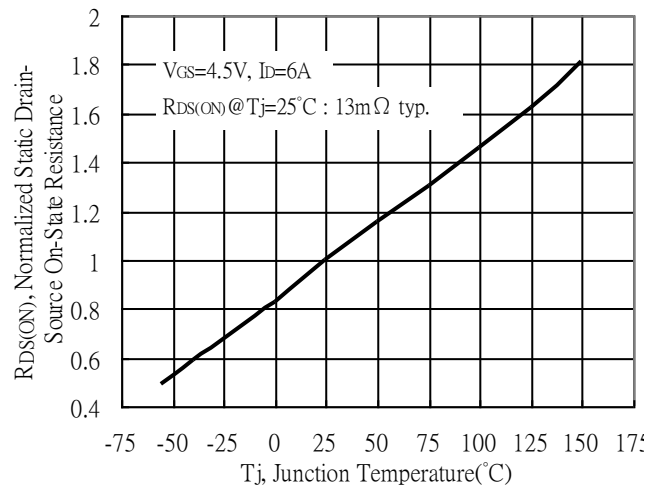
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

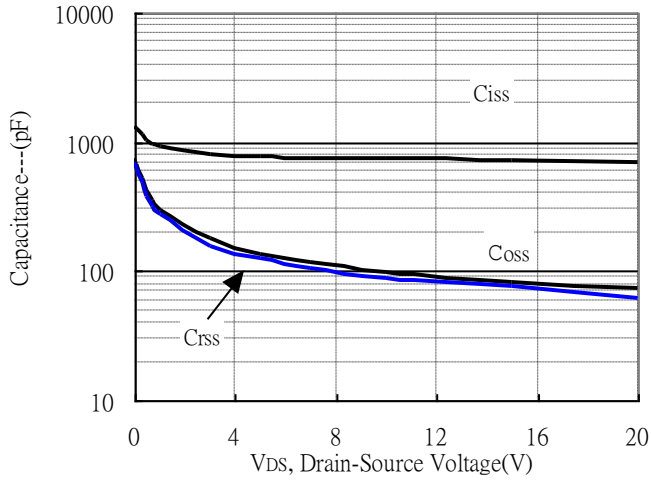


Drain-Source On-State Resistance vs Junction Temperature

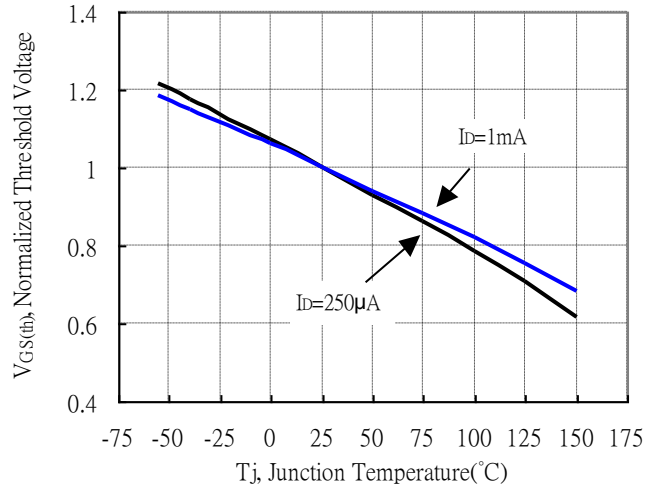


Typical Characteristics(Cont.)

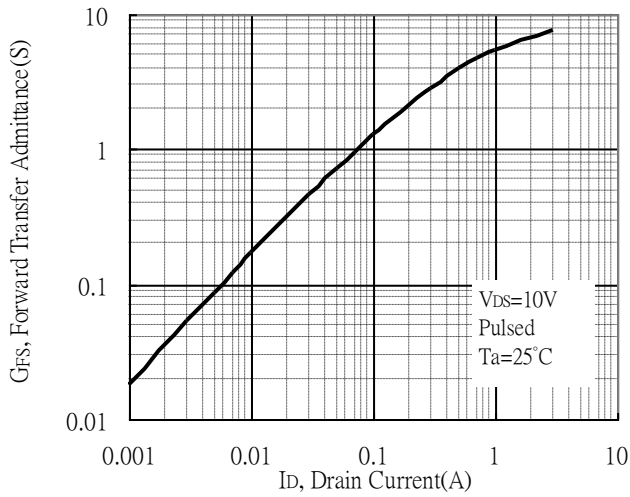
Capacitance vs Drain-to-Source Voltage



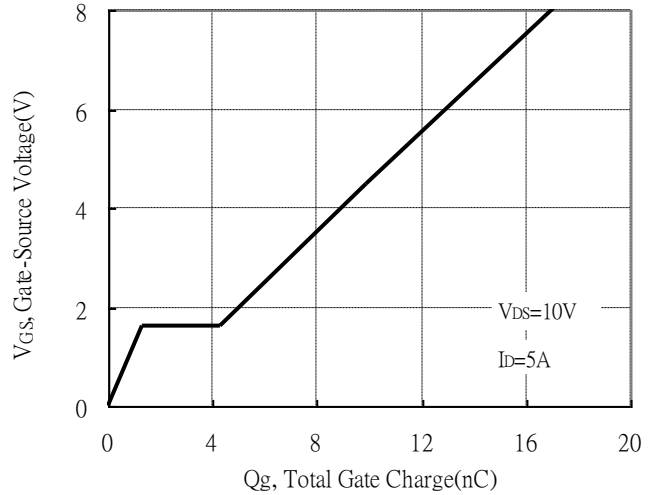
Threshold Voltage vs Junction Temperature



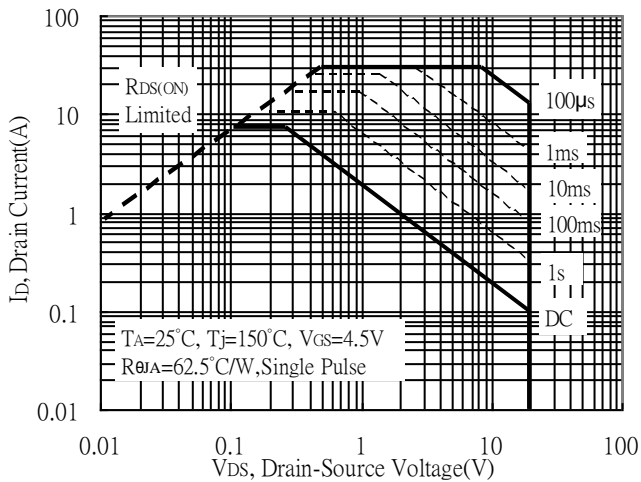
Forward Transfer Admittance vs Drain Current



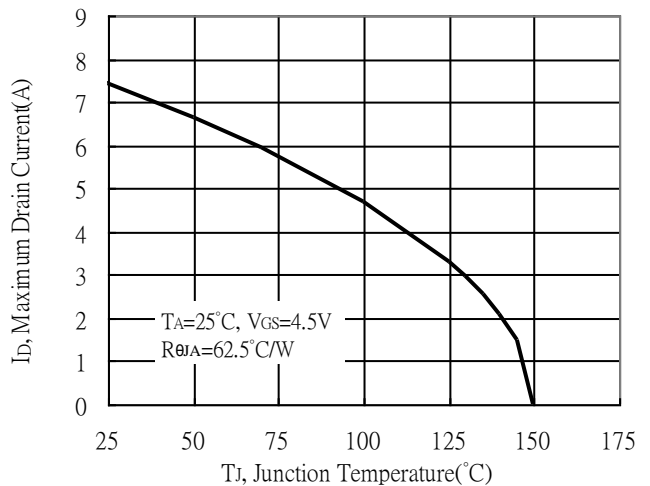
Gate Charge Characteristics



Maximum Safe Operating Area

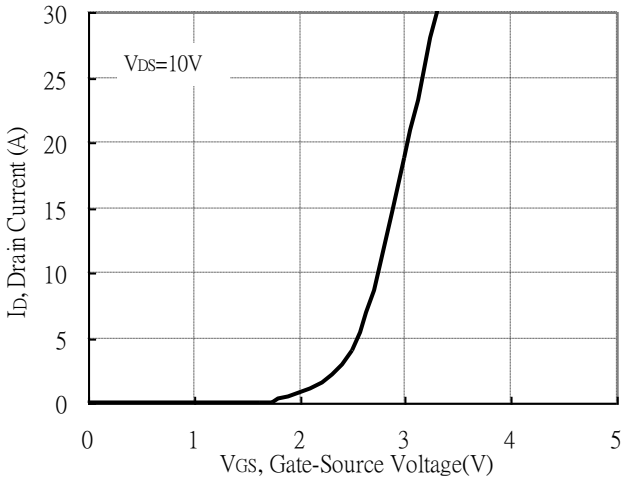


Maximum Drain Current vs Junction Temperature

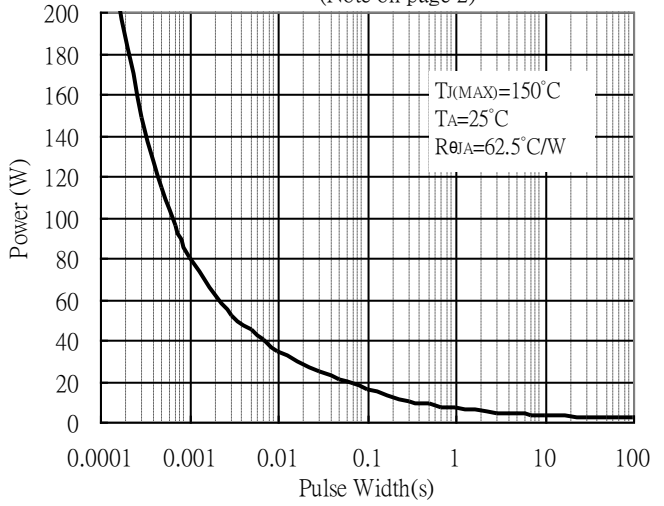


Typical Characteristics(Cont.)

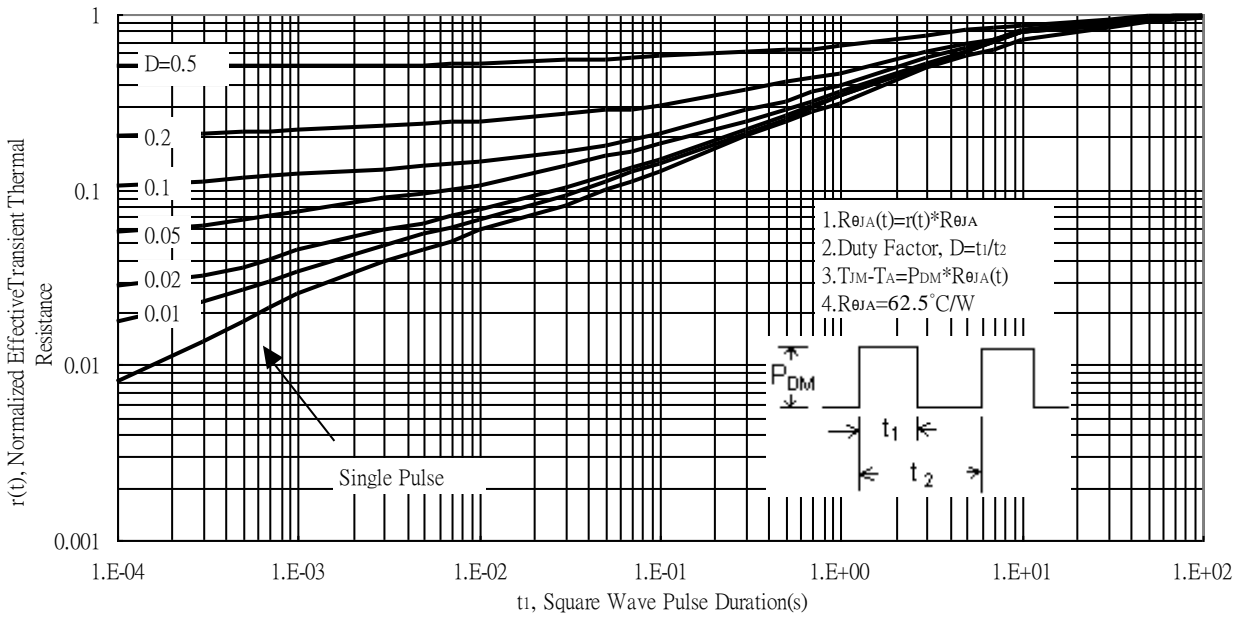
Typical Transfer Characteristics



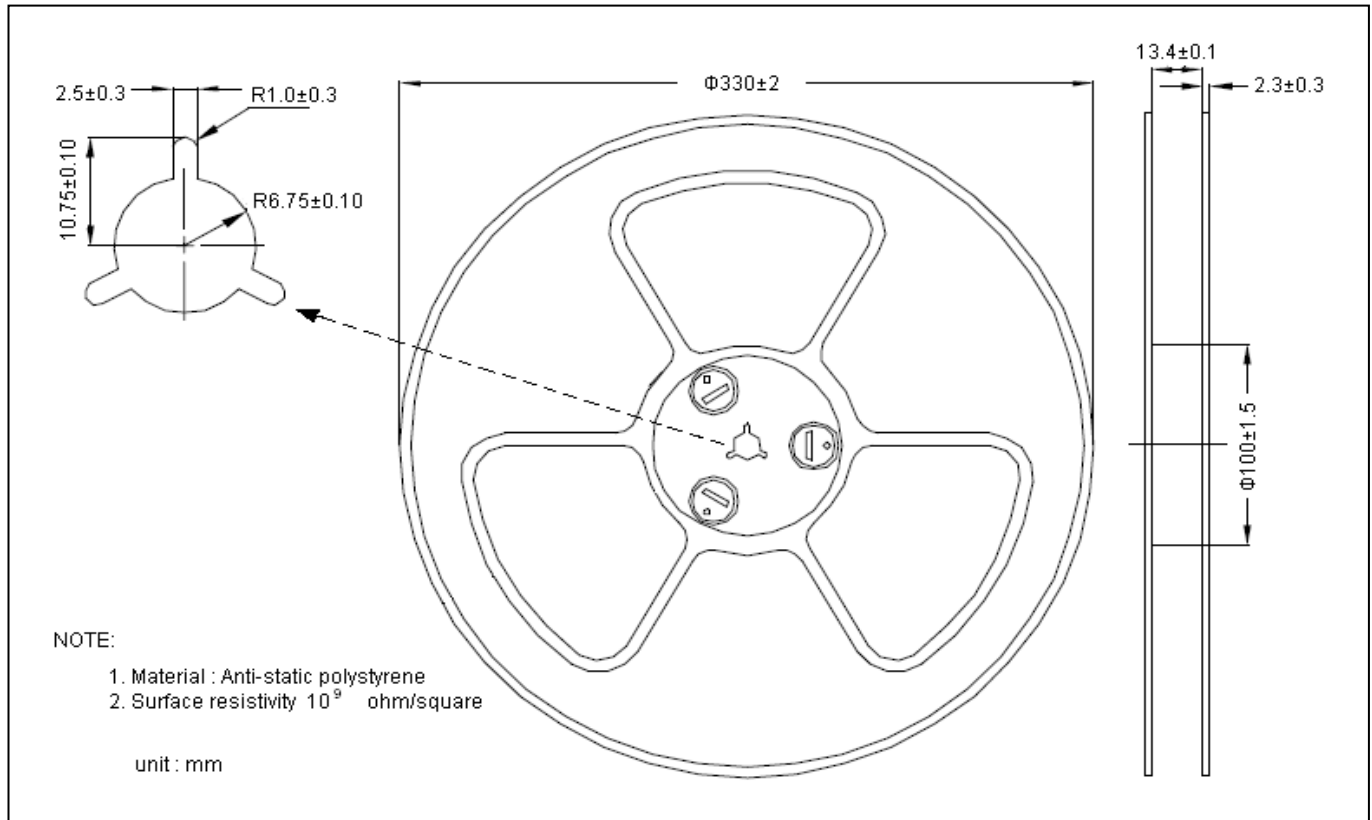
Single Pulse Power Rating, Junction to Ambient
 (Note on page 2)



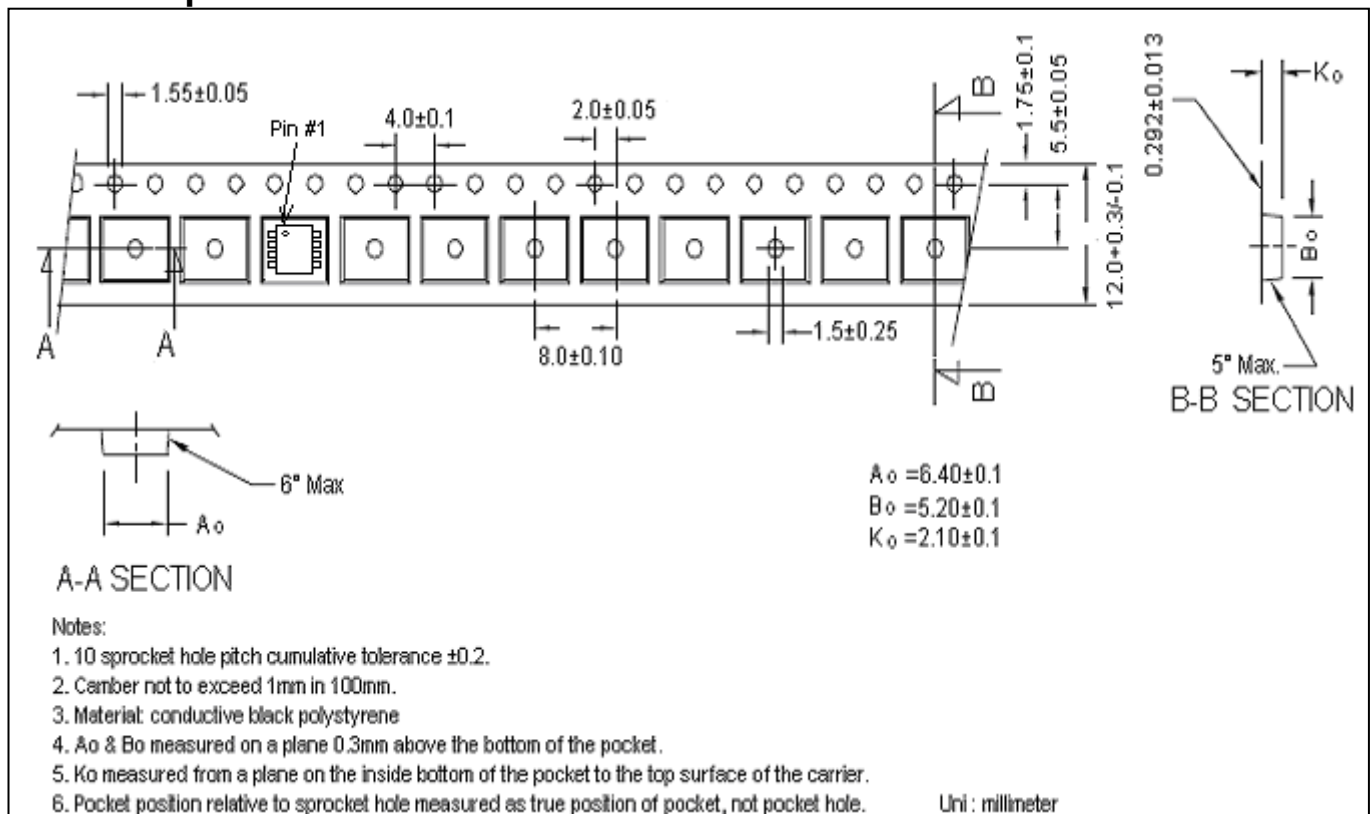
Transient Thermal Response Curves



Reel Dimension



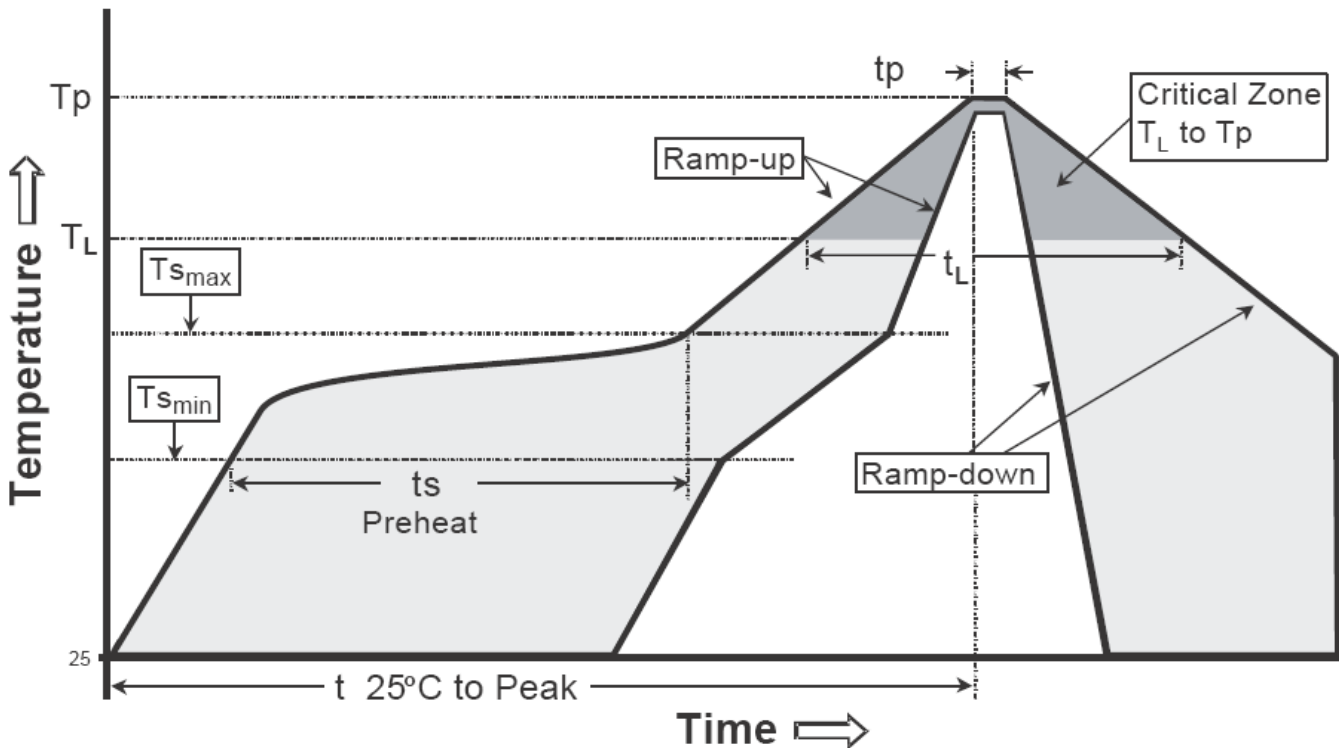
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

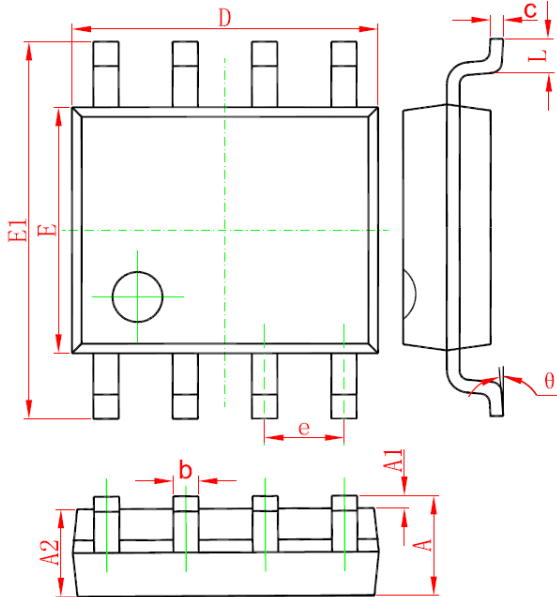
Recommended temperature profile for IR reflow



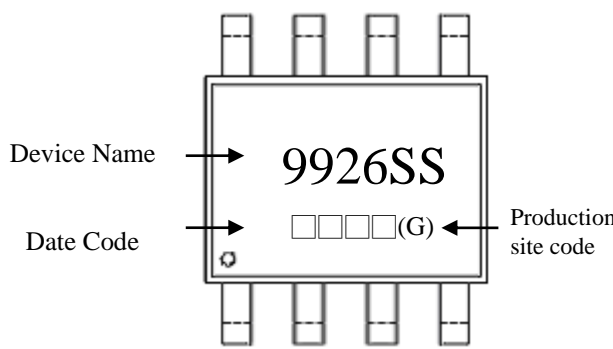
Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

SOP-8 Dimension



Marking:



Device Name → **9926SS**

Date Code → □□□□(G) ← Production site code

Date Code(counting from left to right) :

1st code: year code, the last digit of Christian year

2nd code : month code, Jan→A, Feb→B, Mar→C, Apr→D
 May→E, Jun→F, Jul→G, Aug→H, Sep→J,
 Oct→K, Nov→L, Dec→M

3rd and 4th codes : production serial number, 01~99

Production site code : blank→ JCET, G →GEM

8-Lead SOP-8 Plastic Package
 CYStek Package Code: Q8

*: Typical

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069	E	3.800	4.000	0.150	0.157
A1	0.100	0.250	0.004	0.010	E1	5.800	6.200	0.228	0.244
A2	1.350	1.550	0.053	0.061	e	*1.270		*0.050	
b	0.330	0.510	0.013	0.020	L	0.400	1.270	0.016	0.050
c	0.170	0.250	0.006	0.010	θ	0°	8°	0°	8°
D	4.700	5.100	0.185	0.200					

- Notes:** 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.