

Dual N -Channel Enhancement Mode MOSFET

MTDN8233X6

BV_{DSS}		20V
I_D	$V_{GS}=4.5V, T_A=25^\circ C$	11A
$R_{DSON} (TYP.)$	$V_{GS}=4.5V, I_D=5.5A$	6.0m Ω
	$V_{GS}=4.0V, I_D=5.5A$	6.0m Ω
	$V_{GS}=3.7V, I_D=5.5A$	6.2 m Ω
	$V_{GS}=3.1V, I_D=5.5A$	6.7 m Ω
	$V_{GS}=2.5V, I_D=5.5A$	7.8 m Ω

Description

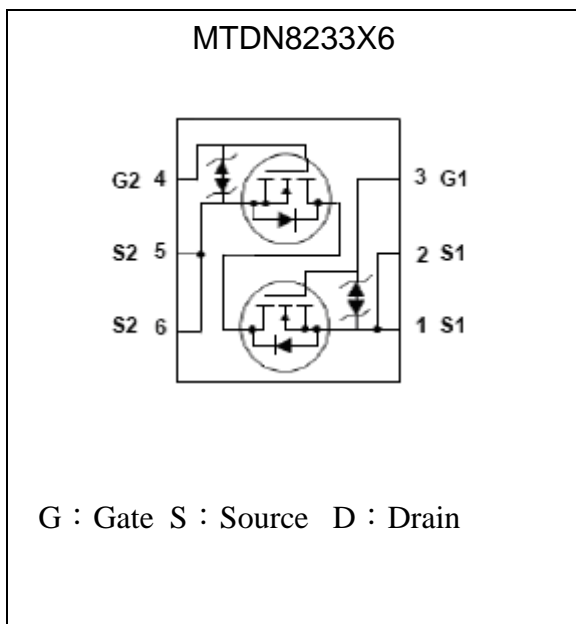
The MTDN8233X6 consists of two N-channel enhancement-mode MOSFETs in a single TDFN2x3-6L package, providing the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TDFN2x3-6L package is universally preferred for all commercial-industrial surface mount applications.

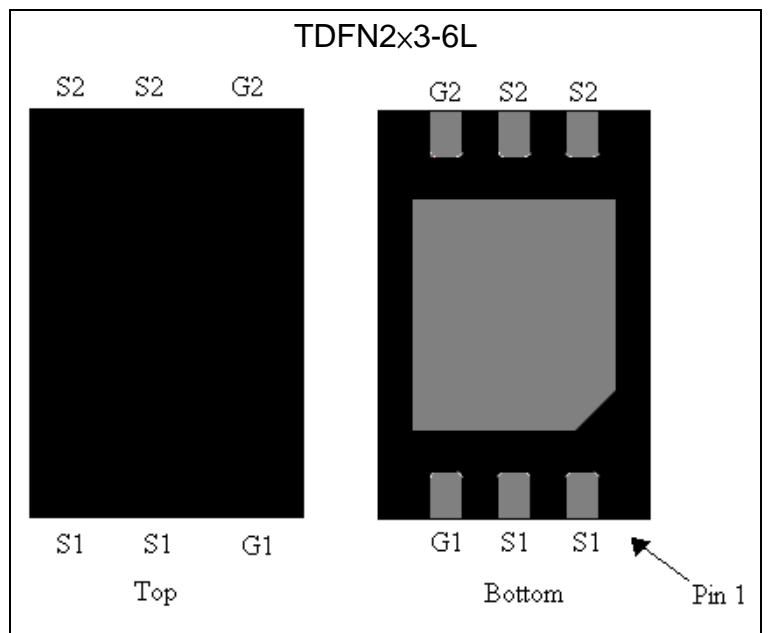
Features

- Simple drive requirement
- Low gate charge
- Low on-resistance
- Fast switching speed
- ESD protected
- Pb-free lead plating and halogen-free package

Equivalent Circuit



Outline





Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	20	V
Gate-Source Voltage	V _{GS}	±8	
Continuous Drain Current (Note 1)	I _D	T _A =25 °C, V _{GS} =4.5V	11
		T _A =70 °C, V _{GS} =4.5V	8.8
Pulsed Drain Current (Note 2)	I _{DM}	70	A
Total Power Dissipation (Note 1)	P _D	T _A =25 °C	1.56
		T _A =70 °C	1.00
Operating Junction and Storage Temperature	T _j , T _{stg}	-55~+150	°C

Note : 1.Surface mounted on 1 in² copper pad of FR-4 board, t≤10 sec
 2.Pulse width limited by maximum junction temperature

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-ambient, max	R _{θJA}	80 (Note)	°C/W

Note : Surface mounted on 1 in² copper pad of FR-4 board, t≤10 sec; 161°C/W when mounted on minimum copper pad

Electrical Characteristics (Tj=25°C, unless otherwise specified)

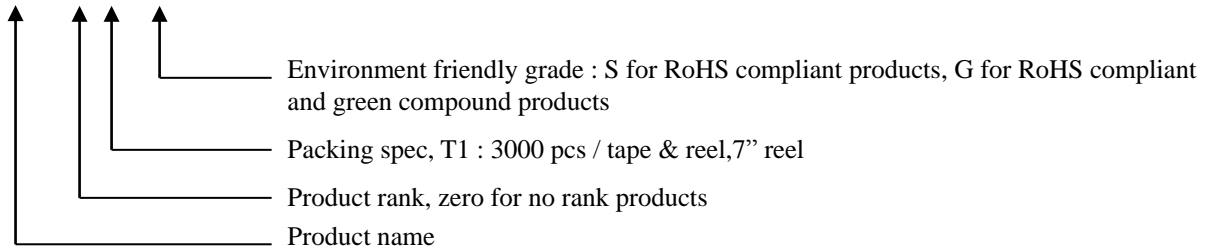
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	20	-	-	V	V _{GS} =0V, I _D =250μA
ΔBV _{DSS} /ΔT _j	-	0.02	-	V/°C	Reference to 25°C, I _D =1mA
V _{GS(th)}	0.5	0.72	1.5	V	V _{DS} =V _{GS} , I _D =1mA
I _{GSS}	-	-	±10	μA	V _{GS} =±8V, V _{DS} =0V
I _{DSS}	-	-	1		V _{DS} =18V, V _{GS} =0V
	-	-	10	V _{DS} =16V, V _{GS} =0V, T _j =70°C	
*R _{DS(ON)}	5.0	6.0	8.2	mΩ	I _D =5.5A, V _{GS} =4.5V
	5.2	6.0	8.5		I _D =5.5A, V _{GS} =4V
	5.4	6.2	9		I _D =5.5A, V _{GS} =3.7V
	5.8	6.7	9.4		I _D =5.5A, V _{GS} =3.1V
	6.0	7.8	11		I _D =5.5A, V _{GS} =2.5V
*G _{FS}	-	20	-	S	V _{DS} =5V, I _D =5.5A
Dynamic					
C _{iss}	-	1350	-	pF	V _{DS} =10V, V _{GS} =0V, f=1MHz
C _{oss}	-	185	-		
C _{rss}	-	160	-		
*t _{d(ON)}	-	28	-	ns	V _{DS} =16V, I _D =5.5A, V _{GS} =4.5V, R _G =6Ω
*t _r	-	64	-		
*t _{d(OFF)}	-	60	-		
*t _f	-	55	-		

*Qg	-	15	-	nC	V _{DS} =16V, I _D =11A, V _{GS} =4.5V
*Qgs	-	2.8	-		
*Qgd	-	4.4	-		
Source-Drain Diode					
*V _{SD}	-	0.82	1.2	V	V _{GS} =0V, I _S =11A

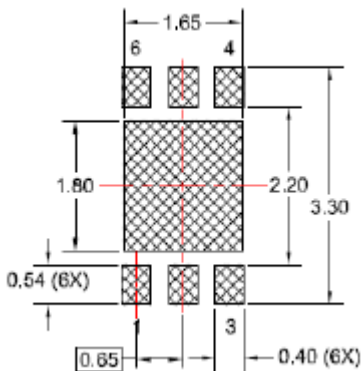
*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Ordering Information

Device	Package	Shipping
MTDN8233X6-0-T1-G	TDFN2x3-6L (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel



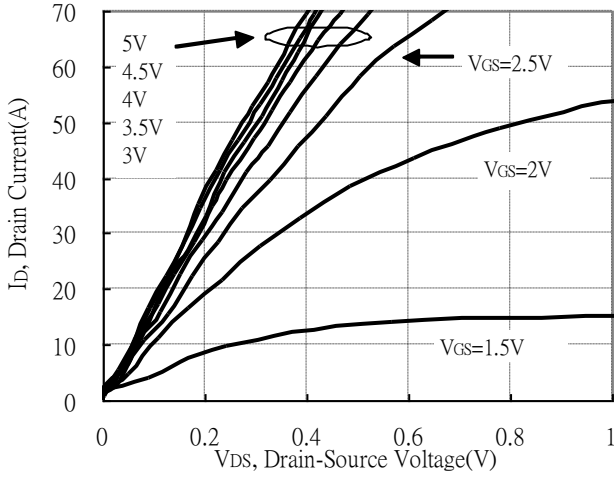
Recommended Soldering Footprint



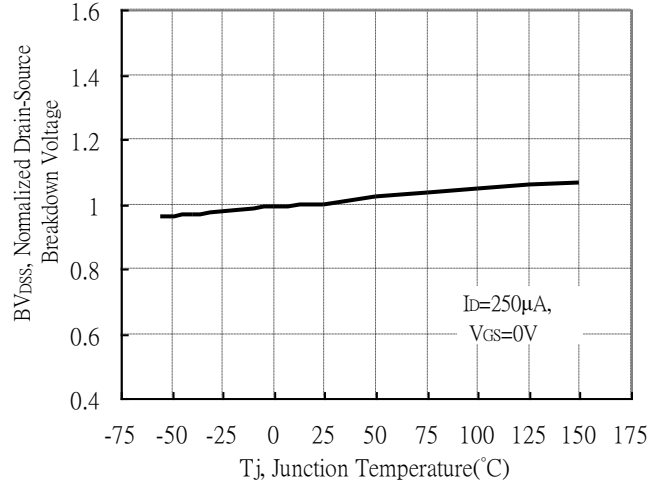
unit : mm

Typical Characteristics

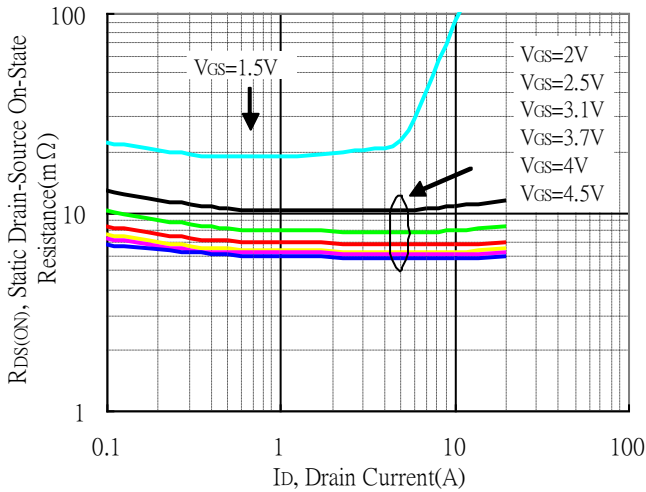
Typical Output Characteristics



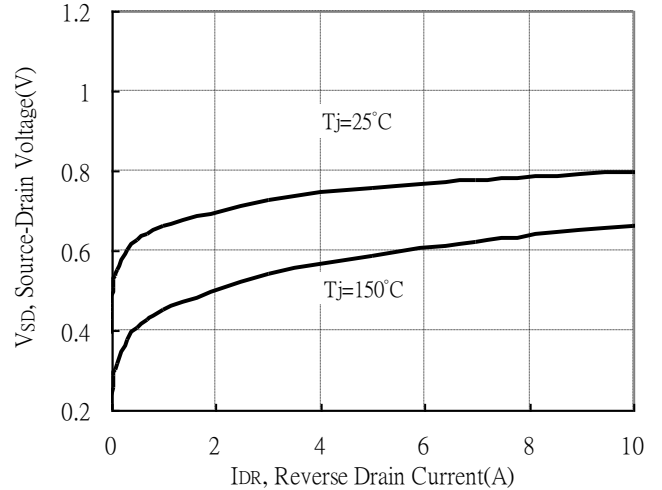
Brekdown Voltage vs Ambient Temperature



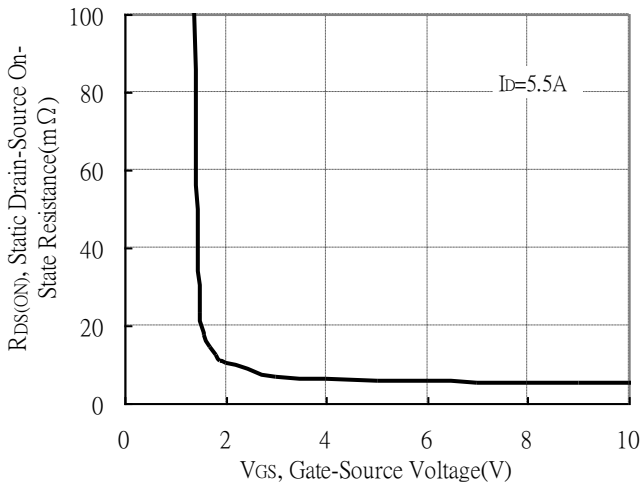
Static Drain-Source On-State resistance vs Drain Current



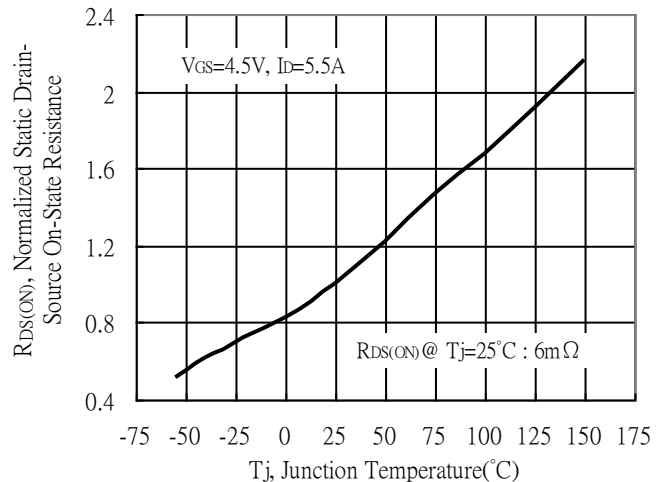
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

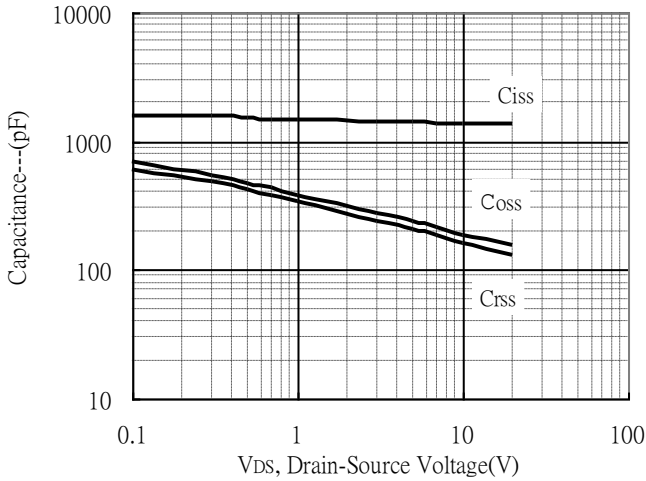


Drain-Source On-State Resistance vs Junction Temperature

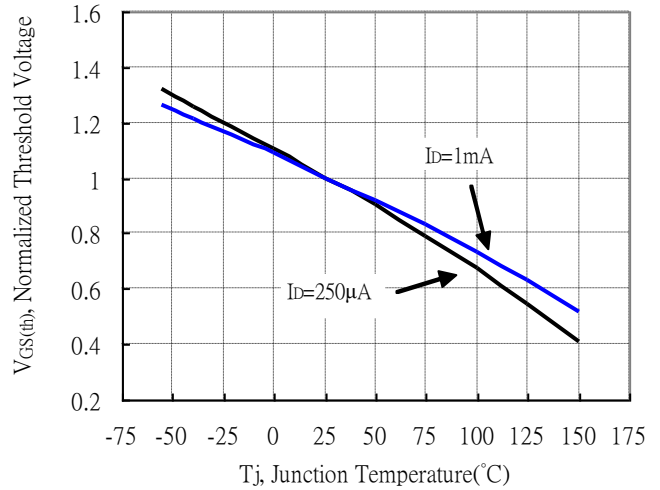


Typical Characteristics(Cont.)

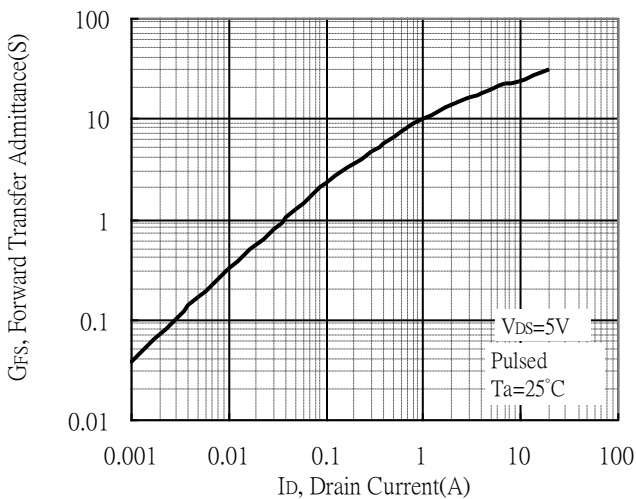
Capacitance vs Drain-to-Source Voltage



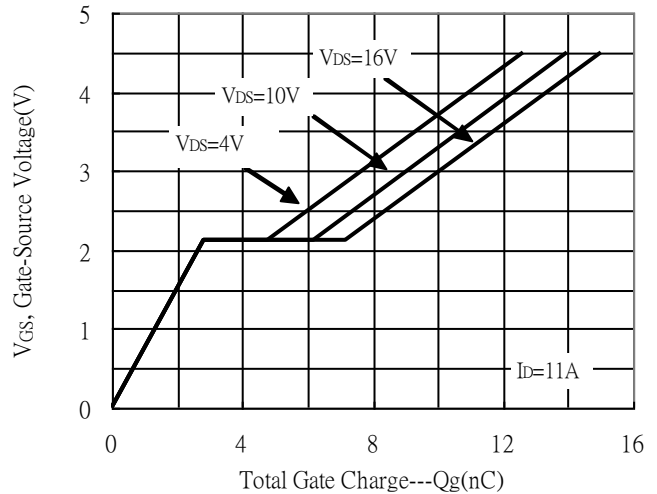
Threshold Voltage vs Junction Temperature



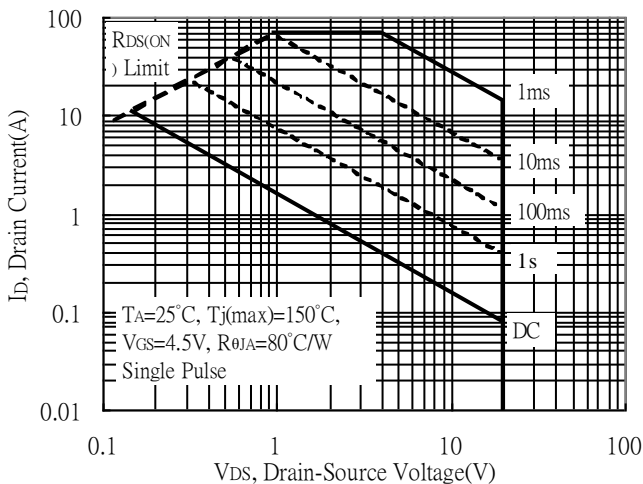
Forward Transfer Admittance vs Drain Current



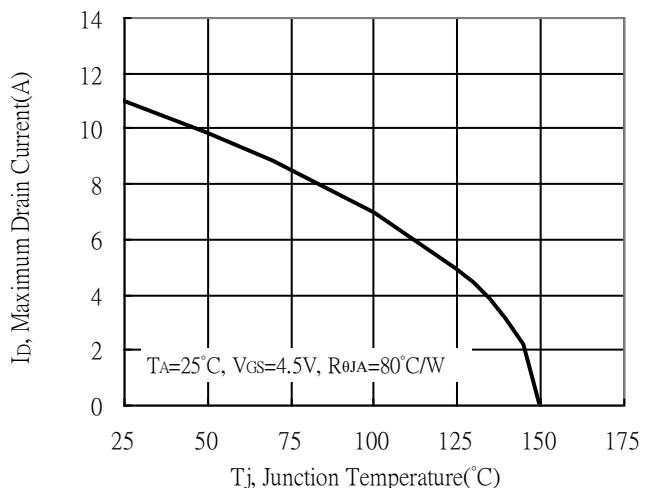
Gate Charge Characteristics



Maximum Safe Operating Area

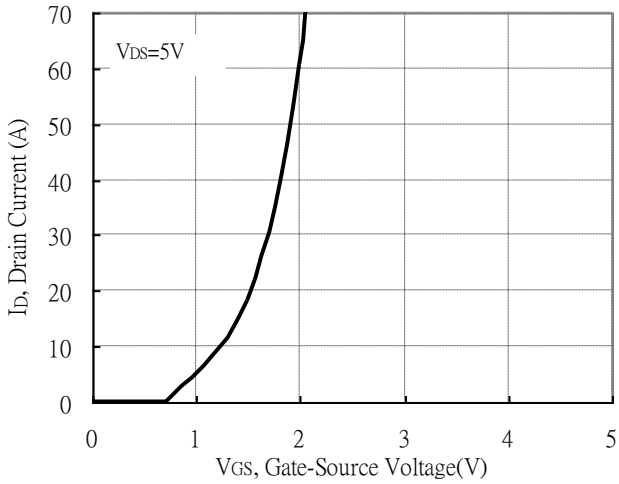


Maximum Drain Current vs Junction Temperature

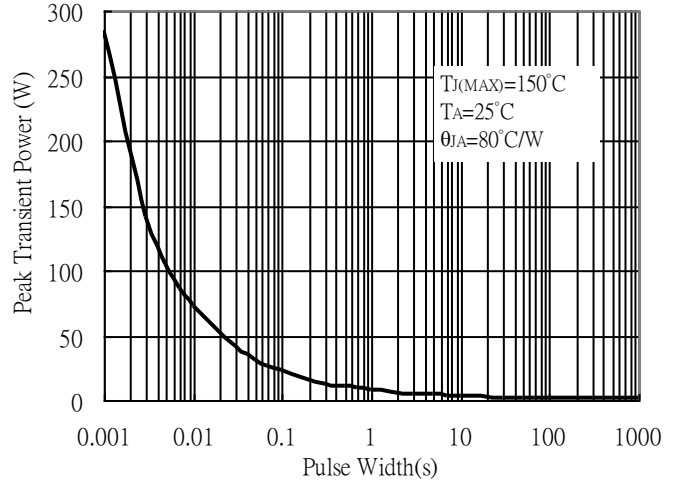


Typical Characteristics(Cont.)

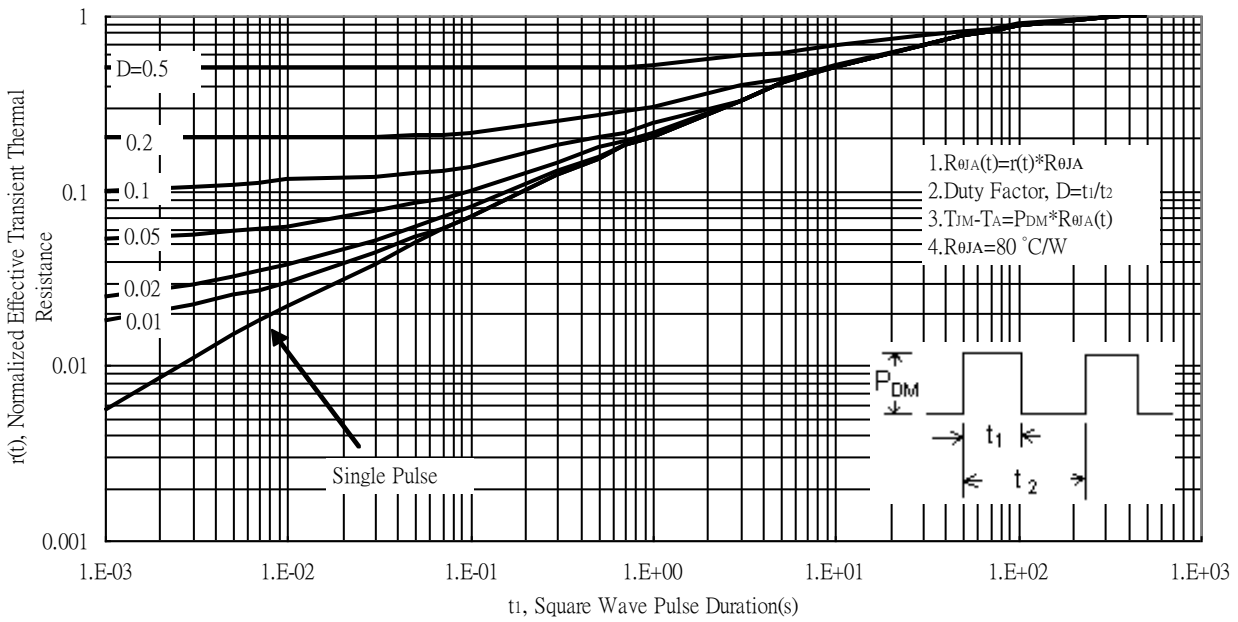
Typical Transfer Characteristics



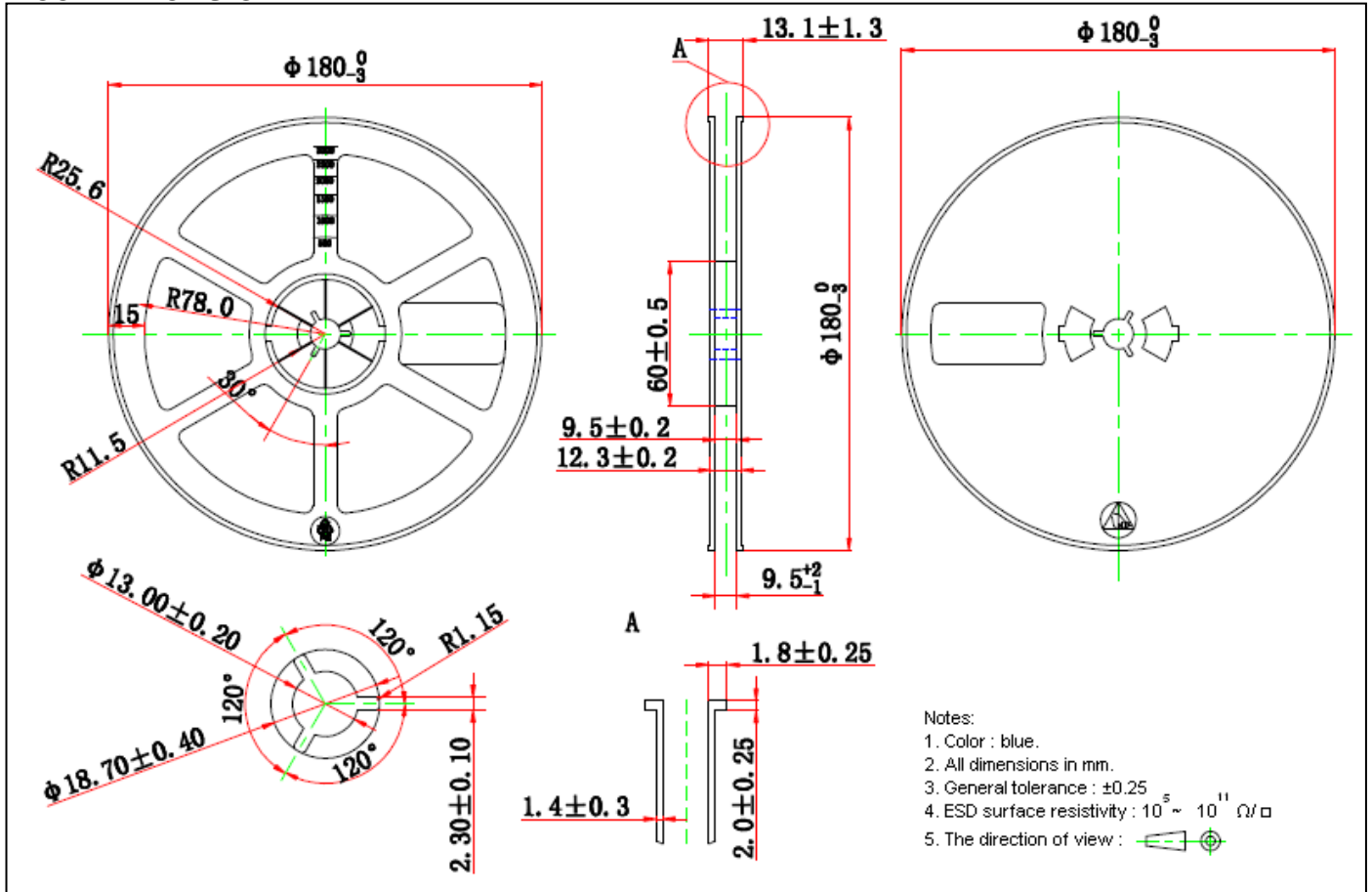
Single Pulse Maximum Power Dissipation



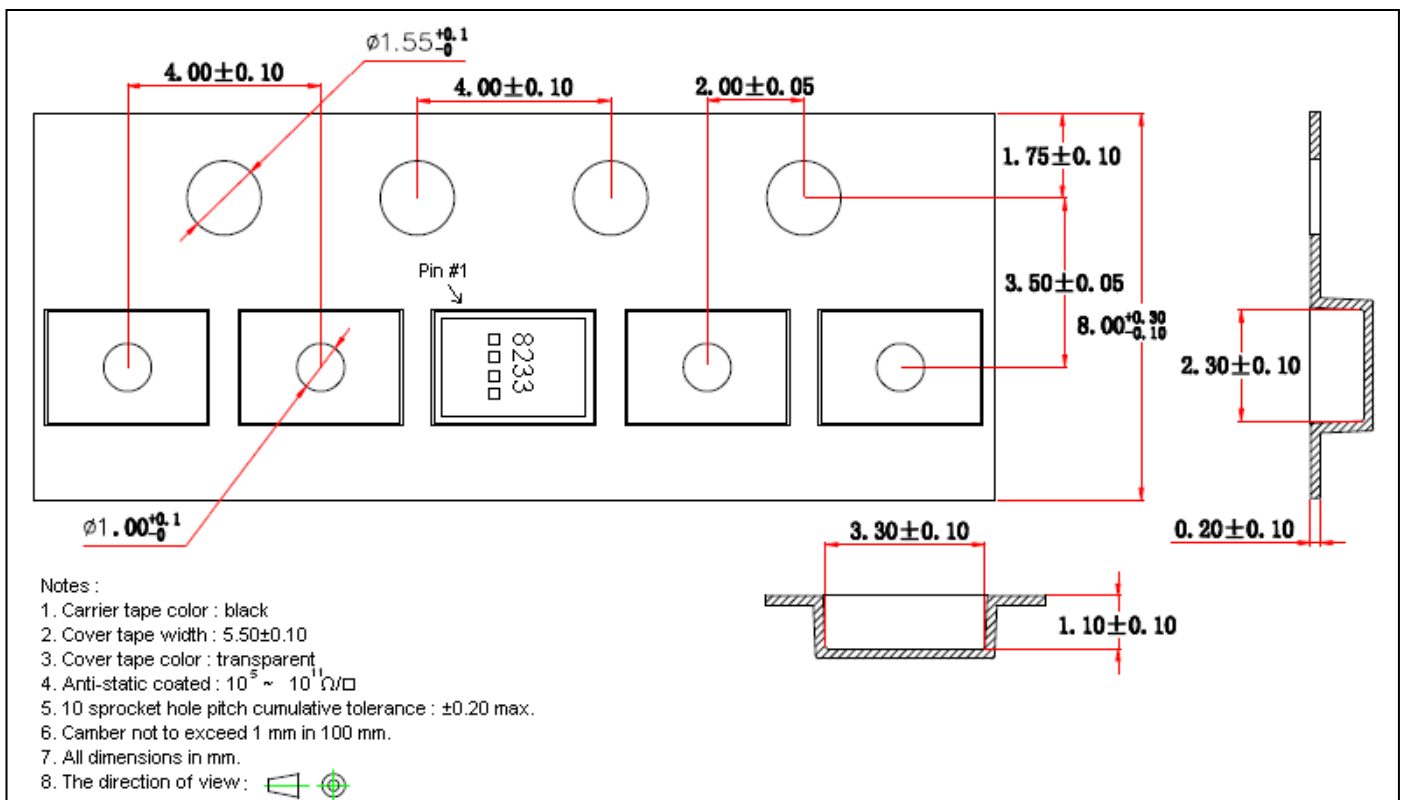
Transient Thermal Response Curves



Reel Dimension



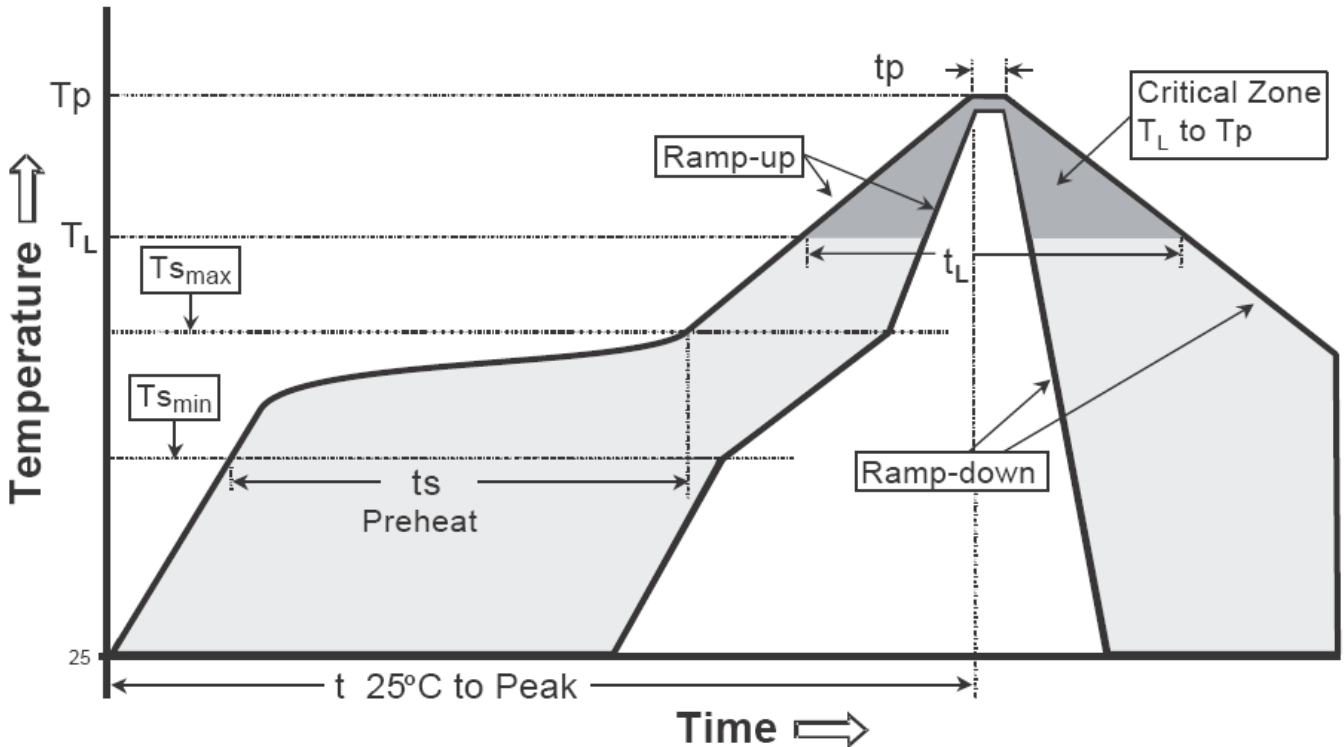
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

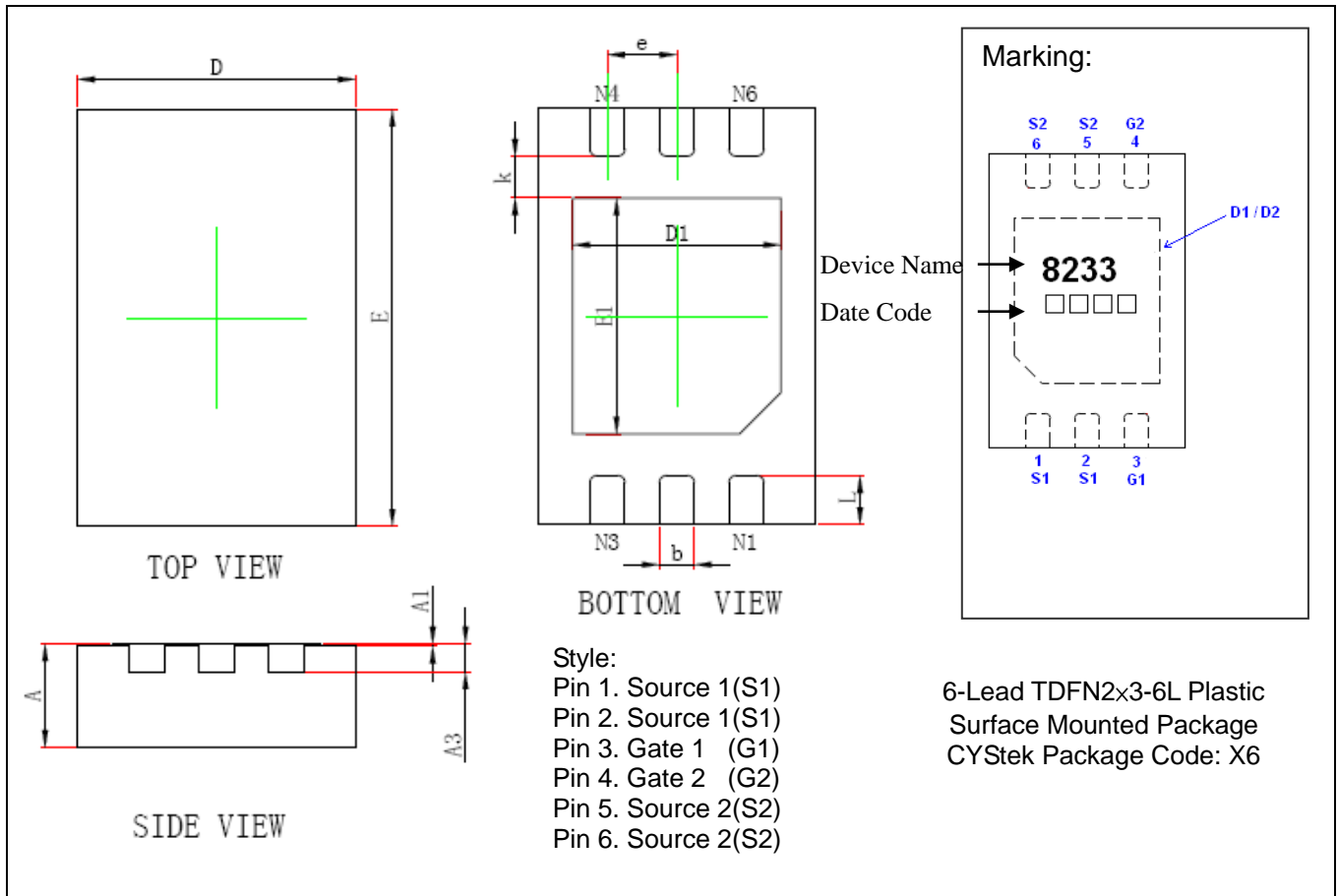
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (Tl)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TDFN2x3-6L Dimension



DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.700	0.850	0.028	0.033	E1	1.650	1.750	0.065	0.069
A1	0.000	0.050	0.000	0.002	k	0.200	-	0.008	-
A3	0.203	REF	0.008	REF	b	0.200	0.300	0.008	0.012
D	1.950	2.050	0.077	0.081	e	0.500	TYP	0.020	TYP
E	2.950	3.050	0.116	0.120	L	0.300	0.400	0.012	0.016
D1	1.450	1.550	0.057	0.061					

Notes : 1.Controlling dimension : millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead :Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.