

N- AND P-Channel Enhancement Mode MOSFET

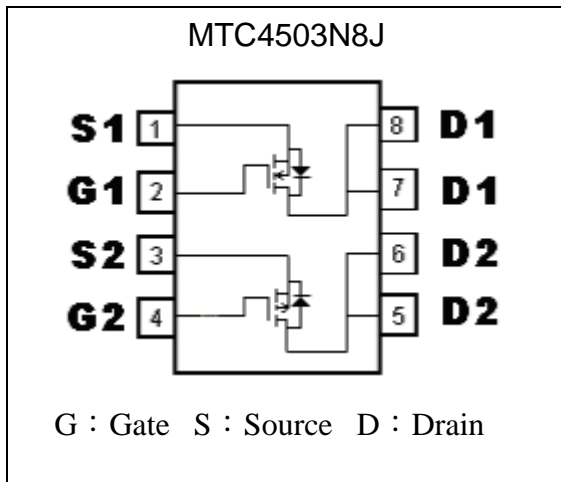
MTC4503N8J

	N-CH	P-CH
BV _{DSS}	30V	-30V
I _D @V _{GS} =10V(-10V), T _A =25°C	6.3A	-5.2A
I _D @V _{GS} =10V(-10V), T _C =25°C	9.1A	-7.6A
R _{DS(on)} @V _{GS} =10V(-10V) typ.	14.4mΩ	23.2mΩ
R _{DS(on)} @V _{GS} =4.5V(-4.5V) typ.	19.1mΩ	32.3mΩ
R _{DS(on)} @V _{GS} =4V(-4V) typ.	21.7mΩ	37.4mΩ

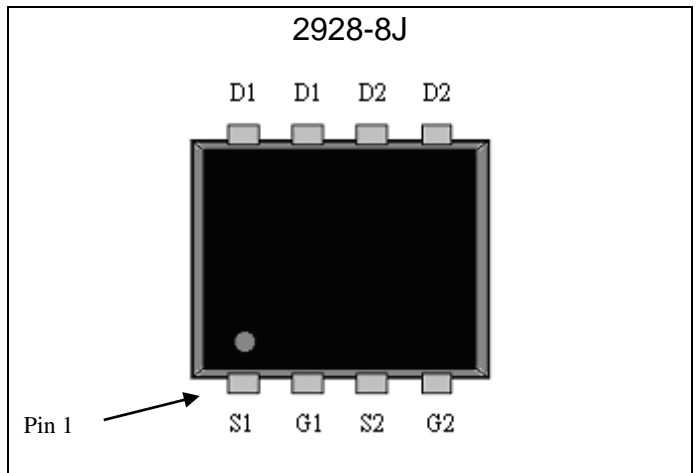
Features

- Simple drive requirement
- Low on-resistance
- Fast switching speed
- Pb-free lead plating and halogen-free package

Equivalent Circuit

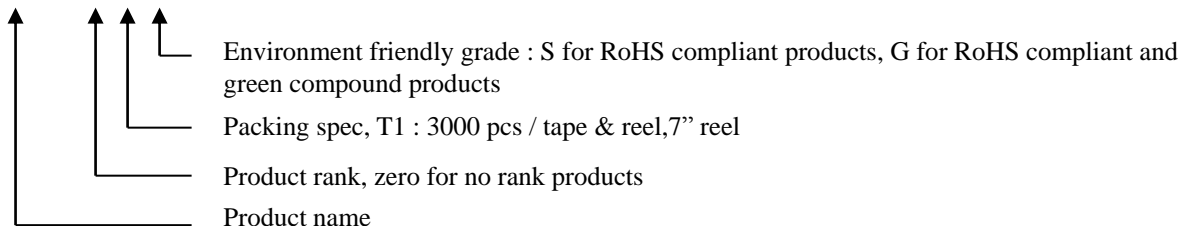


Outline



Ordering Information

Device	Package	Shipping
MTC4503N8J-0-T1-G	2928-8J (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel





Absolute Maximum Ratings (T_C=25°C, unless otherwise noted)

Parameter		Symbol	Limits		Unit
			N-channel	P-channel	
Drain-Source Breakdown Voltage		BV _{DSS}	30	-30	V
Gate-Source Voltage		V _{GS}	±20	±20	
Continuous Drain Current *2	T _A =25 °C, V _{GS} =10V (-10V)	I _{DSM}	6.3	-5.2	A
	T _A =70 °C, V _{GS} =10V (-10V)		5.0	-4.2	
Continuous Drain Current	T _C =25 °C, V _{GS} =10V (-10V)	I _D	9.1	-7.6	
	T _C =100 °C, V _{GS} =10V (-10V)		5.8	-4.8	
Pulsed Drain Current *3		I _{DM}	36	-30	
Total Power Dissipation	T _A =25°C, Single device operation	P _{DSM}	1.5 *2		
	T _A =70°C, Single device operation		0.96 *2		
	T _A =25°C, Single device value at dual operation		1.24 *2		
	T _A =70°C, Single device value at dual operation		0.79 *2		
	T _C =25°C	P _D *1	3.1		
	T _C =100°C		1.2		
Operating Junction and Storage Temperature Range		T _j ; T _{stg}	-55~+150		°C

Thermal Data

Parameter	Symbol	Value	Unit
Max. Thermal Resistance, Junction-to-ambient, single device operation	R _{th,j-a}	84 *2	°C/W
Max. Thermal Resistance, Junction-to-ambient, single device value at dual operation		101 *2	
Max. Thermal Resistance, Junction-to-case	R _{th,j-c}	40	

- Note : 1.The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
2. The value of R_{θJA} is measured with the device mounted on 1 in²FR-4 board with 2 oz. copper, in a still air environment with T_A=25°C, t≤5s. 216°C/W when mounted on a minimum pad of 2 oz. copper. The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
3. Pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low duty cycles to keep initial T_J=25°C.

N-Channel Electrical Characteristics (T_C=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	30	-	-	V	V _{GS} =0V, I _D =250μA
V _{GS(th)}	1	-	2.5		V _{DS} =V _{GS} , I _D =250μA
I _{GSS}	-	-	±100	nA	V _{GS} =±20V, V _{DS} =0V
I _{DSS}	-	-	1	μA	V _{DS} =24V, V _{GS} =0V
	-	-	10		V _{DS} =24V, V _{GS} =0V, T _j =70°C
*R _{DS(ON)}	-	14.4	19	mΩ	V _{GS} =10V, I _D =6A
	-	19.1	26		V _{GS} =4.5V, I _D =6A
	-	21.7	35		V _{GS} =4V, I _D =6A
*G _{FS}	-	5.4	-	S	V _{DS} =10V, I _D =3A



Dynamic					
Ciss	-	521	-	pF	V _{DS} =10V, V _{GS} =0V, f=1MHz
Coss	-	90	-		
Crss	-	72	-		
*td(ON)	-	5.6	-	ns	V _{DS} =15V, I _D =3A, V _{GS} =10V, R _G =10Ω
*tr	-	16	-		
*td(OFF)	-	31	-		
*tf	-	9.4	-		
*Qg	-	6.9	-	nC	V _{DS} =15V, I _D =6A, V _{GS} =5V
*Qgs	-	1.6	-		
*Qgd	-	2.6	-		
Body Diode					
*VSD	-	0.85	1.2	V	V _{GS} =0V, I _S =6A
*trr	-	7.2	-	ns	I _F =6A, V _{GS} =0V, dI _F /dt=100A/μs
*Qrr	-	3.0	-	nC	

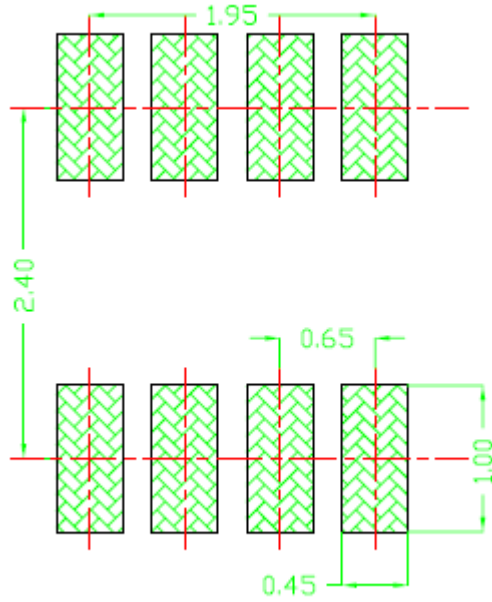
*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

P-Channel Electrical Characteristics (T_c=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	-30	-	-	V	V _{GS} =0V, I _D =-250μA
V _{GS(th)}	-1	-	-2.5		V _{DS} =V _{GS} , I _D =-250μA
I _{GSS}	-	-	±100	nA	V _{GS} =±20V, V _{DS} =0V
I _{DSS}	-	-	-1	μA	V _{DS} =-24V, V _{GS} =0V
	-	-	-10		V _{DS} =-24V, V _{GS} =0V, T _j =70°C
*R _{DSS(ON)}	-	23.2	34	mΩ	V _{GS} =-10V, I _D =-5A
	-	32.3	47		V _{GS} =-4.5V, I _D =-2.5A
	-	37.4	60		V _{GS} =-4V, I _D =-2.5A
*G _{FS}	-	6.2	-	S	V _{DS} =-10V, I _D =-3A
Dynamic					
Ciss	-	947	-	pF	V _{DS} =-10V, V _{GS} =0V, f=1MHz
Coss	-	131	-		
Crss	-	109	-		
*td(ON)	-	6.8	-	ns	V _{DS} =-15V, I _D =-3.5A, V _{GS} =-10V, R _G =10Ω
*tr	-	16.8	-		
*td(OFF)	-	93.4	-		
*tf	-	48.2	-		
*Qg	-	10.7	-	nC	V _{DS} =-15V, I _D =-7A, V _{GS} =-5V
*Qgs	-	3.1	-		
*Qgd	-	3.9	-		
Body Diode					
*VSD	-	-0.85	-1.2	V	V _{GS} =0V, I _S =-5A
*trr	-	9.3	-	ns	I _F =-7A, V _{GS} =0V, dI _F /dt=100A/μs
*Qrr	-	4.3	-	nC	

*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

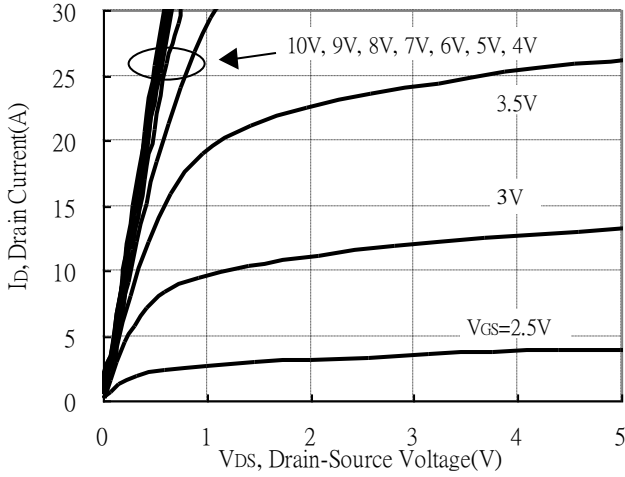
Recommended Soldering Footprint



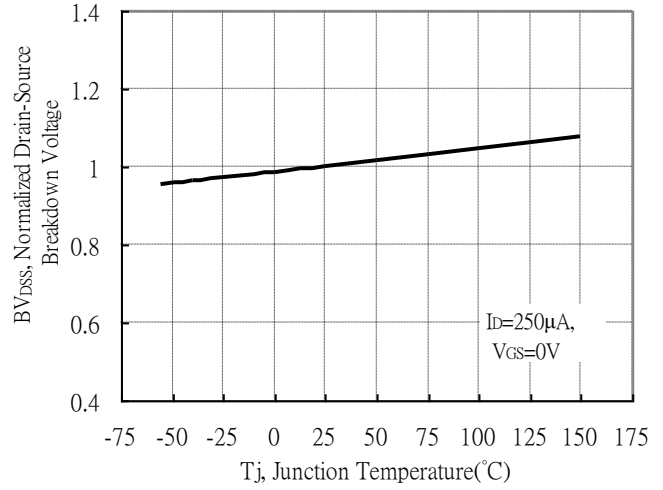
unit : mm

Typical Characteristics : Q1(N-channel)

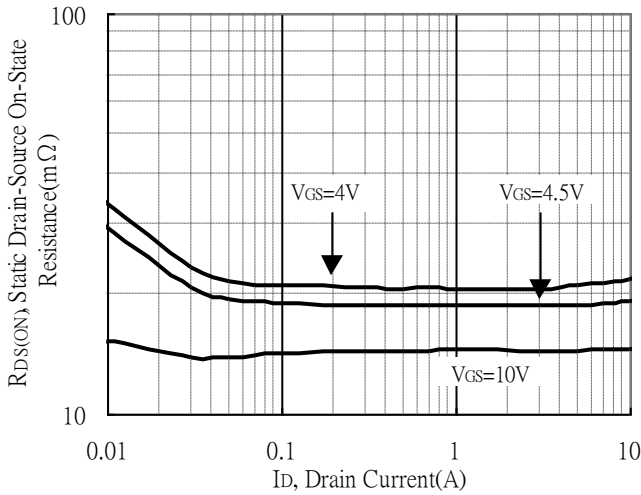
Typical Output Characteristics



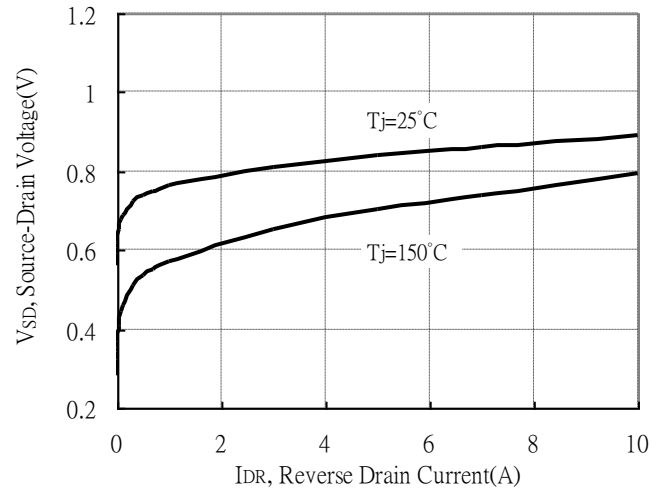
Brekdown Voltage vs Ambient Temperature



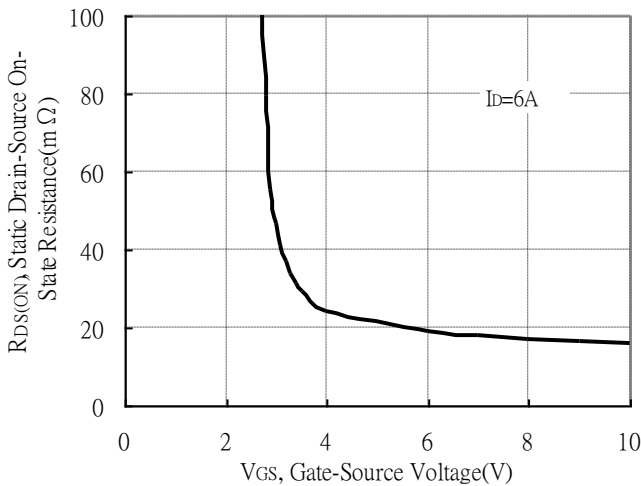
Static Drain-Source On-State resistance vs Drain Current



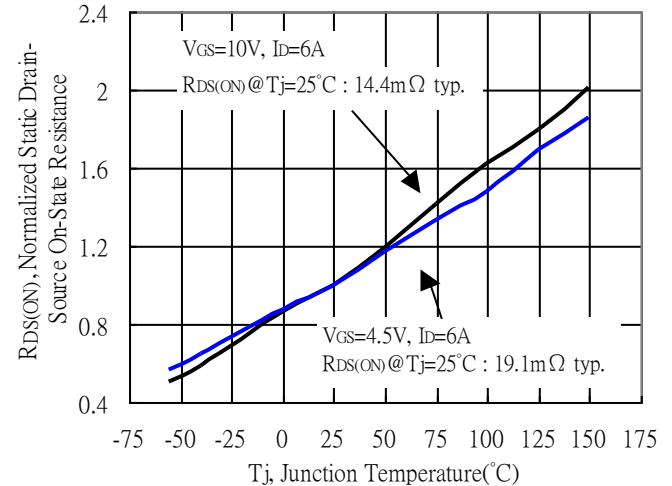
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

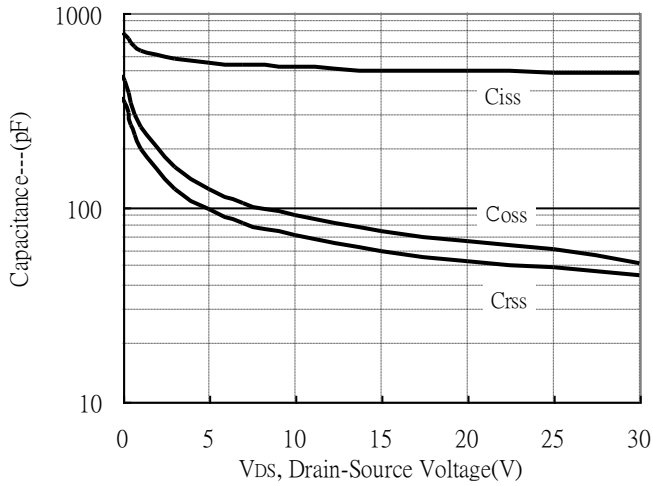


Drain-Source On-State Resistance vs Junction Temperature

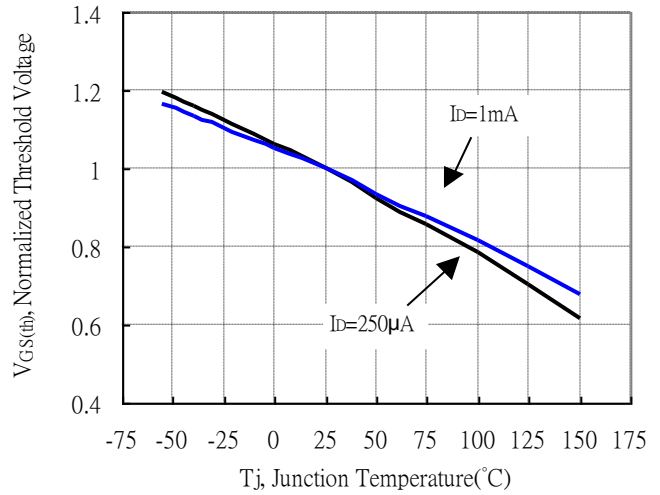


Typical Characteristics(Cont.) : Q1(N-channel)

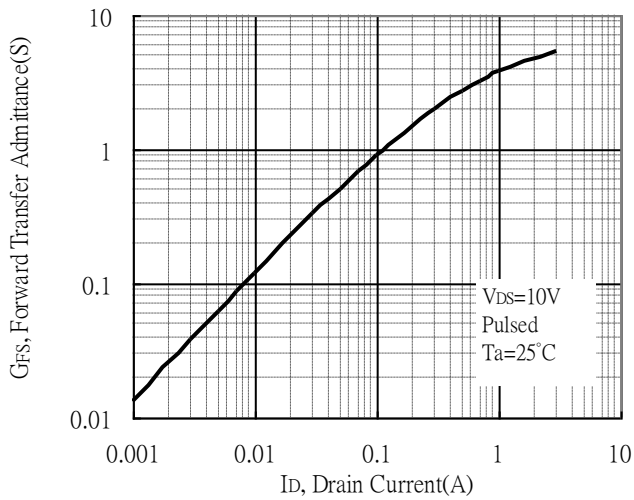
Capacitance vs Drain-to-Source Voltage



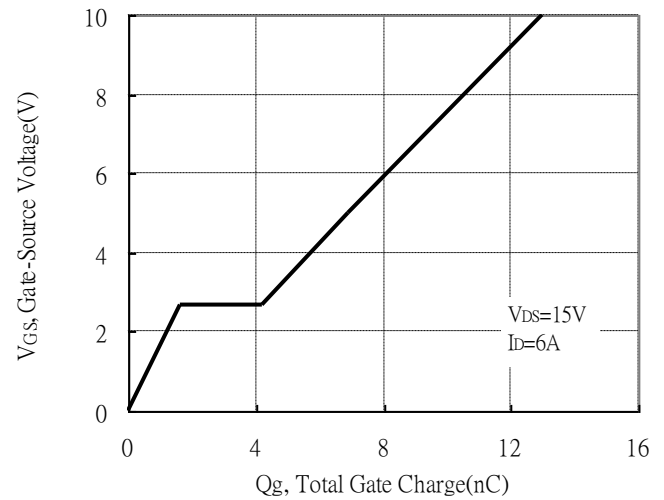
Threshold Voltage vs Junction Temperature



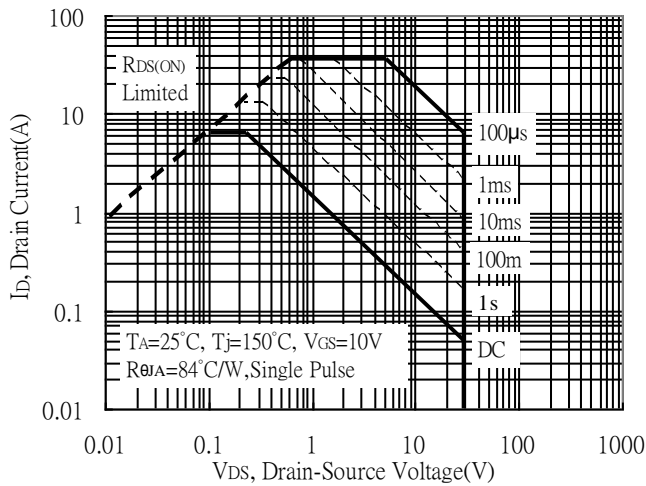
Forward Transfer Admittance vs Drain Current



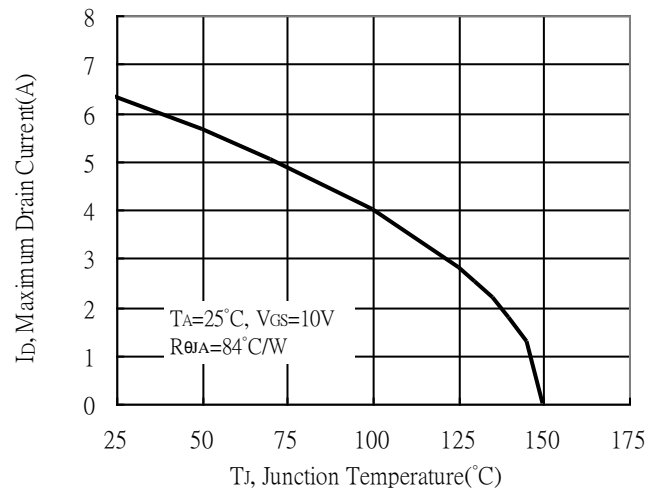
Gate Charge Characteristics



Maximum Safe Operating Area



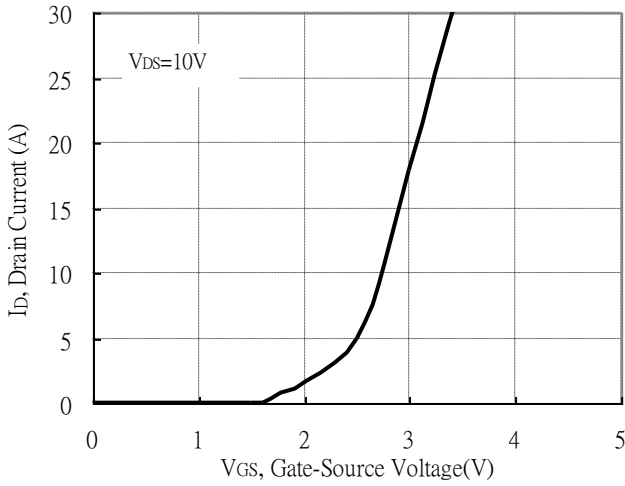
Maximum Drain Current vs Junction Temperature



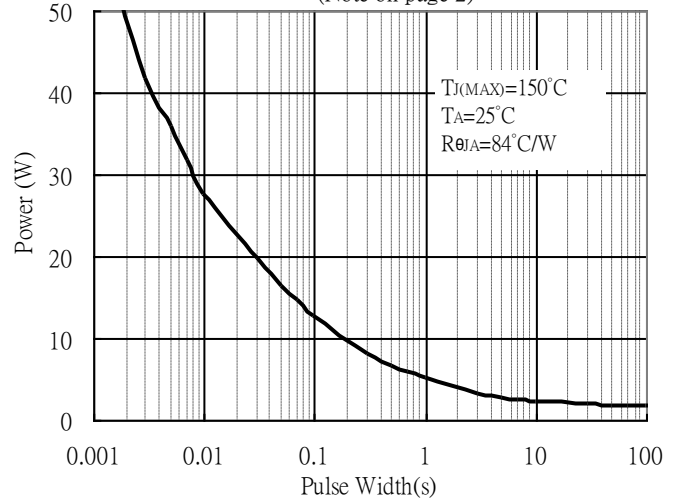


Typical Characteristics(Cont.) : Q1(N-channel)

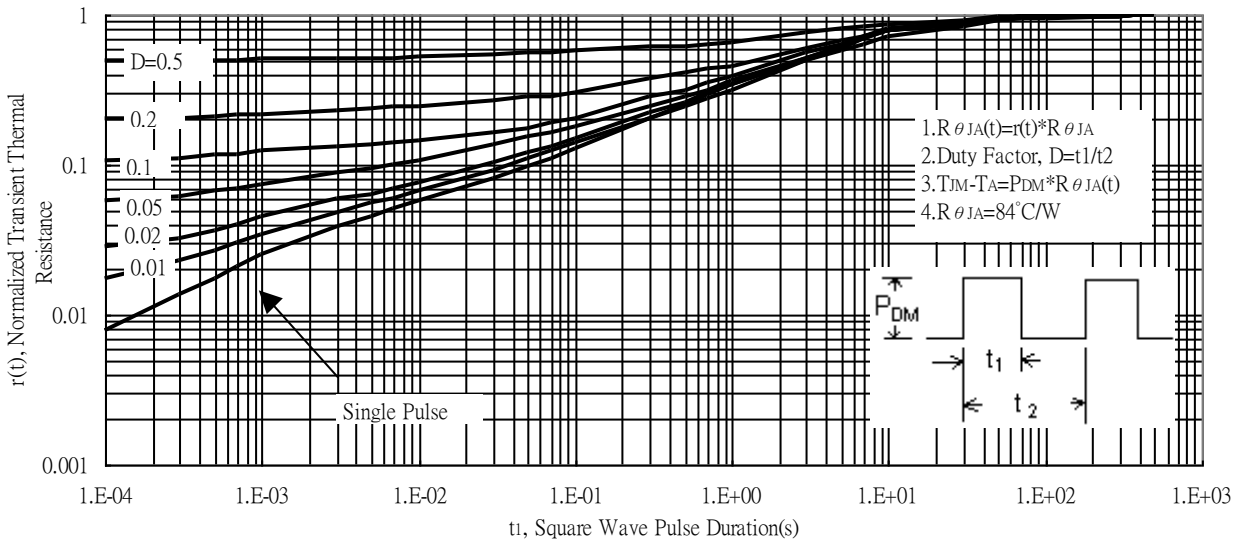
Typical Transfer Characteristics



Single Pulse Power Rating, Junction to Ambient
 (Note on page 2)

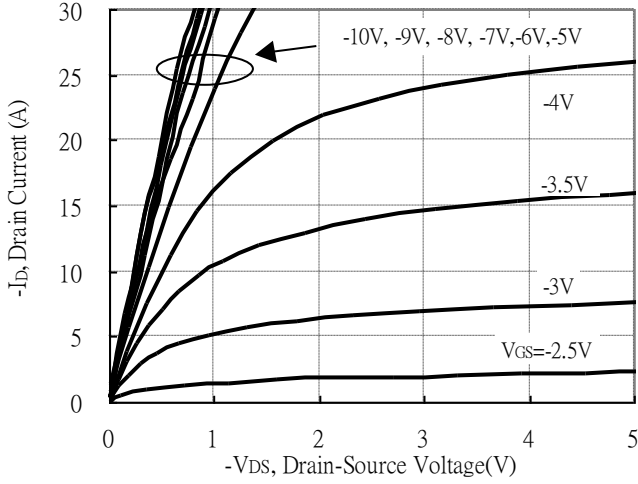


Transient Thermal Response Curves

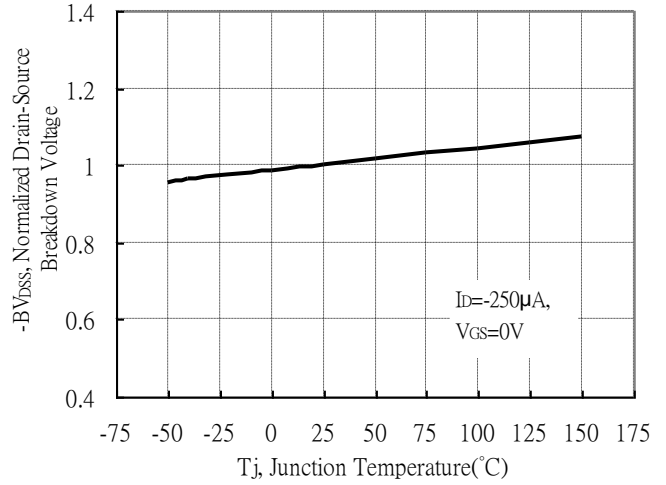


Typical Characteristics : Q2(P-channel)

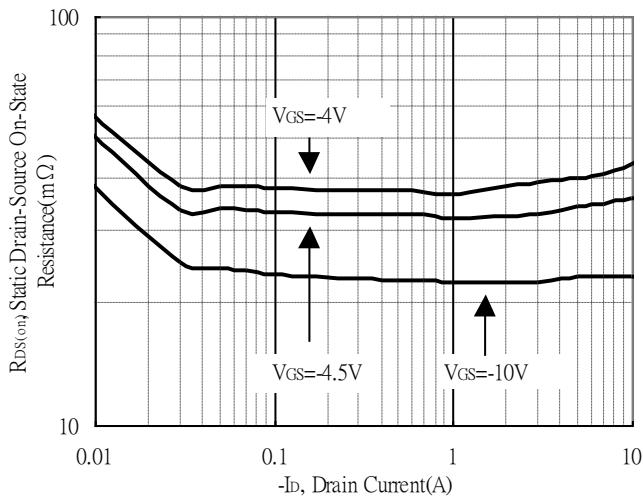
Typical Output Characteristics



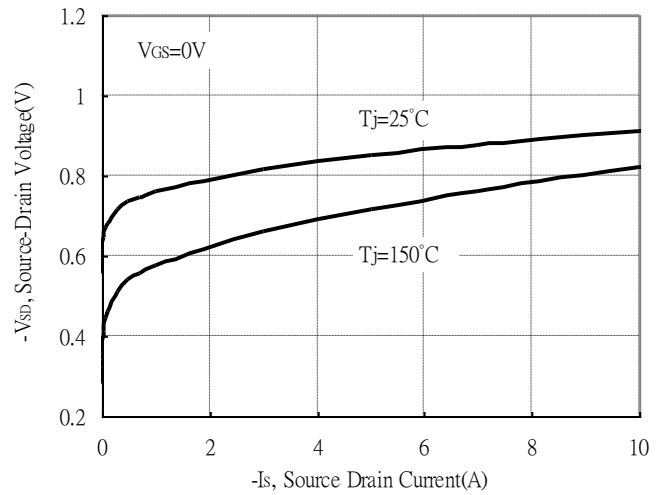
Brekdown Voltage vs Ambient Temperature



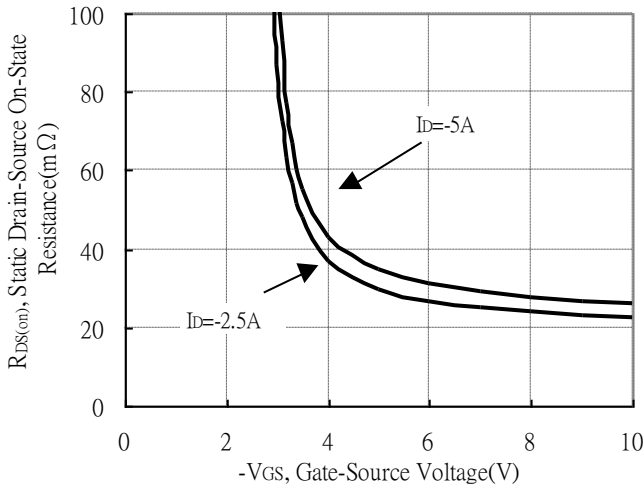
Static Drain-Source On-State resistance vs Drain Current



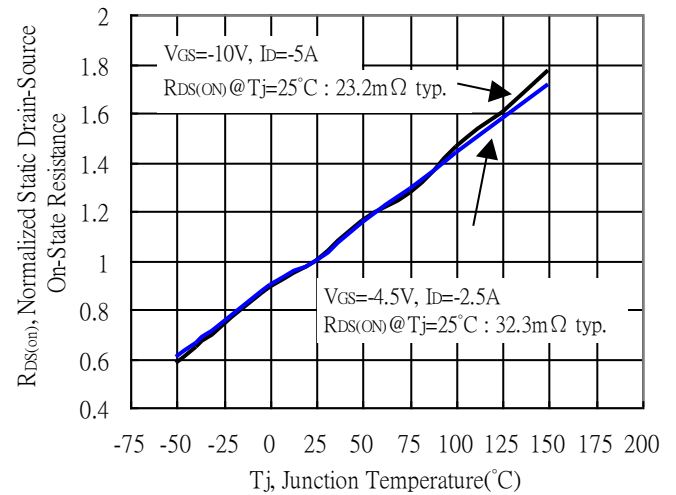
Source Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

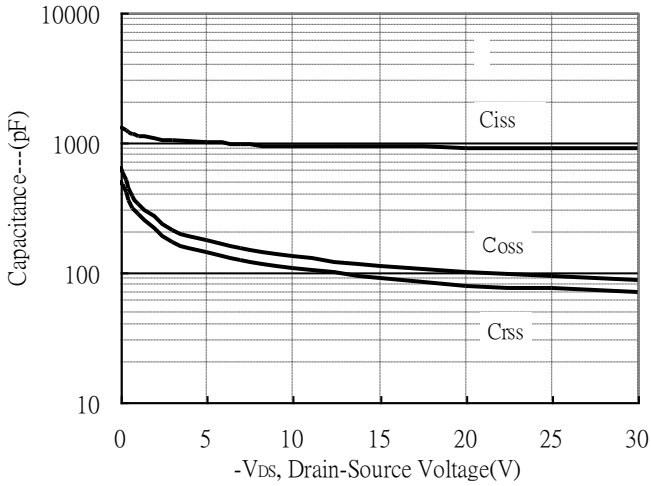


Drain-Source On-State Resistance vs Junction Temperature

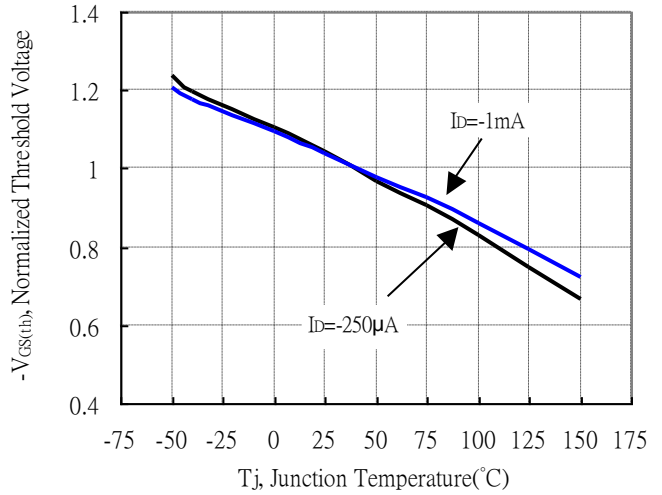


Typical Characteristics(Cont.) : Q2(P-channel)

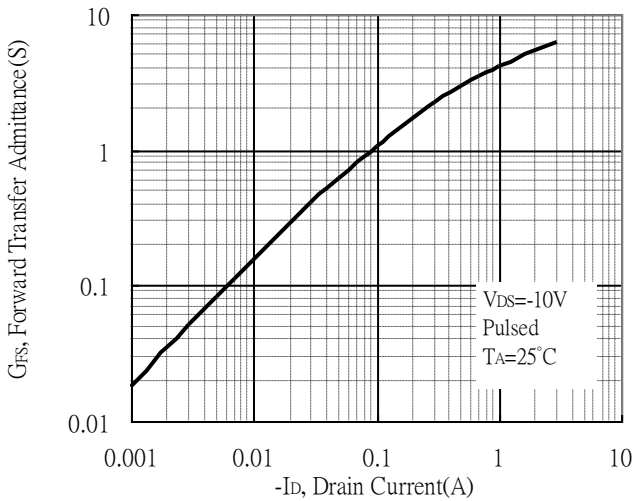
Capacitance vs Drain-to-Source Voltage



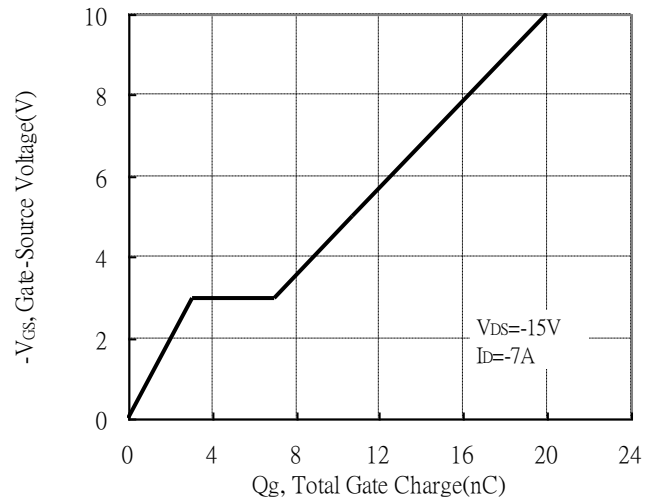
Threshold Voltage vs Junction Temperature



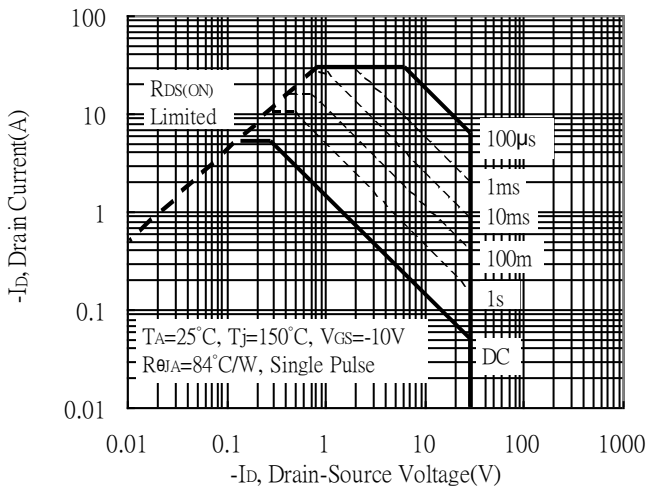
Forward Transfer Admittance vs Drain Current



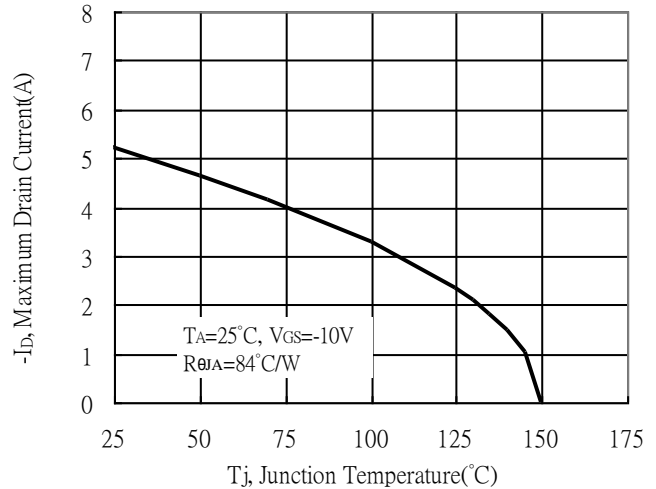
Gate Charge Characteristics



Maximum Safe Operating Area

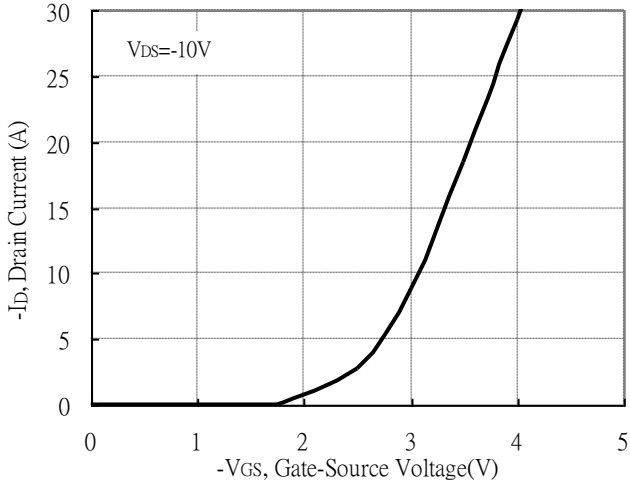


Maximum Drain Current vs Junction Temperature

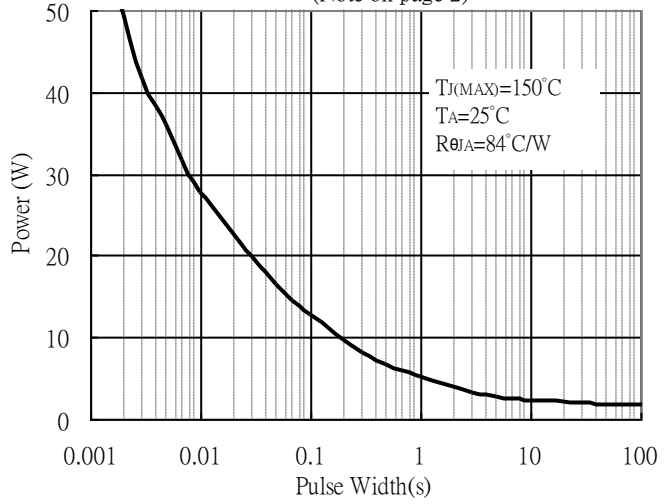


Typical Characteristics(Cont.) : Q2(P-channel)

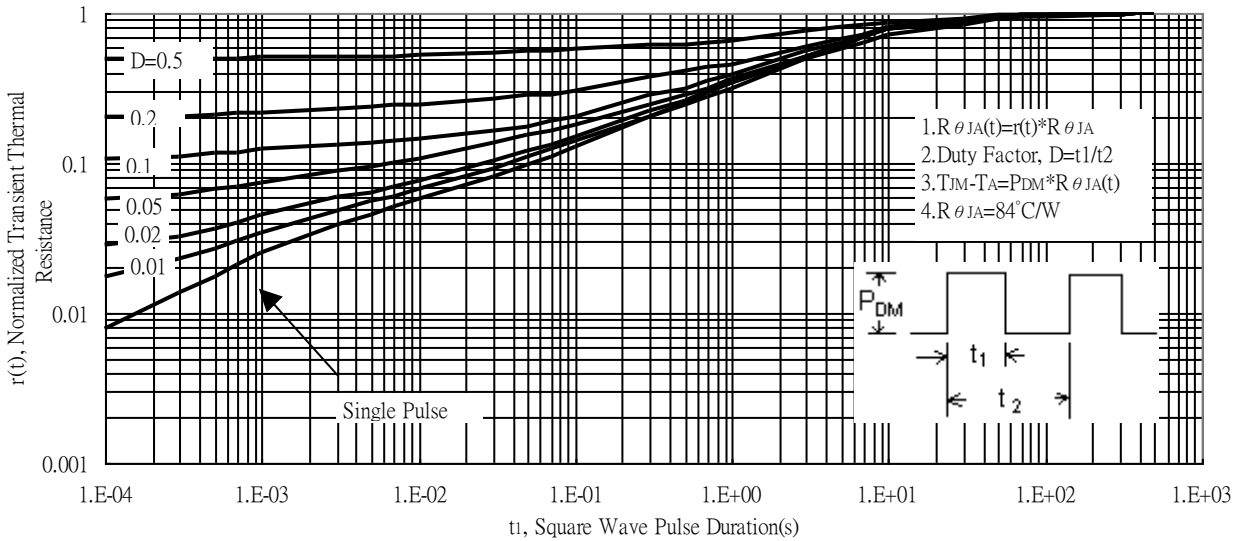
Typical Transfer Characteristics



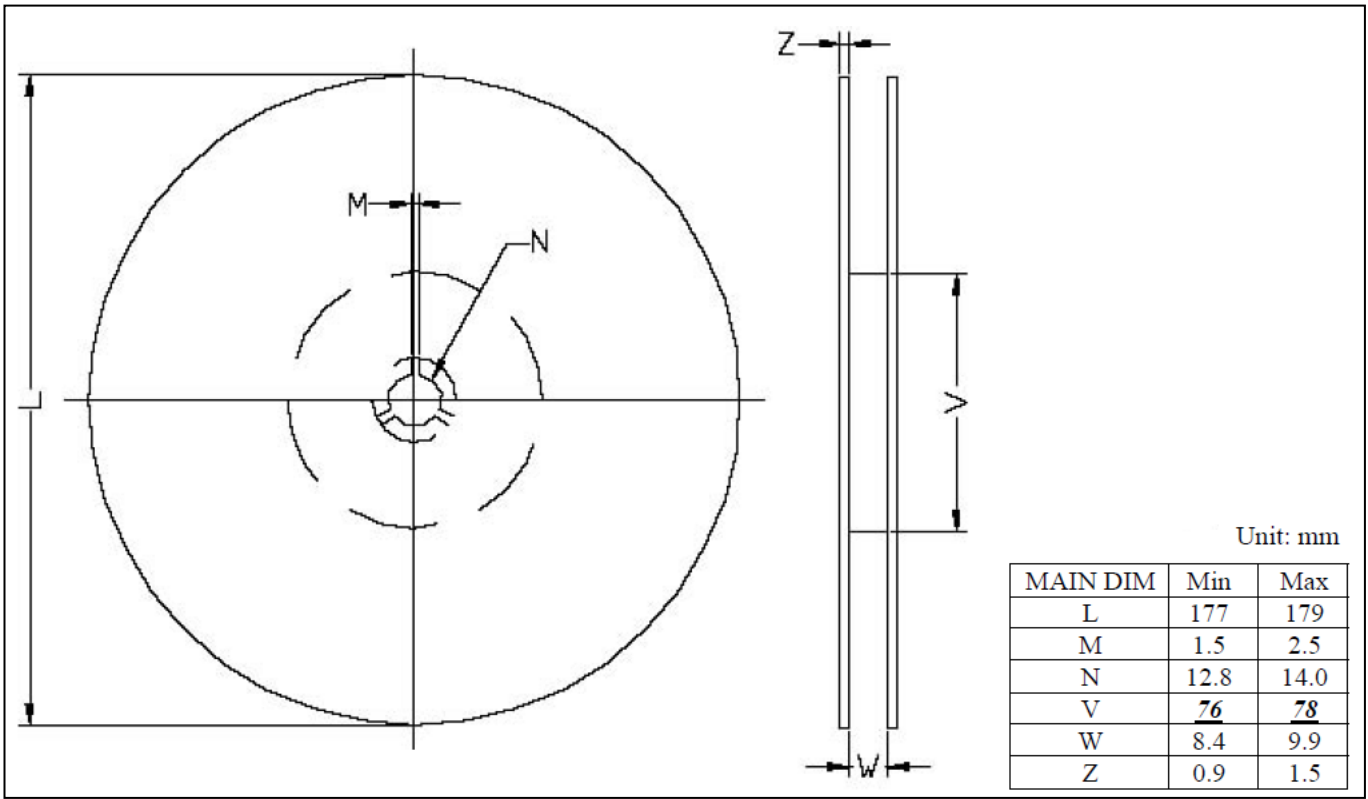
Single Pulse Power Rating, Junction to Ambient
 (Note on page 2)



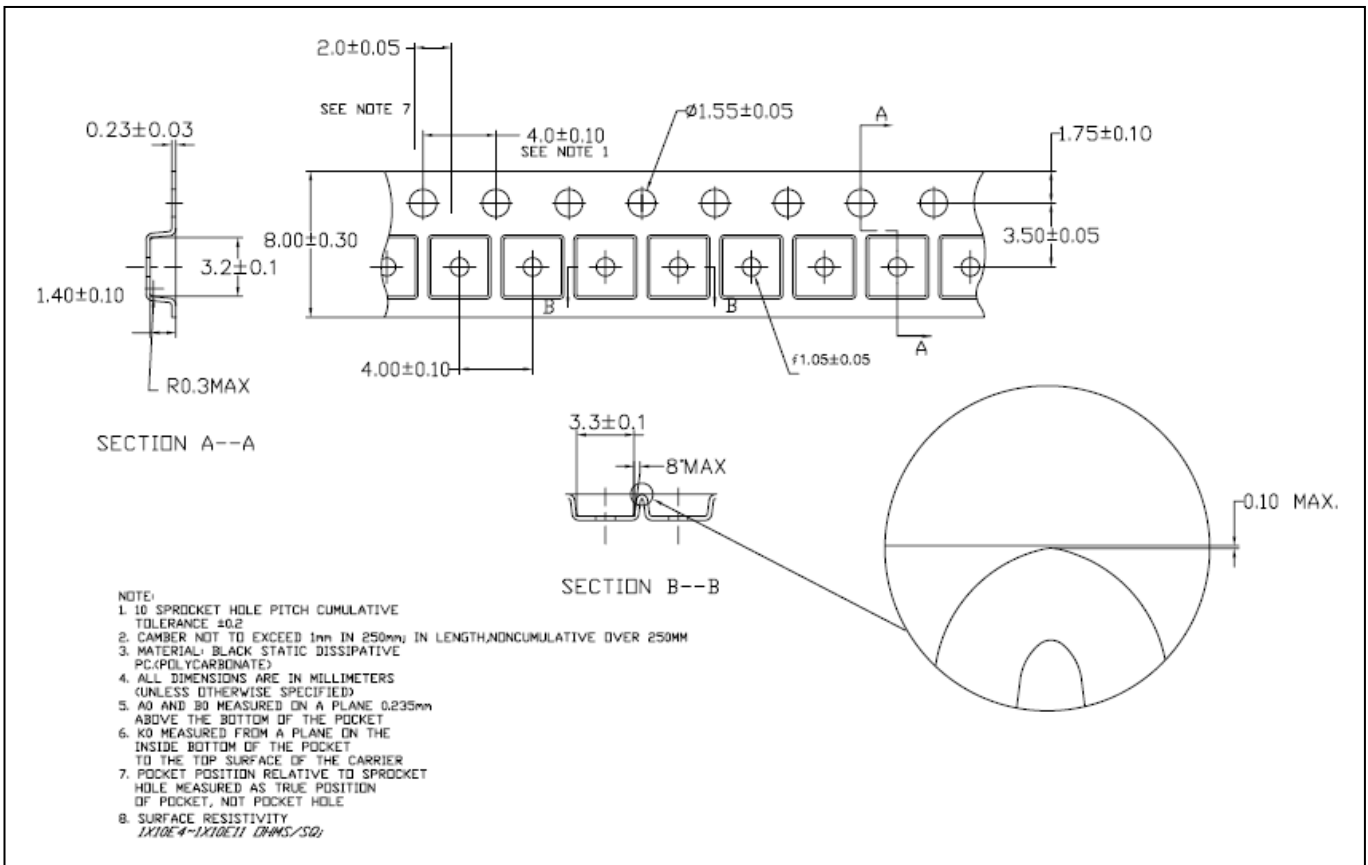
Transient Thermal Response Curves



Reel Dimension



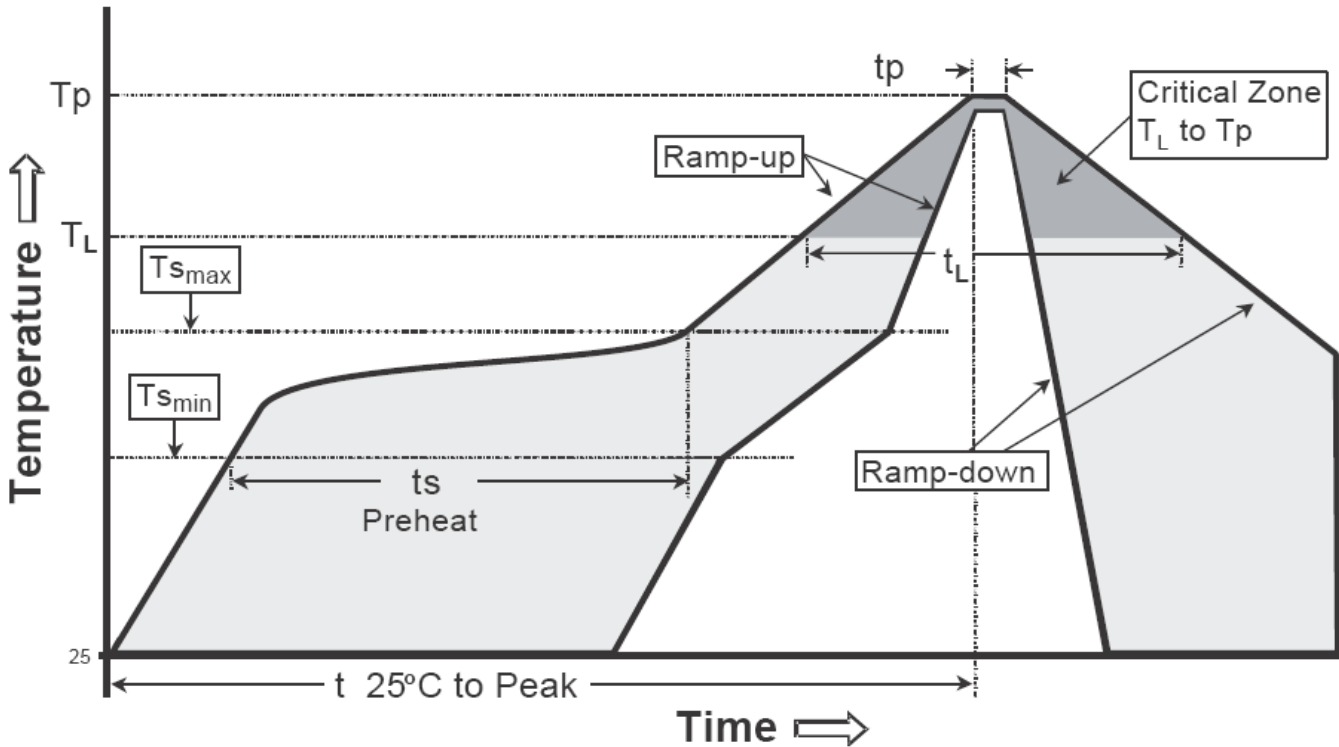
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note :1. All temperatures refer to topside of the package, measured on the package body surface.
 2.For devices mounted on FR-4 PCB of 1.6mm or equivalent grade PCB. If other grade PCB is used, care should be taken to match the coefficients of thermal expansion between components and PCB. If they are not matched well, the solder joints may crack or the bodies of the parts may crack or shatter as the assembly cools.

2928-8J Dimension

Marking:

D1 D1 D2 D2

4503

□□□□(G)

S1 G1 S2 G2

Assembly site code :
 blank →JCET
 G→GEM

8-Lead 2928-8J Plastic Package
 CYStek Package Code: N8J

Date Code(counting from left to right) :

1st code: year code, the last digit of Christian year
 2nd code: month code, Jan→A, Feb→B, Mar→C,
 Apr→D, May→E, Jun→F, Jul→G, Aug→H,
 Sep→J, Oct→K, Nov→L, Dec→M
 3rd and 4th codes : production serial number, 01~99

Note:

1. All Dimension Are In mm.
2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
4. The Package Top May Be Smaller Than The Package Bottom.
5. Dimension "b" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.08 mm Total In Excess Of "b" Dimension At Maximum Material Condition. The Dambar Cannot Be Located On The Lower Radius Of The Foot.

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.935	1.100	0.0368	0.0433	E1	2.300	2.500	0.0906	0.0984
A1	0.010	0.100	0.0004	0.0039	E2	2.650	3.050	0.1043	0.1201
A2	0.925	1.000	0.0364	0.0394	e	0.65 BSC		0.0256	BSC
b	0.250	0.400	0.0098	0.0157	L	0.300	0.600	0.0118	0.0236
c	0.100	0.200	0.0039	0.0079	θ	0°	8°	0°	8°
D	2.950	3.100	0.1161	0.1220	θ1	7° TYP		7° TYP	
E	2.500	3.000	0.0984	0.1181					

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.